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DATA TECHNOLOGY CORPORATION

DTC-11-1 HOST ADAPTER*

FOR THE LSI-11

PRODUCT SPECIFICATION

MARCH 30, 1981

*THE DTC-11-1 HOST ADAPTER HAS AN
ADDRESS BUS WIDTH OF 22 BITS.

09-00163
30 Mar 81

SPEC REVISION RECORD

Revision	Description
10/22/80	DTC-11 Specification for DTC-11 Host Adapter with address bus width of 18 bits. Fabrication revision 00 or 01.
3/16/81	1st Preliminary Specification for DTC-11-1 Host Adapter
3/30/81	DTC-11-1 Specification for DTC-11-1 Host Adapter with address bus width of 22 bits. Fabrication Revision 02.

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1.0 INTRODUCTION

This specification illustrates the manner in which the DTC-11-1 Host Adapter can be used with any of the Data Technology Corporation disk controllers. It further provides the programming mechanism and command block format utilized by the DTC-11-1. The detailed specifications for the DTC controllers can be found in their respective controller documentation.

The DTC-11-1 Host Adapter fits into a single, dual-wide LSI-11 Bus slot and presents one unit load to the bus. The address bus width is 22 bits.

Commands are issued to the controller through the host adapter in the host computer. The controller accepts data from the host adapter and transfers the data to the correct location on the disk. In addition, the controller will detect/correct burst errors from the fixed disk drive (four bits in length) before data is transferred to the computer.

2.0 DISK SUBSYSTEM

The DTC-11-1 host adapter and a DTC fixed disk controller together comprise one part of a disk storage subsystem. Each of the controllers complies with the interface requirements for the particular disk drive - so that installation is fairly simple. In addition, the DTC-11-1 Host Adapter will operate with any DTC controller/formatter with the standard DTC host interface.

2.1 Theory of Operation

Disk commands are issued to the DTC controller via commands stored in the main LSI-11 memory (the command structure is described in section 4.0 of each of the DTC controller specifications). Depending on the type of command, the controller will request up to 10 command bytes. Upon receipt of the last command byte, the controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status is flagged if it exceeds the drive limits. The data is stored in a sector buffer on the controller before it is transferred to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will store the completion status in a register in the host adapter. (Further delineation of the completion status may be requested by issuing the appropriate sense commands.)

Odd parity is generated by the DTC controllers for all information that is transferred to the host adapter. If enabled, the DTC controller will flag any information that it receives with bad parity from the host adapter.

2.2 Electrical Interface

The electrical interface to the Winchester disk drives and flexible drives will conform to the requirements described in the fixed disk and flexible disk interface specifications.

The electrical interface to the LSI-11 Bus will conform to the particular requirements of the LSI-11 backplane.

3.0 DTC-11-1 HOST ADAPTER

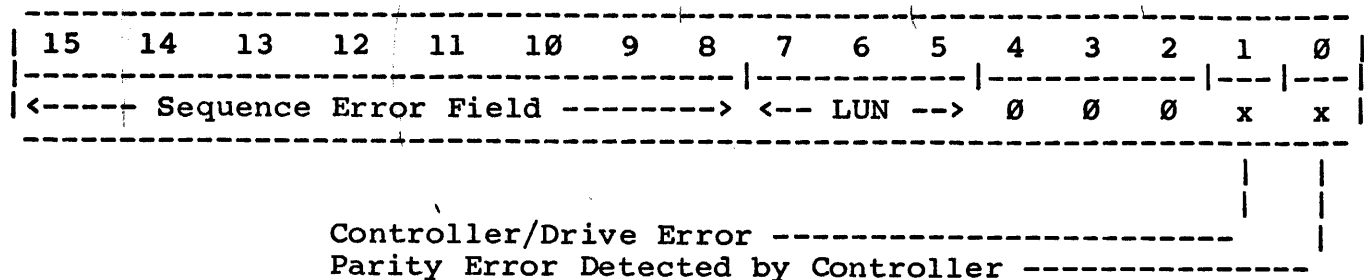
3.1 Interface Register Definition

The DTC-11-1 Host Adapter is controlled by six interface registers. These are as follows:

- 1) Command Completion Status Register(CCSR) (BASE ADDR)
- 2) Control/Status Register(CSR) (BASE ADDR + 2)
- 3) Data Buffer Address Register(DAR) (BASE ADDR + 4)
- 4) Command Buffer Address Register(CAR) (BASE ADDR + 6)
- 5) Extension Data Address Register(XDAR) (BASE ADDR + 10)
- 6) Extension Command Address Register(XCAR) (BASE ADDR + 12)

3.1.1 Command Completion Status Register - CCSR

This is a read-only register that contains the status byte returned by the controller after the completion of a command.



Controller/Drive Error - Set if the controller detected an error during the execution of a command. A Request Sense Command should be issued to the controller to determine the source of the error. This bit is not set on a Correctable Data Error.

Parity Error Detected - Set if the controller detected a parity error on the host bus while receiving data/commands from the host adapter.

LUN - This contains the Logical Unit Number of the drive on which the error occurred. The value that is returned in this field should be used when issuing a REQUEST SENSE Command.

Sequence Error - After DONE is set, if any bits in the upper byte of this word are set, a sequence error has occurred. The circumstances that can cause this are:

- 1) Parity errors to controller
- 2) NXM during data transfers to the host adapter.

Retry action in this circumstance is performed by re-issuing the command.

3.1.2 Control/Status Register - CSR

This register contains the error status indicators and control function bits for the controller.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	0	19	18	17	16	x	x	19	18	17	16	x	x
A	N	P					C		D				D	F	G
n	X	a					o		o				a	o	o
y	M	r					m		n				t	r	
E		i					a		e				a	c	
r		t					n		r			X		e	
r		y					d		u			M		R	
r		E					X		p			A		e	
		r					M		t					s	
		r					A		E					e	
									n					t	
									a						
									b						
									l						
									e						

- Any Error (read only) - Set if any error occurred. Logical "OR" of bits 14-13 in the CSR and bits 0 & 12 in CCSR. Cleared by any write to CSR.
- NXM (read only) - Non-existent memory error. Set if the host adapter did not receive a BRPLY within 100us from the memory during a memory transfer. In those DTC controllers that do not timeout on receiving the Acknowledge signal from the host adapter, a NXM condition will cause both DONE and an interrupt to occur (if Interrupt Enable is set). At this time the controller will hang waiting for Acknowledge. After DONE is set, the controller must be reset to clear this condition before any other command is issued. This bit is cleared by any write to the CSR. (Refer to the appropriate controller specification to determine whether or not the controller times out on the reception of Acknowledge from the host adaptor.)

- Parity Error (read only) - Set if the host adapter detected a parity error while receiving data from the controller. Cleared by any write to the CSR.
- Command XMA (write only) - These bits represent the BDAL 19 thru 16 bits used for extended addresses on the LSI-11 bus during the fetch of a command block. These bits are write only and are read as ones.
- DONE (read only) - Set by the controller at the end of a command. This bit is cleared by a write to the CSR.
- Interrupt Enable (read/write) - When set, allows DONE to generate an interrupt request to the LSI-11. This bit is cleared by a reset.
- Data XMA (write only) - These bits represent the BDAL 19 thru 16 bits used for extended addresses on the LSI-11 bus during the fetch/store of data between the host adaptor and the LSI-11 memory. These bits are write only and are read as ones.
- Force Reset (write only) - When set, the host adapter sends a reset to the controller. This bit is logical "OR'd" with the BINIT signal. The following bits are cleared by INIT or FORCE RESET:

- 1) Any Error
- 2) NXM
- 3) Parity Error
- 4) BOOT
- 5) DONE
- 6) Interrupt Enable
- 7) GO

The following bits are not cleared on INIT or FORCE RESET:

- 1) Command XMA
- 2) Data XMA
- 3) DAR
- 4) CAR

- Go (set/read) - When written with a "1", this bit indicates to the controller that a command is ready to be read from the DTC-11-1 memory. This bit is cleared when the controller responds to the host adapter and begins the command fetch phase. The GO bit may be set immediately following a FORCE RESET condition.

3.2 Software Theory of Operation

The method by which a command is executed is as follows:

- 1 - Device driver builds a Command Descriptor Block (CDB) in system memory (see section 4.0 of the DTC controller specifications).
- 2 - The driver then writes the address of the first word of the CDB into the Command Address Register (CAR) and the Extension Command Address Register (XCAR) of the host adapter. The command bytes will be sent to the controller, low byte first, high byte next.
- 3 - The DAR & XDAR are also set up if a data transfer is required. Commands requiring data transfers are READ, WRITE, READ ID, REQUEST SENSE, REQUEST SYNDROME, WRITE ECC. As in the command byte transfer, the data bytes are transferred between the controller and the LSI-11 memory; low byte first, high byte next, beginning at the address in the DAR. Transfers are always begun on a word boundary.
- 4 - The driver can also set the Interrupt Enable bit in the CSR to enable the host adapter to interrupt the LSI-11 upon command completion.
- 5 - The driver now sets Go in the CSR to indicate that the command is ready to be executed. Interrupt Enable bit must be written concurrently if interrupts are required. (Also, the memory address bits 16-19 should be written into the CSR at this time.)
- 6 - The controller responds to the host adapter by clearing the Go bit and begins the command byte fetch phase. The controller fetches the command bytes via the CAR. Although the controller communicates in bytes, the host adapter always transfers 16-bit words across the LSI-11 bus.
- 7 - The controller verifies that the command is correct and begins the command execution phase. At this time the data is transferred to the host adapter and into the LSI-11 memory via the DAR.
- 8 - After the data transfer is completed, the controller enters the command completion phase. The controller sends a one-byte status to the host adapter indicating whether or not an error occurred during command execution. Finally, the controller sends the message byte (of zeroes) which sets the DONE bit in the host adaptor.

- 9 - At this time the controller enters the idle mode awaiting another command. If any error was encountered by the controller, the appropriate bit in the CCSR is set. It is the responsibility of the device driver to issue a REQUEST SENSE command to request any detailed information about the error.
- 10 - Note that all transfers between the host adapter and the LSI-11 Bus are word transfers.

3.3 Hardware Theory of Operation

The DTC-11-1 host adapter is capable of functioning in the following three modes on the LSI-11 bus:

- 1) Slave Mode
- 2) Direct Memory Access (DMA) Mode
- 3) Interrupt Mode

3.3.1 Slave Mode

In Slave Mode, the host adapter recognizes its address during the addressing portion of the LSI-11 bus cycle. The assertion of BSYNC on the bus latches the address selection logic in preparation for the receipt of the BDATI or BDATO signal. During a BDATI sequence, the data from the selected register is enabled onto the bus at the leading edge of BDATI, and is held onto bus for the duration of this signal. BRPLY is delayed by approximately 100ns to assure data stability on the system bus. During a BDATO sequence the data is written into the register for the duration of the BDATO signal.

3.3.2 Direct Memory Access (DMA) Mode

DMA mode is entered upon the assertion of the GO bit in the CSR. A DMA cycle on the LSI-11 bus is performed for each word transferred. When the host adapter needs to perform a data transfer across the LSI-11 bus, it issues BDMR to request bus mastership. When BDMG is asserted, the host adapter asserts BSACK and enters the LSI-11 bus cycle timing. The timing conforms to the DEC LSI-11 processor handbook. After the cycle has ended, the host adapter deasserts BSACK to release the bus and responds correctly to the controller.

If the data transfer is from the controller, the host adapter will accumulate two bytes before a DMA request is issued to the LSI-11 bus. If the data transfer is to the controller, the host adapter (upon receipt of REQ from the controller) first issues a DMA request to the LSI-11 bus. After the word is in the host adapter and the BSACK is deasserted, the host adapter then transmits each byte to the controller over the controller host bus.

3.3.3 Interrupt Mode

The interrupt channel in the host adapter can be enabled by setting the particular bit in the CSR. Upon receipt of the message byte of zeroes from the controller, the host adapter asserts DONE in the CSR and asserts BIRQ on the LSI-11 bus. Upon receipt of BIAKI, the host adapter enables the vector onto the BDAL lines and asserts BRPLY 100ns later. BRPLY and the BDAL lines will remain asserted for the duration of BIAKI.

4.0 ELECTRICAL/MECHANICAL SPECIFICATIONS

Host Adapter Physical Parameters

(The DTC-11-1 fits into a dual height slot in the LSI-11 backplane)

Width	5.2	inches
Length	8.4	inches
Height	0.75	inch
Weight	0.7	lbs.

NOTE

Be sure there are no vacant slots between the host adapter and the LSI-11 processor board; otherwise the DMA and Interrupt Grant signals will not be routed to the host adapter board.

Environmental Parameters

	Operating:	Storage:
Temperature (degrees F/C)	32/0 to 131/55	-40/-10 to 167/75
Relative Humidity (@ 40 degrees F, wet bulb temp, no condensation)	10% to 95%	10% to 95%
Altitude	sea level to 10K feet	sea level to 15K feet

Power Requirements

Voltage @ current(host adapter) +5 VDC @ 2A (max)

NOTE

For the physical parameters of the controller, refer to its DTC controller specification.

5.0 INSTALLATION

5.1 Inspection

Inspect all shipping containers for damage. If a container is damaged, retain until the contents are checked and the host adapter is verified electrically. If the host adapter is damaged, call Data Technology Corporation Customer Service for Return Material Authorization number. Please retain all shipping labels and documentation.

5.2 Preparation for Use

Before the host adapter can be used, initial setup may be required. Be sure the power requirements for the host adapter are met (section 4.0). The host adapter is installed into a vacant slot in the LSI-11 backplane. Be sure there are no vacant slots between the host adapter and the LSI-11 processor board (propagation of the grant signals).

A 50-pin, mass-terminated cable connects the host adapter to location J6 on the DTC controller board (pin 1 is marked on both the host adapter and the controller silkscreen). Refer to the interconnection diagram in the appropriate controller specification for connection of the controller to the disk drives. Note that all cables (including drive cables) are of the mass-terminated type, so no inadvertant signal swapping can occur.

Be sure the controller has adequate DC power (refer to the controller specification; the controller maintains the same power connector pinouts as the disk drive). To set up the controller, refer to the switch setting instructions in the controller specification.

The following sections describe in detail the proper jumper settings on the host adapter.

5.2.1 Address Selection Switches

The base address of the host adapter is determined by the Address Selection jumpers on the board. The address range is 160000 - 177760 in the I/O page (BBS7 asserted).

Factory default is 177460.

<u>Location</u>	<u>Address Bit</u>	
W1	BDAL 12	shorted = compare with zero open = compare with one (asserted)
8D - 1	BDAL 11	on = compare with zero (deasserted)
8D - 2	BDAL 10	off = compare with one (asserted)
8D - 3	BDAL 9	
8D - 4	BDAL 8	
8D - 5	BDAL 7	
8D - 6	BDAL 6	
8D - 7	BDAL 5	
8D - 8	BDAL 4	

5.2.2 Interrupt Vector Selection

The interrupt vector selection is performed in a similar manner. The range is 000 - 374.

Factory default is 134

<u>Location</u>	<u>Address Bit</u>	
3F - 1	BDAL 7	on = transmit zero (deasserted)
3F - 2	BDAL 6	off = transmit one (asserted)
3F - 3	BDAL 5	
3F - 4	BDAL 4	
3F - 5	BDAL 3	
3F - 6	BDAL 2	
3F - 7	not used	
3F - 8	not used	

5.2.3 Receive Parity Enable Selection (near location 5A)

If E-F are jumpered, the host adapter will not generate/compare parity bits during transfers with the controller.

If D-E are jumpered, ODD parity will be generated/compared during transfers over the host bus. (Unless trace is cut, this mode is default).

Note: If the host adapter has parity enabled, the controller must have parity enabled also.

5.2.4 Interrupt Priority Selection (near location 6J)

<u>Jumper Name</u>	<u>Q-Bus Signal</u>	Jumper across for connection; only one jumper installed
J-H	BIRQ 4	
E-F	BIRQ 5	
C-D	BIRQ 6	
A-B	BIRQ 7	

NOTE:

1. LSI-11/23 is the only CPU version that allows priority other than 4. Factory default is J-H.
2. The host adapter requires the POSITION DEPENDENT method of interrupt priority for installation in the LSI-11/23 bus. Since the DTC controller has an on-board full sector buffer, the host adapter may be set to any interrupt level.

5.3 Initial Checkout

The initial verification of the disk subsystem can be done via the LSI-11 operator's console. First, verify that all the interface registers are accessible through the correct addresses and that the registers can be read/written with the expected results. (Keep in mind that the CCSR will only be written into during the processing of a command, so initially it may contain non-zero information.)

Next, attempt to issue a few commands to the disk subsystem again via the console. Referring to this specification and section 4.0 of the controller specification, set up a command in LSI-11 memory. The following example sets up a read command of block zero on LUN 0. The statements preceded by "@" are generated by the console program in the LSI-11; the underlined statements are to be executed by the user.

```
@1000/ xxxxxx 10<line feed> ;read block command
@1002/ xxxxxx 0<line feed>
@1004/ xxxxxx 1<carriage return> ;one block transfer
@177466/ xxxxxx 1000<up arrow> ;the first word of the command
@177464/ xxxxxx 2000<carriage return> ;the data buffer address
@177470/ xxxxxx 0<line feed> ;XDAR
@177472/ xxxxxx 0<carriage return> ;XCAR
@177462/ xxxxxx 1<carriage return> ;set the GO bit
@177462/ 007674 <carriage return> ;this is the correct
completion result. If bit 15
is set, an error has
occurred. The error will be
posted in the controller
LED's and will be returned
via the REQUEST SENSE
command.

@177460/ 000000 ;this is the correct
completion result.
```

After the command has been completed correctly, the address registers for both the command and the data will point to the next memory location.

A recommended approach is to first issue a RECALIBRATE command. After verifying that it executed correctly, issue a SEEK command to verify the Logical Address calculation is performed correctly. Then issue a FORMAT DRIVE command; the recommended interleave for the LSI-11 is 2. Finally, the data transfer command should be issued to verify the data. All commands can be issued via the console programmer's interface.

6.0 REFERENCE DOCUMENTATION

This section provides the user with information regarding the documentation available for use with the DTC-11-1 Host Adapter.

6.1 DTC Supplied Documentation

6.1.1 DTC Controller Specification

Each controller manufactured by DTC is described by its own specification. Refer to the appropriate controller document when attempting to program the disk subsystem.

6.1.2 RT-11 Installation Guide

When the RT-11 package is purchased from DTC, a system generation guide is provided to incorporate the DTC generated drivers.

6.2 Other Documentation

6.2.1 Digital Equipment Corporation

- a. Microcomputer Processor Handbook
- b. Memories and Peripherals Handbook

6.2.2 Drive Manufacturer Documentation

Refer to the appropriate disk drive specification for your drive.

Appendix A COMMANDS/PROGRAMMING

An I/O request to the DTC controller is performed by passing a command descriptor block (CDB) to the controller. The first byte of a CDB is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, and number of blocks to transfer. The controller performs an implied seek and verify when commanded to access a block.

Due to the different types of commands each controllers recognizes, the command format for the host adapter will only indicate the skeletal representation of the command. The user is directed to section 4.0 of the appropriate DTC controller specification for more detailed command information.

A.1 Command Format

A.1.1 Commands Requiring 8 Bytes (or 4 words)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Command Byte 1								Command Byte 0								XXXXXXX
Command Byte 3								Command Byte 2								XXXXXXX + 2
Command Byte 5								Command Byte 4								XXXXXXX + 4
Command Byte 7								Command Byte 6								XXXXXXX + 6
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

XXXXXXX is the octal address that is loaded into the CAR

A.1.2 Commands Requiring 10 Bytes (5 words)

This command requires 5 words.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Command Byte 1								Command Byte 0								XXXXXXX
Command Byte 3								Command Byte 2								XXXXXXX + 2
Command Byte 5								Command Byte 4								XXXXXXX + 4
Command Byte 7								Command Byte 6								XXXXXXX + 6
Command Byte 9.								Command Byte 8.								XXXXXXX + 10
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

A.2 Request Syndrome Command

The Request Syndrome Command returns 2 bytes of information. The data returned for the Request Syndrome Command is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Byte 1								Byte 0								XXXXXX

XXXXXX is the octal address that is loaded into DAR.

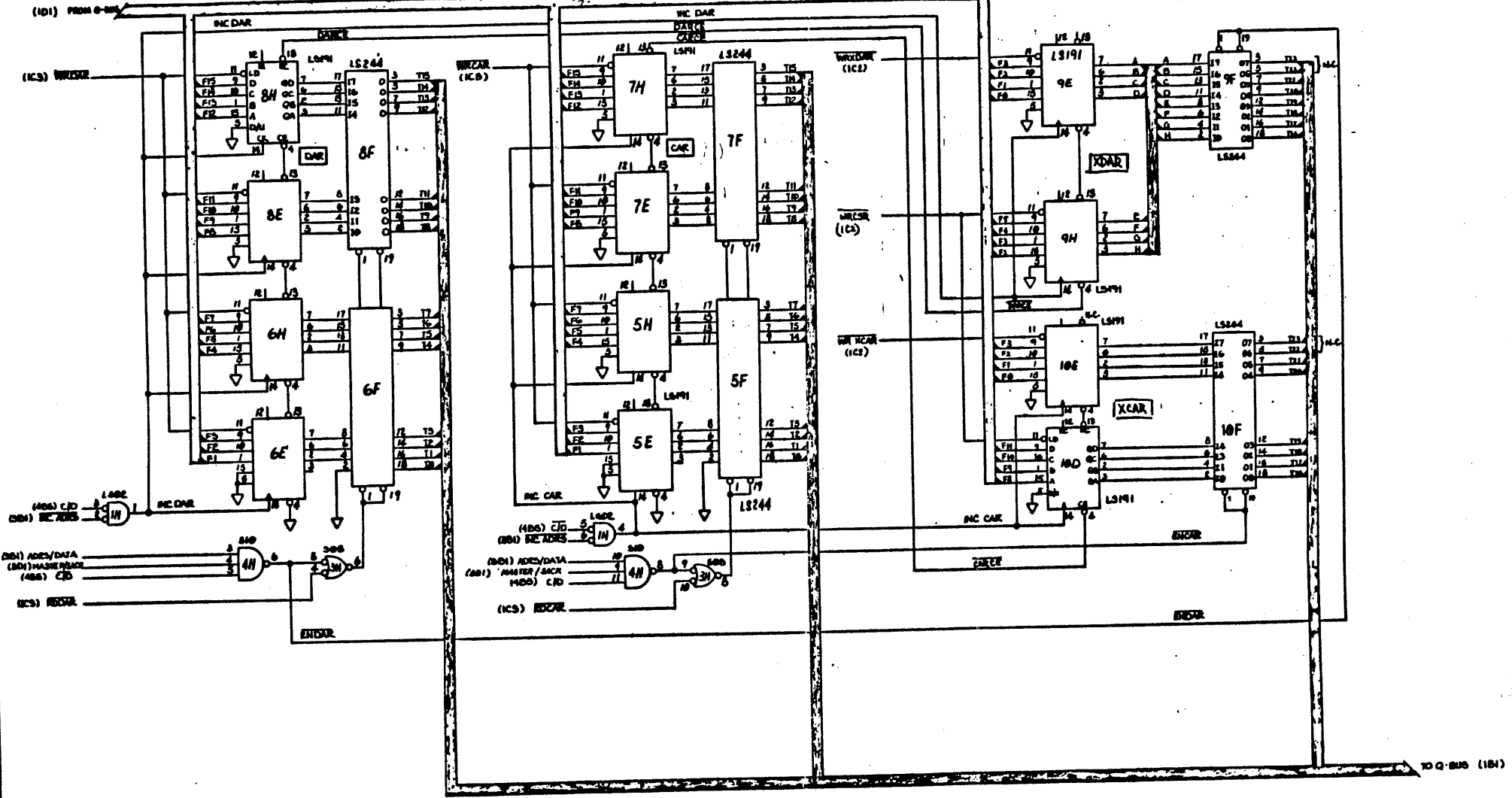
A.3 Drive and Controller Sense Information

Upon the execution of the REQUEST SENSE command, the controller returns 4 bytes of information in the following format. Refer to the section on Drive and Controller Sense in the respective DTC controller specifications for a detailed interpretation of these bytes.




15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Sense Byte 1								Sense Byte 0								XXXXXX
Sense Byte 3								Sense Byte 2								XXXXXX + 2
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

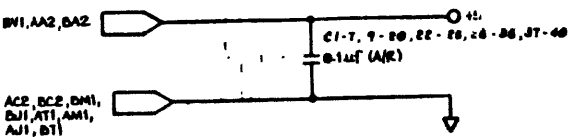
XXXXXX is the octal address that is loaded into the DAR.

Note: Data received from the controller as well as data sent to the controller will be transferred in the above order.



NOTES:

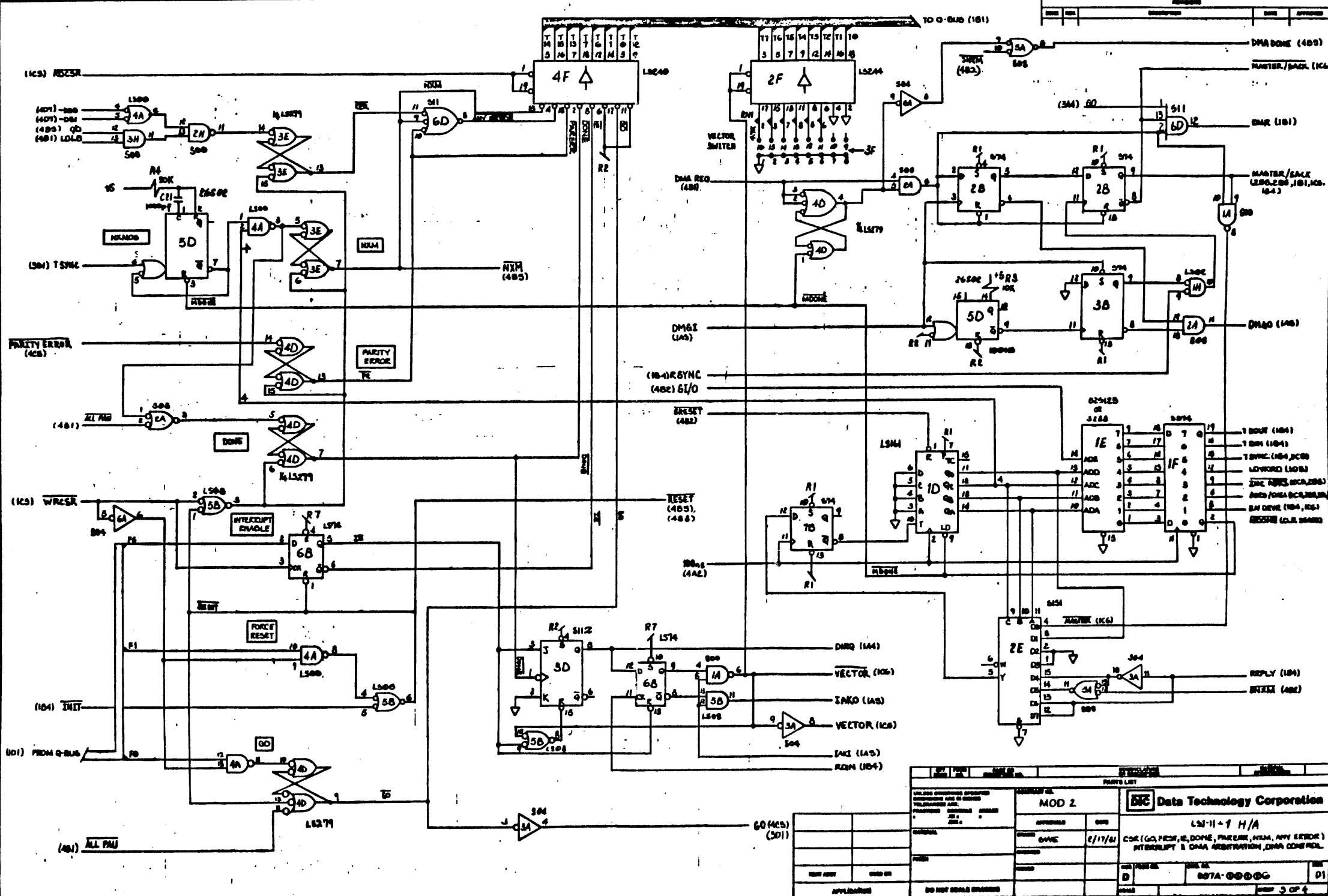
1. IF DISCREET RESISTOR USED, LAW FLAT W/0.4" BENT LEADS.
2.  MAY BE OMITTED.
3.  ONE PER SIGNAL LINE.
4.  ONE PAIR PER SIGNAL EITHER 5M OR DISCREET 5%, 1/4W.



PARTS LIST		REVISIONS	
NO.	DESCRIPTION	DATE	BY

MOD 2 DATE 3/17/81		DTIC Data Technology Corporation LSI-11-1 H/A CAR, DAR, CSR (DARUMA, CARUMA)
PART NO. D	QTY. 00006	

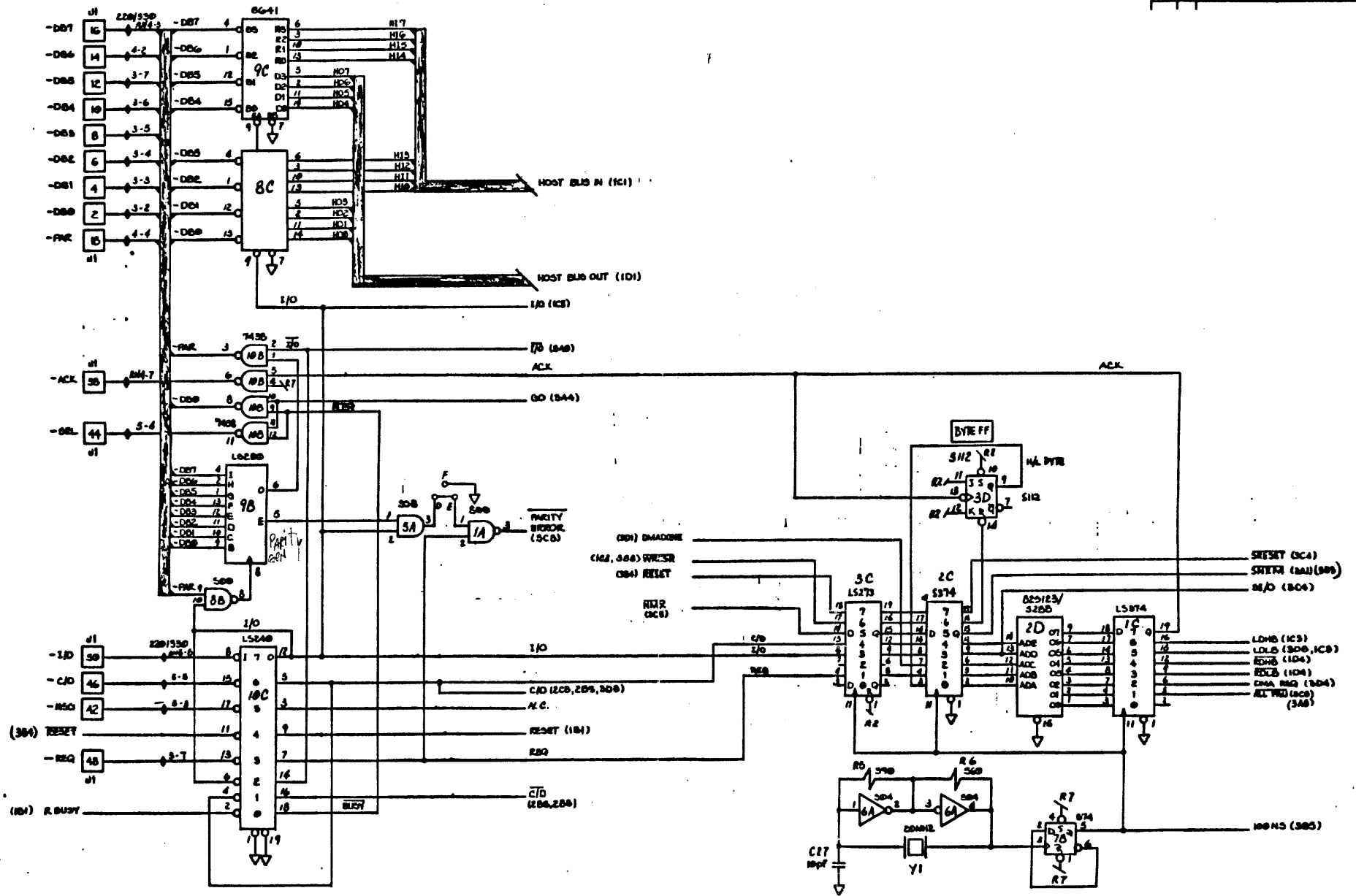
TO Q-BUS (ID1)



PARTS LIST		REVISIONS	
QTY	DESCRIPTION	DATE	BY

MOD 2 APPROVED: [Signature] DATE: 2/17/61		DEC Data Technology Corporation LSI-11-1 H/A CSR (GO, FERR, R, DONE, PARERR, NRM, ANY ERR) & INTERRUPT & DMA ARBITRATION, DMA CONTROL.
PARTS LIST QTY: 1 DESCRIPTION: [Blank] DATE: [Blank] BY: [Blank]		

DESIGNED BY: [Blank] DRAWN BY: [Blank] CHECKED BY: [Blank] DATE: [Blank]	PARTS LIST QTY: 1 DESCRIPTION: [Blank] DATE: [Blank] BY: [Blank]
---	--



31- NI 000 PDMS

PARTS LIST		REVISIONS		DATE	
NO.	DESCRIPTION	BY	DATE	REV.	DATE
1	MOD 2				
Data Technology Corporation 151-11-1 H/A HOST BUS INTERFACE		APPROVED: GWE 8/17/81 DESIGNED: GWE CHECKED: GWE DRAWN: GWE PARTS LIST: GWE			
DO NOT SCALE DIMENSIONS		PART NO. 007A-0000G QTY 4 OF 4			