UC01/L

(RL01/RL02 COMPATIBLE)

UNIVERSAL CONTROLLER

TECHNICAL MANUAL

PRELIMINARY

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Section 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the UC01/L Universal Controller manufactured by Emulex Corporation. This manual also provides diagnostics and application information.

1.2 OVERVIEW

The UC01/L Universal Controller is a single printed circuit board assembly (PCBA) designed to be embedded in a Digital Equipment Corporation (DEC) LSI-11 central processing unit (CPU). The UC01/L controller can be used to interface the LSI-11 CPU with any disk mass-memory peripheral device that uses the Small Computer System Interface (SCSI) based on the ANSC X3T9.2 standard.

1.2.1 UC01/L Emulation of RL01 and RL02

In conjunction with one of several SCSI-compatible disk drives, the UC01/L controller emulates two DEC RLV11 (18-bit address capability) or RLV12 (22-bit address capability) disk controllers and attached RL01 and RL02 disk drives. The UC01/L controller includes a BDV11-Compatible Clock Simulator plus bootstrap programmable read only memories (PROMs), and Q-Bus termination resistors. The UC01/L controller is compatible with all single-ended SCSI devices and and DEC operating systems used on LSI-11 CPUs that support DEC RL01 or RL02 disk subsystems. The UC01/L controller may be configured, by switching, to operate with and map into many different types of SCSI-compatible drives.

1.2.2 UC01/L Configuration

Emulation of the RLV11/RLV12 provides a convenient controller architecture for a wide variety of modern technology disk drives. The RLV11/RLV12 controller emulation is supported by DEC LSI-11 operating systems and is easy to program.

Each controller on the UC01/L controller PCBA can handle up to eight drives. The drives need not be of the same type or manufacture. The UC01/L controller configures each drive from information stored in a configuration PROM. This configuration technique permits up to 64 different switch-selectable combinations of drive arrangements.

1.2.3 SCSI Bus

The SCSI bus interface can accept data rates up to about four megabytes/second, and allows device independence without requiring system hardware or software modification. The SCSI interface uses logical addressing for all command/data structures. All data are addressed as logical blocks up to the maximum number of blocks in a peripheral device; each device can be interrogated to determine how many blocks it contains.

1.3 FEATURES

The UC01/L Universal Controller includes seven features that enhance performance and versatility.

1.3.1 Microprocessor Design

The UC01/L controller design incorporates a unique 8-bit bipolar microprocessor that performs all controller functions. Using the microprocessor reduces the component count, provides high reliability and easy maintainability, and enables a single set of hardware to be adapted to a wide range of emulation capabilities through the flexibility of microprogramming. The Emulex UC01/L Universal Controller achieves functional capability that exceeds performance of emulated DEC controllers by providing enhancement features such as built-in self-test during power-up, built-in disk formatting, and ability to work with drives of various types, sizes and capacities.

1.3.2 Packaging

The UC01/L is constructed on a single, quad-size, multiple-layer printed circuit board assembly (PCBA) which plugs directly into the Q-Bus in the DEC LSI-11 CPU chassis or expansion box. No cabling is required between the CPU and the UC01/L controller. The UC01/L controller obtains its power from the chassis in which it is mounted.

1.3.3 Self Test

The UC01/L controller firmware includes an internal self-test routine which is automatically executed when power is first applied (power-up mode). This self test exercises all parts of the microprocessor, buffer, and storage-device data logic. It does not test all controller circuitry, but successful execution indicates high probability that the controller is operational. If the controller fails the self test, the red FAULT light emitting diode (LED) on the upper edge of the PCBA is lit and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The UC01/L controller contains a 1K x 8-bit high-speed random access memory (RAM) buffer. The RAM buffer is used to temporarily store the contents of the controller's device registers plus a full 512-byte block of data from a selected disk sector. This buffering permits multiple Read operations to be performed with a 1-to-1 data block interlace format. Buffer operations eliminate the possibility of a data-late condition, and permit the controller to be operated at low bus priorities.

1.3.5 Options

Sockets allow insertion of optional 512-word bootstrap PROMs, and Q-Bus termination resistor packs. Dual in-line package (DIP) switch settings allow optional user functions to be selected, and also enable a software-controlled line time clock (LTC). These optional functions are compatible with the functions provided by the BDV11; therefore, no BDV11 module is required in the LSI-11 system that uses the UC01/L controller.

1.3.6 Configuration Switches

DIP switches are provided to configure the UC01/L controller for various device types, sizes and capacities, Q-Bus addresses, and operating characteristics. Up to 64 possible combinations of drive characteristics can be selected for the eight drive devices handled by the UC01/L controller.

1.4 FUNCTIONAL COMPATIBILITY

The UC01/L Universal Controller is compatible with media, address mapping, diagnostics, and operating systems to the extent described in this subsection.

1.4.1 Media Compatibility

Disk packs formatted with the UC01/L controller are not media compatible with other Emulex controllers or with RL01 or RL02 disk drives.

1.4.2 Address Mapping

From one to four logical units may be mapped by the controller on the selected drive. The number of logical units mapped depends on the type, size, and capacity of the drive. Various mapping organizations can be used. Most mapping organizations do not leave direct one-to-one correlation between the logical and physical addresses.

1.4.3 Diagnostics

On LSI-11 CPU systems, the UC01/L controller can run the following diagnostic programs:

- o ZRLGB0 Controller Test No. 1
- o ZRLHB0 Controller Test No. 2
- o ZRLKB1 Performance Exerciser
- o ZRLMB0 Bad Sector File Tool

No modification of any of these diagnostic programs is required.

1.4.4 Operating Systems

The UC01/L controller is compatible with all DEC operating systems used on LSI-11 CPUs that support DEC RL01 or RL02 disk subsystems. No operating system modifications are required. Table 1-1 lists and describes disk subsystem specifications that are compatible with the UC01/L controller.

Table 1-1. RLV11/RL01/RL02 or RLV12/RL01/RL02 Disk Subsystem Specifications

	Characteristics	
Parameter	RL01	RL02
Surfaces/Drive	2	2
MBytes/Logical Unit	10.24	20.48
Blocks/Drive	10,240	20,480
Tracks/Cylinder	2	2
Cylinders/Drive	256	512
Sectors/Track	40	40
Data Bytes/Sector	256	256
Sectors/Data Block	2	2
Drives/Controller, Maximum	4	4

1.5 UC01/L CONTROLLER SPECIFICATIONS

Specifications for the UC01/L Universal Controller are listed and described in Table 1-2.

Table 1-2. UC01/L Controller Specifications

Parameter	Characteristics
FUNCTIONAL	
Emulation	DEC RLV11 and RLV12 controllers and RL01 and RL02 disk drives
Media Format	1:1 or 2:1 sector interlace
Drive Interface	SCSI
Number of Drives	Up to 8
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each physical drive
Tracks/Cylinder	Selectable for each physical drive
Cylinders/Drive	Selectable for each physical drive
Drive Type Code	RL01 or RL02 for each physical drive
Computer Interface	LSI-11 Q-Bus
Vector Address	210 standard, 150 optional
Q-Bus Addresses	Controller registers: 774400-774406 Bootstrap PROM: 773000-773776 and 765000-765776 LTC Register: 777546
Priority Level	Level 5 and 4
Data Buffering	1 Sector (256 words)
Data Transfer	High-speed direct memory access (DMA) operation
Self Test	Extensive internal self-test automatically occurs on power-up sequence
Indicator	Activity/Error/Status LED

Table 1-2. UC01/L Controller Specifications (continued)

Parameter	Characteristics
Options	512 word bootstrap Q-Bus termination BDV11 LTC control 22-bit addressing.
Design	High-speed, bipolar microprocessor that uses 2901 bit-slice components
PHYSICAL	
Mounting	Any LSI-11 Q-Bus quad slot in CPU or expansion box
Connectors	One 50-pin flat-cable connector
ELECTRICAL	
Q-Bus Interface	DEC approved line drivers and receivers
Drive Interface	Differential line drivers and receivers. Cable accumulative length to 35 feet.
Power	+5 Volts (V) ± 5 percent, 5 Amperes (A)

2.1 CONTROLLER ORGANIZATION

The UC01/L controller is organized around an 8-bit, high-speed, bipolar microprocessor. A simplified block diagram of the functional elements in the UC01/L controller is shown in Figure 2-1. The arithmetic logic unit (ALU) and the register file portion of the microprocessor are implemented with two 2901 bit-slice IC components. The microinstruction code is 48 bits long, and the 1024-word control memory is implemented by 12 1K x 4-byte PROMs.

2.1.1 RAM Buffer

The UC01/L controller incorporates a 1K x 8-byte high-speed RAM buffer which temporarily stores (buffers) the contents of the controller's device registers plus one sector or block (512 bytes) of data.

2.1.2 SCSI Bus and Bus Control Circuitry

The SCSI bus interfaces the UC01/L controller with the selected drive device. Signals are supplied at 50-pin connector J1. A simplified diagram of the SCSI bus is shown in Figure 2-2,

The SCSI bus control circuitry establishes the physical path between the initiator and the target, shown in Figure 2-3, and controls all event sequences occurring via the SCSI bus.

Figure 2-1. UC01/L Universal Controller, Simplified Block Diagram

Figure 2-2. SCSI Bus, Simplified Diagram

Figure 2-3. SCSI Bus Physical Path

Serial data bits from the selected drive are converted into eight-bit parallel data characters and transferred to the RAM buffer via the microprocessor. Conversely, parallel bytes accessed from the RAM buffer via the microprocessor are serialized in time with the Servo Clock pulse received from the drive, and sent to the selected drive.

2.1.3 Q-Bus Interface

The Q-Bus interface consists of four circuit board edge connectors:

A, B, C, and D. These connectors use 48 low-level active signal lines. Two of these lines are unidirectional and 46 are bidirectional. The Q-Bus interface is used for programmed input/output (I/O), CPU interrupts, and data transfers.

2.1.4 Microprocessor

The microprocessor responds to all programmed I/O and executes the I/O functions required for the addressed control register. The microprocessor also controls all direct memory access (DMA) operations, and transfers data between the Q-Bus data lines and the RAM buffer.

2.2 PHYSICAL DESCRIPTION

The UC01/L Universal Controller consists of a single quad-sized PCBA which plugs directly into the four Q-Bus connectors in a DEC LSI-11 CPU chassis or expansion box. The UC01/L PCBA is shown in Figure 2-4.

2.2.1 Connectors

In addition to the Q-Bus circuit board edge connectors, which are part of the board substrate, the UC01/L PCBA contains connectors J1, J2, and J3.

2.2.1.1 SCSI Bus Connector

The 50-pin flat cable connector, reference designated J1, at the top center edge of the PCBA is for the SCSI bus cable that interfaces the controller with the first drive device and daisy chains to all drives in the system (up to eight).

2.2.1.2 Test Connectors

Connectors J2 and J3 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

Figure 2-4. UC01/L Universal Controller PCBA, Component Side

2.2.2 Switches

The UC01/L controller contains six DIP switch packs, reference designated SW1, SW2, SW3, SW4, SW5, and SW6. Each switch is so configured that the ON condition of any switch in the pack occurs when the slide is pushed to the right (toward the number side of the switch pack). DIP switch functions are described in Section 3. Functions occur only for switch-ON (closed) condition; for no description, switch is either open or not used.

2.2.3 LED Indicator

There is an LED indicator mounted between switches SW1 and SW3 at the upper-right edge of the board, as viewed from the component side. The LED indicates operating conditions that may have several causes:

a. When the controller is reset (SW1.1 ON), or if a Power-Up sequence occurs on the system in which the controller is installed, the controller performs a self test of its internal logic. The self test takes only a fraction of a second, but during self testing the LED is lit. The LED is extinguished after the self test is completed.

b. If self test fails, the LED remains continuously lit and the controller registers remain inaccessible. The controller must be removed and replaced or repaired before the system can be functional.

c. If no drive is attached to the SCSI bus, or if a drive attached to the SCSI bus fails to respond to status polling, the LED blinks ON and OFF with a period of approximately one second. The LED remains extinguished as long as drive(s) attached to the SCSI bus respond to status polling.

NOTE

The UC01/L controller continuously polls drives assigned to it to determine drive status at all times.

d. The LED illuminates during data transfers to and from any drive. This LED illumination provides a visual indication of system activity.

2.2.4 Firmware PROMs

The control memory uses 12 PROM sockets for insertion of PROM ICs. The PROM sockets are located along the left edge of the circuit board, as viewed from the component side. The PROM sockets are labled PROM0 through PROM11 in a discontinuous physical order. The

number on the top of each PROM IC is an Emulex part number which identifies the unique program pattern of the PROM. The PROMs are used to emulate specific DEC equipment functions. When inserting PROMs in sockets, the ID numbers on the top of the PROMs must be in the same sequence as the PROM numbers on the circuit board beside each respective socket; e.g., ID 9 must be inserted in PROM 9.

2.2.5 Bootstrap PROMs

Two PROM sockets are provided for installation of optional Bootstrap PROMs. Socket U101 receives P/N 014x and socket U103 receives P/N 015x. These sockets are in middle of second row of ICs (from bottom).

2.2.6 Configuration PROM

PROM configuration is determined by installing the proper Configuration PROM in socket U64 (next to SW4 in right-center of circuit board).

2.2.7 Address PROM

Header addressing is determined by the configuration of the Address PROM. The Address PROM is installed in PROM socket U104. This socket is near middle of second row of ICs (from bottom) next to switch SW5.

2.2.8 22-Bit Addressing

Socket U126 (bottom row below switch SW5) is available for installation of a 2908 IC if 22-bit addressing is required by the system. when this IC is installed, switch SW2.7 must be set to the ON position (see Section 3).

2.3 INTERFACES

The UC01/L controller interfaces with selected disk drive or tape drive via the SCSI bus flat cable and 50-pin connector J1. It interfaces with the LSI-11 CPU via the Q-Bus.

2.3.1 SCSI Bus Interface

The SCSI bus consists of a flat cable with a 50-pin flat-cable connector that is daisy chained to all drives and terminated at the last drive in the daisy chain. The SCSI bus is shown in Figures 2-2 and 2-3, and interface pin assignments for the nine control signals and nine data signals (including parity) are listed in Table 2-1.

Table 2-1. SCSI Bus Device Interface Pin Assignments

Signal		Name	J1 Pin Number
DB0	L	Data Bus Bit 0	2
DB1	L	Data Bus Bit 1	4
DB2	L	Data Bus Bit 2	6
DB3	L	Data Bus Bit 3	8
DB4	L	Data Bus Bit 4	10
DB5	L	Data Bus Bit 5	12
DB6	L	Data Bus Bit 6	14
DB7	L	Data Bus Bit 7	16
DBP	L	Data Bus Bit Parity	18
GROUND			20
GROUND			22
GROUND			24
+5V		Termination Power	26
GROUND			28
GROUND			30
ATN	L	Attention	32
GROUND			34
BSY	L	Busy	36
ACK	L	Acknowledge	38
RST	L	Reset	40
MSG	L	Message	42
SEL	L	Select	44
C/D	L/H	Command (L)/Data (H)	46
REQ	L	Request	48
I/O	L/H	Input (L)/Output (H)	50

All odd-numbered pins are connected to ground.
DB7 (L) is most significant bit (MSB) and
DB0 is least significant bit (LSB).

The SCSI bus transfers parallel information between the initiator and the target (see Figure 2-3). It is designed for intelligent peripheral devices.

The SCSI bus is capable of operating in eight distinct phases, but in only one phase at a time. The SCSI bus phases are listed and briefly described in Table 2-2. For further information about the SCSI bus, see publication ANSC X3T9.2/82-2, REV. 6 (14 February 83).

Table 2-2. SCSI Bus Phases

Phase	Description
CONTROL	
Bus Free	Indicates no SCSI device is using the bus and that the SCSI bus is available for use. Created by passive release of all SCSI bus signal lines.
Arbitration	Allows one SCSI device to control SCSI bus.
Selection	Allows initiator to select target for reading or writing of data. I/O signal line not asserted.
Reselection	Allows target to reconnect to an initiator. Arbitration must first be in effect.
INFORMATION TRANSFER	
Command	Allows initiator to command target.
Data	Allows Read or Write operations to be performed.
Status	Allows initiator to receive target status information.
Message	Allows initiator and target to exchange messages.

When the SCSI bus is between two phases, the bus signals are restricted by the following limitations:

a. The BSY, SEL, REQ, and ACK signals cannot change.

b. The C/D, I/O, MSG, and DATA signals may change.

c. The ATN and RST signals may change if certain ATTENTION and RESET conditions are met.

2.3.2 Q-Bus Interface

The LSI-11 Q-Bus has 42 bidirectional and two unidirectional signal lines on connectors A and B, and two unidirectional signal lines on

connector C. Q-Bus interface pin assignments are listed and described in Table 2-3. The CPU, memory and I/O devices use these lines for control, data, and address information. The Q-Bus interface lines are grouped in the following categories:

a. Twenty-two data/address lines - <BDAL00:BDAL21>. The four data/address lines which carry the most significant bits (MSB) are lines BDAL21:BDAL18. They are used for addressing only and do not carry data. Lines BDAL17 and BDAL16 reflect the parity status of the 16-bit data word during a Write or Read data transfer operation via the Q-Bus cycle.

b. Six data transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, and BWTBT.

c. Six direct memory access (DMA) control lines - BDMR, BSACK, BDMGI (connectors A and C), and BDMGO (connectors A and C).

d. Seven interrupt control lines - BEVNT, BIAKI, BIAKO, BIRQ4, BIRQ5, BIRQ6, and BIRQ7.

e. Five system control lines - BDCOK, BHALT, BINIT, BPOK, and BREF.

Table 2-3. Q-Bus Interface Pin Assignments

	Connector A Signal		Connector B Signal	
Pin	Component Side	Solder Side	Component Side	Solder Side
A	BIRQ5	+5V	BDCOK	+5V
B	BIRQ6		BPOK	
C	BDAL16	0V (GND)	BDAL18	0V (GND)
D	BDAL17		BDAL19	
E		BDOUT	BDAL20	BDAL02
F		BRPLY	BDAL21	BDAL03
H		BDIN		BDAL04
J	0V (GND)	BSYNC	0V (GND)	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	0V (GND)	BIAKI	0V (GND)	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVNT	BDAL11
S		BDMGO		BDAL12
T	0V (GND)	BINIT	0V (GND)	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

Table 2-3. Q-Bus Interface Pin Assignments (Continued)

	Connector C Signal		Connector D Signal	
Pin	Component Side	Solder Side	Component Side	Solder Side
A		+5V		+5V
B				
C		0V (GND)		0V (GND)
D				
E				
F				
H				
J	0V (GND)		0V (GND)	
K				
L				
M	0V (GND)	BIAKI	0V (GND)	
N		BIAKO		
P				
R		BDMGI		
S		BDMGO		
T	0V (GND)		0V (GND)	
U				
V				

All signals, except BDCOK and BPOK, are low active.

2.3.2.1 Interrupt Priority Level

The UC01/L controller is hardwired to issue level-4 and level-5 interrupt requests. The level-4 interrupt request line is needed for compatibility with either an LSI-11 or LSI-11/2 CPU.

2.3.2.2 Register Address

The register address and the number of registers assigned to the UC01/L controller are decoded by the Address PROM, installed in PROM socket U104 (see paragraph 2.2.7). The available user-selectable options are determined by the settings of configuration DIP switch SW1 (see Section 3).

2.3.2.3 DCOK and INIT Signals

The DCOK and INIT signals can each individually perform Controller Clear operation. The Self-Test function is performed only when DC power is initially applied (Power-Up mode).

2.4 LOGICAL DISK FORMAT

The logical disk format involves mapping the system in such a way that the software corresponds with logical addresses on physical devices.

To the system software, the UC01/L controller/drive subsystem appears to be formatted exactly as an RL01 or RL02 drive. Actually, the controller firmware multiplies the cylinder, track, and sector components of a standard disk drive header address to obtain a numerically sequenced block address (same as a 512-byte sector on a disk drive), so that the UC01/L controller can operate drives in any combination by merely addressing sequential data block numbers. The possinbility of a 1:1 correspondence between a logical address and a physical address is extremely unlikely.

The LSI-11 Q-Bus has two card slots that can be used to interface with one DEC RLV11 or RLV12 controller or with two Emulex UC01/L controllers. One RLV11 controller (18-bit address capability) can control up to four RL01 drives, each of which has 10.24 megabytes of storage, or up to four RL02 drives, each of which has 20.48 megabytes of storage. One RLV12 controller can control the same number and types of drives, except it has 22-bit address capability; therefore, both the RLV11 and RLV12 controllers are capable of interfacing with peripheral devices that can provide up to 81.92 megabytes of storage.

The Emulex UC01/L controller is equivalent to two RLV11 or RLV12 controllers. When two UC01/L controllers are installed in the Q-Bus, the CPU detects the same interface as it would experience with four RLV11 or RLV12 controllers. Since each UC01/L controller can control up to eight RL01- or RL02-type drives, two UC01/L controllers can control up to 16 RL01- or RL02-type drives that provide 327.68 megabytes of storage. Thus, the Emulex system supports up to four times the storage capacity as the DEC system can support in the same allotted Q-Bus interface.

2.4.1 Media Organization

Formatting a disk pack and mapping one or more logical drive units onto a physical disk drive is rather complicated and varies with disk drive capacity. Some of the disk formatting information is supplied by the configuration PROM (IC socket U64, see paragraph 2.2.6). In all applications, however, the headers actually written on the disk drives are not standard RL01 or RL02 headers. A one-to-one or two-to-one sector interleave is also generated for disk drives by the hardware formatter. A two-to-one sector interleave is used when the physical disk drive has 23 or fewer sectors/track; otherwise, a one-to-one interleave is used. Disk packs that are formatted with a UC01/L controller are not media compatible with RL01 or RL02 disk packs, nor with other Emulex controllers.

2.4.2 Mapping

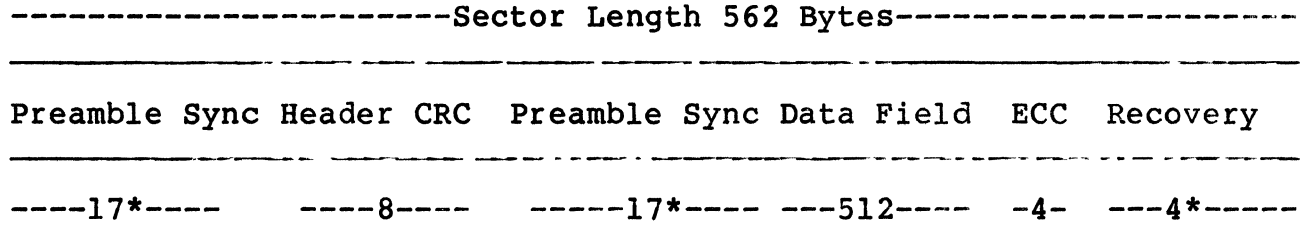
Depending on the type and capacity of the media, up to eight logical units may be mapped on the physical drive. The UC01/L controller can control a maximum of eight logical drive units distributed on up to, but not more than eight physical disk drives.

NOTE

A logical drive unit may not be mapped across a physical drive unit boundary.

2.4.3 Sector or Data Block Format

Each sector or data block contains a detached two-word header and a 256-word data field. The header field is terminated with two vertical check characters and the data field is terminated with a 32-bit ECC. The controller attempts corrections only on the data field, never on the header. Each field is preceded by at least 11 bytes of zeros and an eight-bit SYNC byte. Each sector is organized as shown in Figure 2-5.



*Values shown are minimums which apply to most Winchester-type units; however, these values may vary to accommodate different physical drive types and are determined by configuration PROM data.

Figure 2-5. Sector or Data Block Format

2.4.3.1 Header Format

The header is the address of a 512-byte block of storage in the peripheral device. System software can read the logical header by issuing a Read Header command. Headers are not actually read from the disk or tape media, but are generated by the firmware in the controller according to the logical position relationship of the head(s) and media.

The header preamble is used to synchronize the Phase Locked Oscillator (PLO) in the drive to the data on the media. The SYNC byte is used by the controller to synchronize with the data bytes and their boundaries, and by the drive to synchronize with the phase of the data. The logical header format is shown in Figure 2-6. For the physical header format word organization, the user should see the SCSI interface manual because the word organization structure is different for the header and data fields of each command or function.

Header Word 1:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Cylinder Address								HS		Sector Address					

Header Word 2:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Zeros															

Header Word 3:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CRC															

Figure 2-6. Logical Header Format

2.4.3.2 Data Field

The preamble and SYNC bytes for the data field have the same functions as the preamble and SYNC bytes for the header. The data field itself is always 512 bytes (256 words) long. During a Write operation, any unused portion of the data field is finished and terminated with all-zeros bytes.

2.4.3.3 Postamble

The postamble at the end of each data field not only separates data blocks, but also provides time for the system to turn off the Write amplifiers, turn on the Read amplifiers, and thus switch from Write mode to Read mode. Write splices can sometimes be allowed to exist in any postamble area. On drives that contain removable media, the Sector pulse postamble may also include a recovery area required to allow time to realign head scattering within proper tolerances.

Section 3
INSTALLATION

3.1 INTRODUCTION

This section describes the step-by-step procedure for installation of the UC01/L Universal Controller in an LSI-11 system. The following list is an outline of the procedure. Each step in the list correlates to a second-level heading in this section; i.e., item 1, Inspect the UC01/L, procedure is described in paragraph 3.2.

1. Inspect the UC01/L
2. Prepare the SCSI controller
3. Prepare the drives
4. Prepare the LSI-11
5. Configure the UC01/L
6. Install the UC01/L
7. Route the drive I/O cables
8. Run the diagnostics.

3.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the UC01/L controller, visually inspect the entire assembly for bent or broken connector pins, damaged components, or other visual evidence of physical damage. The PROMs should be carefully examined to ensure each is firmly and completely seated in its socket. Verify that controller model or part number designation, revision level, and serial number agree with those on shipping invoice. This verification is important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

3.3 SCSI CONTROLLER PREPARATION

Unpack, inspect, and install the SCSI controllers as instructed by manufacturers. These controllers interface the SCSI bus with the drives as shown in Figure 3-1.

Figure 3-1. SCSI Bus System Components, Simplified

3.4 DRIVE PREPARATION

Unpack, inspect, and install system disk drives or tape drives as instructed by manufacturers. Position and level them in their final places before beginning the UC01/L controller installation. This positioning enables needed length and routing of system I/O cables to accurately determined. To simplify daisy-chain cable installation, drives should be immediately adjacent to each other; side-by-side, or stacked in standard EIA or RETMA equipment racks.

3.4.1 Unit Addressing

Each drive interfaced with a logical controller should be equipped with an ID plug or equivalent unit selection arrangement such as logic circuitry or select switches, ranging from binary 0 to 7. It is important that no two drives, interfacing with a logical controller, have the same unit select number. See the drive manufacturer's manual for further unit select details.

3.4.2 Data Block Addressing

A data block on a disk drive is equivalent to a sector on a disk drive. All addressing is made to data blocks (not sectors) which are numbered in sequence on an addressed drive device. The user is not concerned with data block address computation because the conversion is automatically made by the microprocessor circuitry in the UC01/L controller. For correct data block count settings, see Configuration Selection in Appendix A. The exact method different drive manufacturers use to determine a data block (or sector) count may differ. For corrrect procedure, see manufacturer's manual.

3.5 CPU PREPARATION

To install the UC01/L controller and associated drives, the interior of the LSI-11 CPU must be made accessible to the installer. Use the following procedures:

a. Power down system and place main AC circuit breaker at rear of cabinet in OFF position. Verify AC POWER indicator remains lit.

b. Slide CPU out of cabinet and remove top cover.

c. Tilt card cage up. Access to card-cage conectors, CPU interior, and other modules should be available.

3.6 UC01 CONTROLLER CONFIGURATION

Controller configuration must be established before it is installed on the Q-Bus in the LSI-11 CPU chassis. Configuration setup is made by setting switches in DIP switch packs SW1, SW2, SW4, SW5, and SW6. DIP switch functions are listed and described in applicable tables in this section.

3.6.1 Controller Address Selection

All Q-Bus controllers have a block of several command and status registers throOugh which the LSI-11 system can command and monitor the controller. These registers are sequentially addressed, beginning with a starting address assigned to the particular controller; i.e., the UC01/L Universal Controller.

DIP switch pack SW6 is used to select the starting address to which each emulated controller is to respond. Each of the two emulated controllers on the UC01/L controller PCBA can be addressed at any of three addresses, but only one address should be made available for each emulated controller at any time. Only one switch in the SW6 DIP switch pack should be closed for each emulated controller on the UC01/L controller PCBA. At least one switch of the three select switches for each emulated controller must be closed to obtain emulated controller response. Table 3-1 lists the starting addresses that can be selected by the switches in DIP switch pack SW6.

Table 3-1. Controller Address Selection

Switch	Function Description
SW6.1	Selects standard controller number 0 address 774400
SW6.2	Selects alternate controller number 0 address 776700
SW6.3	Selects alternate controller number 0 address 776300
SW6.4	Selects standard controller number 1 address 777340
SW6.5	Selects alternate controller number 1 address 776720
SW6.6	Selects alternate controller number 1 address 776320
Closed position = selected, open position = not selected	

The starting address for the UC01/L controller's Q-Bus registers is selected by DIP switch SW6.n (see Table 3-1). For example, the normal starting address of 774400 for emulated controller number zero is obtained by placing switch SW6.1 in the ON position. Alternate starting addresses of 776700 or 776300 are obtained by setting switch SW6.2 or SW6.3 ON, respectively. The starting addresses for emulated controller number one are 777340, 776720, and 776320, which are set by switches SW6.4, SW6.5, and SW6.6, respectively. Only one switch must be ON for each emulated controller; i.e., DO NOT set switches SW6.4 and SW6.5 ON at the same time, but switches SW6.3 and SW6.4 can be ON at the same time because they affect different emulated controllers. UC01/L controller component locations are shown in Figure 3-2.

3.6.2 Interrupt Vector Address

Two switches in DIP switch pack SW2 are used to select the vector address for each of the two emulated controllers on the UC01/L controller PCBA. These switches and their functions are listed and described in Table 3-2.

Table 3-2. Interrupt Vector Address Selection

Switch	Function Description
SW2.1	Selects interrupt vector address for emulated controller number 0 Open = standard vector address of 160 selected Closed = alternate vector address of 370 selected
SW2.2	Selects interrupt vector address for emulated controller number 1 Open = standard vector address of 214 selected Closed = alternate vector address of 374 selected

Figure 3-2. UC01/L Controller Component Locations

3.6.3 Drive Configuration Selection

The phrase "Drive Configuration Selection" means the process by which the UC01/L controller can be configured to use a particular type of physical drive in performing the RL01 or RL02 emulation. That is, a particular set of physical drives is available and the UC01/L controller must be made aware of what type(s) of physical drives is or are to be used in the system. In the UC01/L controller, DIP switches SW1.1 through SW6.6 are used for that purpose. Configuration PROMs are used in conjunction with certain switches in DIP switch packs SW2 and SW4. These switches and their functions are listed and described in Table 3-3.

Table 3-3. Drive Configuration PROM Address Selection Switches

Switch	Function Description
SW2.8	Must be closed. Provides LSB of configuration PROM selection. Used with SW4.1 through SW4.7 closed.
SW4.1 through SW4.7	Must be closed. Used with SW2.8 closed. SW4.7 provides MSB of configuration PROM selection. SW4.1 through SW4.6 provide remainder of configuration PROM selection address pointer bits.

The configuration PROM contains blocks of instructions for configuring the emulation of each emulated controller on the UC01/L controller PCBA and the SCSI controllers with associated disk drives. The configuration PROM address selected by the configuration select switches in Table 3-3 contains a microcode which determines the following elements:

a. SCSI controller (disk formatter) address
b. Disk drive address
c. Disk drive type - RL01 or RL02
d. Disk drive capacity (number of data blocks)
e. SCSI data block size (optional).

For any other configuration PROM address selected, a different configuration microcode would be produced to accommodate the different system components. Any of the configuration PROM address selection switches could be placed in the closed (ON) or open (OFF) position so that up to 256 different configuration microcodes that could be stored in the configuration PROM could be pointed to and selected. At the present design stage, only one configuration microcode has been stored in the configuration PROM; therefore, only one configuration PROM address is selectable by the configuration PROM address selection switches. That address is the one in which all eight of the switches are closed, as described in Table 3-3. As more configurations are developed, additional switch settings can be added and placed in Table A-2 of Appendix A. The potential complexity of system configuration development is shown in Figure 3-3.

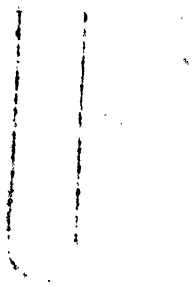


Figure 3-3. UC01/L Configurations

3.6.4 SCSI Device Address

Switches SW1.6, SW1.7, and SW1.8 are used to select any one of eight possible SCSI bus addresses that the UC01/L controller is to use to establish its identity in the system.

SW1.6 = SCSI device address bit 2 (MSB)
SW1.7 = SCSI device address bit 1
SW1.8 = SCSI device address bit 0

Available SCSI device address identities are listed and described in Table 3-4.

Table 3-4. SCSI Device Address Selection Switches

Switch SW1.6 Bit 2	Switch SW1.7 Bit 1	Switch SW1.8 Bit 0	SCSI Device Address Number
O	O	O	00
O	O	C	01
O	C	O	02
O	C	C	03
C	O	O	04
C	O	C	05
C	C	O	06
C	C	C	07

3.6.5 Selection of Miscellaneous Switchable Operating Functions

This subsection has so far described functions in which the states of two or more DIP switches are coordinated to select or produce a desired condition. Most of the DIP switches are used alone to select, enable, or disable some controller, bus, or disk drive function or emulation. Some of the available DIP switches are not used or have not yet been assigned discrete functions. The remaining DIP switches are listed and described in Table 3-5. Functions are described in a positive format; i.e., to cause the function to happen, the closed (ON) condition is implied, unless otherwise specified.

Table 3-5. Unassisted DIP Switch Functions

Switch	Function Description
SW1.1	When closed, resets all UC01/L controller hardware and firmware. In the Reset condition, the contents of all registers and counters in the UC01/L controller are initialized. While the Reset function is being performed, the internal microprocessor in the UC01/L controller does not function, so the UC01/L controller does not function. Momentarily closing, then opening, the SW1.1 switch to establish Reset conditions always causes

Table 3-5. Unassisted DIP Switch Functions (continued)

Switch	Function Description
SW1.1 (cont'd)	the self-test function to be performed by the UC01/L controller as soon as the Reset operation is finished (see paragraph 2.2.3, cause a). The Reset feature is normally used only during servicing to clear and initialize the UC01/L controller after a major malfunction of the UC01/L controller.
SW1.2	Not used.
SW1.3	Not used.
SW1.4	Normally open. Closed only during servicing of the UC01/L controller. When closed, causes the UC01/L controller to automatically perform Seek operations, during execution of Write or Read commands, by using logical header address data to identify cylinder and track. This function is especially useful when hand-loading Write or Read commands because it saves time and eliminates need for user to issue Read Header and Seek commands separately.
SW1.5	When closed, Write Locks all drives at power-up. Write Lock prevents previously written data on drive media from being written over and lost. Although this Write Lock feature protects and preserves valuable data, the drives in the system become Read-only devices and cannot be written to or edited. In effect, the drives are then a storage library that is not likely to need changing or updating. To retain Write/Read capability on one or more drives in the system, SW1.5 should remain open and the extended Write Switch Register command (function code 0) should be used to Write Lock specific drives only (see paragraph 5.3.1 and Figure 5-1). Alternatively, switch SW1.5 can be left closed at power-up and after. Then Write Lock on system drives could be disabled, as required, by using the extended Write Switch Register command to leave only specific drives in system in the Write Locked condition.
SW2.3	Not used.
SW2.4	Normally open. When closed, causes UC01/L controller to change drive selection time-out period on SCSI bus from normal 250 microseconds to 250 milliseconds. This drive selection time-out period is the maximum time the UC01/L controller is able to wait for a response when attempting to select a physical disk drive. When SW2.4 is open, the UC01/L controller uses 250 microseconds for the drive selection time-out period.

Table 3-5. Unassisted DIP Switch Functions (continued)

Switch	Function Description
SW2.4 (cont'd)	This switch is useful when servicing the UC01/L controller and should NOT be left closed during normal operation, because the longer drive selection time-out period would seriously degrade system operation.
SW2.5	Must be open at ALL times.
SW2.6	Normally open. When closed, the arbitration sequence that is normally performed automatically by the UC01/L controller is disabled. SW2.6 may be used in future configurations to accommodate SCSI controllers (disk formatters) that are NOT compatible with all of the SCSI bus requirements.
SW2.7	When closed, causes each of the two controllers on the UC01/L PCBA to emulate a DEC RLV12 controller that has 22-bit addressing capability. To function on 22-bit bus, insert an AMD2908 IC in IC socket U126 to provide the line drivers for four more address lines. The 22-bit addressing provides DEC LSI-11/23 and LSI-11/23 PLUS CPUs with access to four megabytes of memory storage capacity. Switch SW2.7 should be open when UC01/L controller is to be used in system that emulates the DEC RLV11 controller (18-bit addressing) and when the UC01/L controller is installed in LSI-11 CPUs that are not LSI-11/23 or LSI-11/23 PLUS models.
SW3.1 Through SW3.8	(Not yet assigned any functions)
SW4.8	Normally open. If closed, the time duration of the SCSI Reset pulse that is generated by the UC01/L controller is changed from the normal 25 microseconds to less than 10 microseconds. SW4.8 may be used in future configurations to accommodate SCSI controllers (disk formatters) that are NOT compatible with all of the SCSI bus requirements. For the present configuration, closing SW4.8 would seriously impair proper operation of the UC01/L controller.
SW4.9	When closed, enables Line Time Clock (LTC) option (address 777546). The LTC option allows program control of the LTC function, and is enabled when DIP switch SW4.9 is ON. Programming instructions for this option are included in paragraph 4.3.2.

Table 3-5. Unassisted DIP Switch Configurations (continued)

Switch	Function Description
SW4.9	Before the LTC can be used, the CPU must be configured to
(cont'd)	enable that feature. On the LSI-11 CPU and LSI-11/02 CPU, remove jumper W3 (BEVNT Line Enable). On the LSI-11/23 CPU, remove jumper W4 (BEVNT Line Enable). The LTC switch on the CPU front panel must also be set in the ON position.
SW4.9 (cont'd)	When using the UC01/L controller with the RSTS operating system, the LTC option must be OFF (SW4.9 open). The CPU, however, should always be configured to enable the LTC option.
SW4.10	When closed, disables bootstrap PROM (address 765000 or 773000). Address 765000 is automatic bootstrap start address which tries all devices. Address 773000 interrogates for bootstrap device address via CRT. The UC01/L controller responds to the bootstrap addresses whether or not the bootstrap PROMs are installed in the IC sockets U101 and U103 on the UC01/L controller. Closing SW4.10 prevents the UC01/L controller from responding to bootstrap addresses; therefore, bootstrap programs, routines, and/or sequences contained in the UC01/L controller can be bypassed by the user so that other bootstrap programs in other system components, which may have the same bootstrap program addresses, can be accessed as required. Bootstrap PROM options are fully explained in paragraph 3.6.6.3 and the bootstrap program routines are detailed in paragraph 4.3.1.
SW5.1	When closed, causes the UC01/L controller to perform parity checks on data lines of the SCSI bus and to abort operations in which parity errors are found. This switch should be used to automatically check parity on SCSI bus for better data integrity. It should not be used if the device on the SCSI bus does not generate a parity bit. For devices that generate parity bit, when this switch is closed and a parity error is found, the parity error is reported as either a hard data error or as an OPI error. Although the operation is automatically aborted, because such errors are non-recoverable errors, it can be retried.

Table 3-5. Unassisted DIP Switch Configurations (continued)

Switch	Function Description
SW5.2	Not used.
SW5.3	Must ALWAYS be open for proper operation of UC01/L controller.
SW5.4	Must ALWAYS be closed for proper operation of UC01/L controller.
SW5.5	Not used.
SW5.6	Must ALWAYS be open for proper operation of UC01/L controller.

3.6.6 Option Installation

There are a number of other UC01/L controller options that can be selected by the user. They are placed in effect by physically installing the option on the PCBA, or by setting the appropriate DIP switches.

CAUTION

Some manufacturers of Q-Bus backplanes omit 22-bit addressing capability and use the four lines that would be assigned for such addressing as power lines. In such systems, the 2908 IC should not be installed in IC socket U126 because that IC and possibly other circuitry would be destroyed by heat. Also if the UC01/L controller is to be used as Q-Bus terminator in a system that has power connected to lines BDAL18 through BDAL21, pins 1, 4, 5, and 14 should be cut in the terminator resistance pack installed in IC socket U128. Cutting these pins prevents excessive power dissipation.

3.6.6.1 Q-Bus Termination Option

The UC01/L controller fits into any Q-Bus backplane card slot. If the UC01/L controller is to be used as the Q-Bus terminator, it must be installed in the last quad slot on the Q-Bus. To prepare the UC01/L controller for system termination, install the termination-resistor packs in IC sockets U122, U128, and U124. In these packs, 180 Ohms is connected to +5 Volts and 390 Ohms is connected to ground on each Q-Bus line.

These three resistor networks may be ordered from Emulex, or the user may use equivalent terminating resistance networks such as BOURNS P/N 761-5-R181/391.

C A U T I O N

Some manufacturers of a Q-Bus backplanes omit 22-bit addressing capability and use the four lines that would be assigned for such addressing as power lines. In such systems, the 2908 IC should not be installed in IC socket U126 because that IC and possibly other circuitry would be destroyed by heat. Also if the UC01/L controller is to be used as Q-Bus terminator in a system that has power connected to lines BDAL 18 through BDAL 21, pins 1, 4, 5 and 14 should be cut in the terminator resistance pack installed in IC socket U128. Cutting these pins prevents excessive power dissipation.

3.6.6.2 Twentytwo-Bit Memory Addressing Option

The UC01/L controller can include the 22-bit memory addressing option. The option kit is Emulex P/N SC0213102, which consists of a single AMD 2908 IC installed in socket U126. Programming instructions for this option are included in Section 4.

3.6.6.3 Bootstrap PROM Options

These options are firmware routines that load the sytem memory with software that is stored on the disk. The routines are executed by the LSI-11, LSI-11/02 or LSI-11/23 CPUs. The option kit is Emulex P/N SC021301, which consists of two PROMs. The PROM labeled 015x is installed in IC socket U101, and the PROM labled 014x is installed in IC socket U103. Programming instructions for these options are included in Section 4.

The Bootstrap option has two sections, Standard Console Bootstrap Routine, and Automatic Bootstrap Sequence (Auto-Boot). The Standard Console Boostrap Routine is entered by the CPU at address 773000, DEC's conventional starting address. The Auto-Boot Sequence is entered at address 765000.

The LSI-11 and LSI-11/02 both require that Power-Up Mode 2 be selected to take advantage of the Standard Console Bootstrap Routine option. This selection is done by installing jumper W6 and removing jumper W5 on the CPU PCBA. The configuration for both the LSI-11 and the LSI-11/02 is the same. The Auto-Boot Sequence option is not available for these LSI-11 or LSI-11/02 units.

The LSI-11/23 may be configured to take advantage of either the Standard Console Bootstrap routine or the Auto-Boot routines. This CPU also requires that power-up Mode 2 be selected (install jumper W6 and remove jumper W5 on the CPU PCBA). The bootstrap starting address, however, is selected by using jumpers W8 through W15. To select the Standard Console Bootstrap routine, install W8. This jumper causes the microprocessor to default to starting address 773000. To use the Auto-Boot option, remove jumper W8, W10 and W12; then install jumpers W9, W11, W13, W14 and W15.

3.6.6.4 Line Time Clock Option

The Line Time Clock (LTC) option allows program control of the LTC function. This control is enabled by setting DIP switch SW4.9 ON. Programming instructions for this option are included in Section 4.

Before the LTC can be used, the CPU must be configured to enable that feature. On the LSI-11 CPU and LSI-11/02 CPU, remove jumper W3 (BEVNT Line Enable). On the LSI-11/23 CPU, remove jumper W4 (BEVNT Line Enable). The LTC switch on the CPU front panel must also be set to the ON position.

When using the UC01/L controller with the RSTS operating system, the LTC option must be off (SW4.9 open). The CPU, however, should always be configured to enable the LTC option.

3.7 CONTROLLER INSTALLATION

The UC01/L controller can fit into any Q-Bus quad slot on the LSI-11 backplane. If the resistor networks of the Q-Bus Termination option are installed (see paragraph 3.6.6.1), the UC01/L controller should be installed in the quad slot which is to provide termination at the end of the Q-Bus; i.e., in the last quad slot of the Q-Bus that is furthest from the first quad slot in the Q-Bus.

If the Q-Bus Termination option is not installed, the UC01/L controller may be assigned to any desired quad slot, because it uses the LSI-11 four-level interrupt scheme that performs distributed interrupt arbitration.

C A U T I O N

To avoid potential circuit damage, always turn computer power OFF before installing or removing any PCBA.

The UC01/L controller should be plugged into the selected Q-Bus quad slot with the component side facing in the same direction as the CPU and other system modules. Verify the PCBA is in the throat

of the connector before attempting to firmly seat it in the connector. When properly aligned in connector, press extractor handles on each upper corner to firmly seat.

3.7.1 Cabling

Typical subsystem cabling for the controller and drives is shown in Figure 3-4.

Figure 3-4. System Daisy-Chain Cabling

The 50-pin connector of the SCSI bus cable is plugged into connector J1 at the top center of the UC01/L controller. The other end of the SCS1 bus cable is plugged into I/O connector on the first drive. If more than one drive is used, the other drives are daisy chained. Most drives have two I/O connectors that are identically wired one-to-one, so that daisy chaining can be easily accomplished. The last drive on the daisy chain should have a terminator installed. The terminator should be supplied by the drive manufacturer. The terminator is generally plugged into one of the two paired daisy-chain connectors on the drive. Sometimes a ground wire, emerging from the terminator assembly, must be connected to the drive to provide a ground return for the resistors in the terminator assembly. Pin 1 of connector J1 on the controller is on the left when viewing the omponent side of the controller. Pin 1 of the cable connector has a notch on the connector body to identify it. Twisted pairs of wires in the flat cable have brown-brown twist followed by red-brown twist on pin 1 edge of cable. The cable normally exits to the rear of the CPU chasis in which the controller is installed.

NOTE

Connector J1 is not keyed and can be physically reversed in the header. No damage can result from reversed cable connecton, but the subsystem cannot function.

3.7.2 Grounding

For proper computer system operation, all components must have a common Earth ground; i.e., a reliable DC ground connection to the logic ground of the computer, and separated from AC ground. The ground connection should be 1/2-inch braid (preferably insulated) or AWG number 10 or larger. The grounding wire may be daisy-chained between drives. If the drive has a switch or a jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), that connection should be removed when the drive is placed in the On-Line mode with the controller. The DC-AC ground interconnect should be used only when performing local off-line diagnostic tests and maintenance on the drive only.

NOTE

Failure to observe proper grounding methods generally results in marginal system operation with random error conditions.

3.8 TESTING

Testing involves self-test, register examination, hardware formatting, and diagnostics.

NOTE

The register addresses mentioned in the following paragraphs are 18-bit addresses. For system devices that use 22-bit addressing, add 17000000 to obtain

the correct address for each register; e.g., register address 774400 becomes 17774400.

3.8.1 Self-Test

When power is applied to the CPU, that power is also simultaneously applied to the UC01/L controller. Since the UC01/L controller derives its power from the Q-Bus interface with the CPU, the controller automatically executes a built-in self test. The self test is not executed with every INIT signal from the Q-Bus, but only at power-up time. If the self test is successful, the LED on the top edge of the controller becomes extinguished or flashes. The LED flashes when the controller cannot properly address one drive after successful self-test execution. Such flashing can occur if SCSI bus cable is not properly connected, a drive is not powered up with a unit select code plug, or two drives have identical unit select code plug. Steady illumination of the LED indicates the controller failed the self test and cannot be addressed from the CPU.

3.8.2 Register Examination

After power up of CPU and noting LED on controller is not steadily lit, a quick check should be made to verify that all controller registers can be read from the computer console. The Control Status Register (CSR) 774400 should contain 000201 if the controller and drive 0 are both in the Ready state.

3.8.3 Hardware Formatting Media

The controller can format the disk or tape media by writing headers and bad block file data in all data blocks of the media. This formatting command does not verify the data or the headers. For example, if the sytem contains disk drives which are on line, the disk formatting should occur in the following event sequence:

a. Deposit 000013 into Disk Address Register (DAR), 774404.

b. Select drive to be formatted by depositing drive number in bits 09 and 08 of CSR, 774400. Bit 02 must also be set simultaneously.

c. Examine CSR contents. Bit 15 (Error) should be logic 0 and bit 01 (Drive Ready) should be logic 1.

d. Deposit a number to be used as pack identification (ID) in Multipurpose Register (MPR), 774406.

e. Deposit 100001_8 in Bus Address Register (BAR), 774402, to enable Extended command set.

f. To start formatting, deposit in CSR (774400) a hardware Format command for appropriate drive as defined in Table 3-6. Activity LED at top of controller, next to DIP switch SW1, should flash while formatting operation is in progress, when LED is completely extinguished, Format operation is done.

Table 3-6. Hardware Format Command

Drive No.	Command
0	34004
1	34404
2	35004
3	35404

3.8.4 Diagnostics

To verify proper operation of the entire system, run the following DEC RL01/RL02 diagnostics:

- o ZRLGBO - Controller Test No. 1
- o ZRLHBO - Controller Test No. 2
- o ZRLMBO - Bad Sector File Tool
- o ZRLKB1 - RL01/RL02 Performance Exerciser

Without the programmable clock, the diagnostics skip some sections which time drive operations; including those operations that would fail because the physical drive being used is either faster or slower than the real RL02 drives.

On the RL01/RL02 Performance Exerciser diagnostic, the first Read Header operation times out because of the eight-second delay. The user should proceed from the error, and all should continue well; before starting this diagnostic, the user can make the diagnostic more patient by patching location 24352_8 to provide a 20 instead of a 2.

Section 4
PROGRAMMING, AND CONTROLLER REGISTERS

4.1 INTRODUCTION

This section describes programming techniques, option characteristics, and controller registers. Programming information reveals how various operations are handled. Option characteristics describes details of LTC function and bootstrap routines. The controller registers subsection explains the function of each bit in each controller register during performance of commands. Since there are more commands than there are registers, each of the eight registers in the controller generally contributes to the performance of several functions.

4.2 PROGRAMMING INFORMATION

This subsection explains Interrupt and Seek operations, Data Transfer operations, error correction and recovery, 22-bit memory addressing, and special commands.

4.2.1 Interrupt Operations

If the Interrupt Enable (IE) and Controller Ready (CRDY) bits in the CSR are both set (logic 1), the controller can request an Interrupt operation. The IE bit is set or reset (logic 0) by the software. It is also reset by the Initialize (INIT) condition. The CRDY bit is set by the software when a function is done, by an error flag when an error is detected, or by the INIT condition. CRDY can also be set by the software to cause the controller to start a function (negative GO bit). The Interupt Vector Address for controller number one is 160, unless alternate 370 is selected by DIP switch SW2.1. The Interrupt Vector Address for controller number two is 214, unless alternate 374 is selected by DIP switch SW2.2. The normal priority level for the RLV11 Q-Bus is BUS REQUEST 5. The Q-Bus connectors for the RLV11/RLV12 controller, which the Emulex UC01/L controller replaces, uses this normal priority level.

4.2.2 Seek Operation

The Seek operation is performed in the following event sequence:

a. Issue Read Header command to drive, then wait for IE or CRDY signal.

b. Check for error Flag.

c. Read header word from MPR.

d. Calculate difference and direction for Seek operation.

e. Move difference word to DAR.

f. Issue Seek command to drive and wait for Seek operation to be indicated completed by Drive Ready (DRDY) bit 00 in CSR set.

g. Check error flag again.

A software system that optimizes positional latency would keep current data block address inforamtion in core so that steps b, c, and d of the foregoing event sequence would be unnecessary.

4.2.3 Overlapped Seek Operations

Since the controller becomes ready and interrupts as soon as a Seek command is issued, it is possible to issue Seek commands to other drives on the SCSI bus while the first drive is seeking. When any Seek operation is completed, however, no Interrupt condition occurs; therefore, the Data Transfer command should be issued to the drive that needs the shortest Seek time. As soon as all required Seek commands have been issued, the drive which first completes its Seek operation can immediately perform its commanded Data Transfer operation, and issue an Interrupt signal when done.

4.2.4 Data Transfer Operations

A Data Transfer operation is the performance of a Read or Write command. The user should not attempt to do a Write operation on a Write Protected (or Write Locked) drive.

Data Transfer operations are conducted via direct memory access (DMA) facility. The UC01/L controller (number one or number two) provides 256 words of first in-first out (FIFO) random access memory (RAM) buffering; which, like the DEC RLV11/RLV12 controllers, prevents data-late conditions from occurring. Transfers of data to memory (Read operations) are initiated only after the entire data block (sector) has been read. Transfers of data to media (write operations) are initiated only after an entire data block has been loaded into the FIFO RAM buffer.

To perform a Read or Write operation, the software should perform the following event sequences:

a. Load Bus Address Register (BAR) with address if first memory location whose contents are to be transferred.

b. Load Device (Disk) Address Register (DAR) with address of first media (disk) location whose contents are to be transferred.

c. Load Word Count portion of MPR with two's complement of number of words to be transferred.

d. Issue Read Data command or Write Data command, then wait for Interupt signal or test for Drive Ready (DRDY) status condition.

e. Check for error flag.

Other drives in the system could perform Seek or Data Transfer operations during times **between** issuance of seek commands and the issuance of Read or Write commands.

4.2.5 Recovery of Data from Blocks with Bad Headers

Function Code 7 (see description of bits 03:01 of CSR), Read Data Without Header Check, is provided to allow recovery of data from data blocks whose headers have beome unreadable. If constant HNF or HCRC errors are encountered in a particular data block so that data cannot be recovered by a standard Read command, use the following procedure:

a. Perform successive Read Header commands until data block which precedes data block with bad head is found.

b. Issue Read Data Without Header Check command. Data portion of next data block without header compare or header CRC check. Data CRC errors should be reported.

4.2.6 22-Bit Memory Addressing

The 22-Bit Memory Addresing option is Emulex P/N SC0213102, which consists of a single AMD2908 IC, installed in IC socket U126 on the controller PCBA.

The option is enabled by closing DIP switch SW2.7 in this mode, the UC01/L controller emulates the RLV12 controller, which incorporates this feature. Bits 05:00 in the Bus Address Extension Register (BAE) then serve as address bits 21:16: Address extension bits 17 and 16 are duplicated in the CSR (bits 05 and 04, respectively), and they may be modified or examined via either the BAE or CSR.

4.2.7 Deleted Commands

The UC01/L controller emulates the RLV11/RLV12 controller in its responses to all normal commands and register modifications.

4.2.8 Extended Commands

The UC01/L controller can use extended commands that are not implemented by DEC RLV11/RLV12 controllers. These commands allow formatting of media, replacement of tracks, write protection of logical drive units (as well as physical drive units), and various diagnistic functions. Details of extended commands are explained in Section 5.

4.3 OPTION CHARACTERISTICS

The bootstrap routines and Line Time Clock (LTC) feature are options that are enabled by installing special kits in IC sockets on the controller PCBA and/or by closing/opening certain switches in DIP switch packs on the controller PCBA (see paragraphs 3.6.6.3 and 3.6.6.4, respectively).

4.3.1 Bootstrap Routines

Installing the Emulex Bootstrap Option Kit (P/N SC0213001) makes the Standard Console Bootstrap Routine and the Auto-Boot Sequence available as options. Programming information for these options is presented separately.

4.3.1.1 Standard Console Bootstrap

The Standard Console Bootstrap routine allows the user to select one of several bootstrap routines provided by the Bootstrap option by using the system console.

The LSI-11 CPU enters the Standard Console Bootstrap Routine at address location 773000. The CPU PCBA can be jumpered to automatically start at location 773000 during power up (or external DCLO signal set-reset).

After performing several CPU tests, the Standard Console Bootstrap program prompts the operator by displaying a dollar symbol ($) on the screen of the console terminal whose bus addresses are 777560-777564. At this point, the Bootstrap Routine expects terminal input via the console keyboard. If no $ prompt symbol is displayed (or printed on a printing device), then the bootstrap program failed one of the CPU tests it executed before entering the Terminal Input mode.

When the $ prompt symbol appears, the Bootstrap program is ready for input from the terminal. The user should enter one of the two-character codes, plus a single octal number (if an octal number is required and the unit number to be bootstrapped is not zero), followed by a carriage return. Codes and names for Bootstrap routines are listed in Table 4-1. The two-character codes represent Bootstrap routines for specific types of peripheral devices; i.e., drives, etc. When the code is entered, the Bootstrap routine represented by the code is executed. If the code is not recognized, a question mark (?) followed by the $ symbol is displayed or printed. The code to use for the UC01/L controller is "DL".

Table 4-2 contains a list of HALT Routine location addresses. The associated PROM program executes the instructions contained in the appropriately addressed memory location if the Bootstrap Routine, selected from Table 4-1, is not successfully completed.

4.3.1.2 Auto-Boot Sequence

The Auto-Boot Sequence automatically bootstraps the system without operator intervention when the system is powered up or when an external DCLO signal is generated.

The CPU enters the Auto-Boot Sequence at memory location 765000. The LSI-11/23 CPU can be jumpered to start at location 765000 automatically (see paragraph 3.6.6.3).

After performing a Memory Test, the Auto-Boot Sequence is programmed to attempt bootstrapping the system from an RK06/07. If none is present, the sequence attempts to bootstrap the system from an RP02/03. If there is no RP02/03, it attempts to find an RL01/02. In all attempts, the Auto-Boot Sequence only attempts to bootstrap from logical drive unit zero.

If none of the above logical drive units, emulations, or entry points is available for any reason (see Table 4-2), the program prompts the operator with the $ symbol. The operator then uses the terminal keyboard to enter a Bootstrap code (see paragraph 4.3.1.1 and Table 4-1).

Table 4-1. Bootstrap Routine

Code	Name/Description
XC	Execute CPU tests 7-9 only.
XM	Execute memory tests only.
OD	ODT Halt. No routines are executed. A Proceed (P) instruction returns the program to the Terminal Input mode.
MTn	TM11 Magnetic Tape Bootstrap Routine. Can bootstrap logical drive units 0-7.
DXn	RXV11 Floppy Disk Bootstrap Routine. Can bootstrap logical drive units 0-1.
DKn	RK05 Disk Bootstrap Routine. Can bootstrap logical drive units 0-7.
RPn	RP02/3 Disk Bootstrap Routine. Can bootstrap logical drive units 0-7.
DMn	RK06/7 Disk Bootstrap Routine. Can bootstrap logical drive units 0-7.
DBn	RM02/3/5 Disk Bootstrap Routine. Can bootstrap logical drive units 0-7.
DYn	RX211/RX02 Disk Bootstrap Routine. Can bootstrap logical drive units 0-7.
DLn	RL01/02 Disk Bootstrap Routine. Can bootstrap logical drive units 0-7.
DD	TU58 Tape Unit Bootstrap Routine. Can bootstrap logical drive unit 0 only.

NOTE: If "n" not entered, a default unit number of 0 is assumed.

Table 4-2. HALT Routines

HALT Address	Reason for HALT
765320	Nonexistent logical drive unit, logical drive unit not on line and ready, or controller not ready.
765612	Read Error, or Disk Error from aborted Read operation.
765674	Read operation not completed within time limit.
773434	Failure detected in CPU test number 7.
773530	Failure detected in CPU test number 8.
773550, 773556, or 773604	Failure detected in CPU test number 9.
773730	Failure detected in Memory test number 1.
773760	Failure detected in Memory test number 2.

4.3 2 LTC Option

The Line Time Clock (LTC) is a 60 Hertz (HZ) clock pulse which is generated by the LSI-11 CPU power supply and distributed to the Q-Bus backplane as the BEVNT signal (see Table 2-3, connector B, pin R). The high-to-low trailing-edge transition of this signal interrupts the LSI-11 CPU. BEVNT has the highest external interrupt priority; only CPU interrupts have higher priorities. If external Interrupt conditions, such as Power Supply (PS) bit 07 = 0 are present, the processor (PC) word R7 and the PS word are placed on the processor stack. The LTC (or external event device) Service Routine is entered by Vector Address 100; the usual Interrupt Vector Address input operation by the processor is not required because Vector Address 100 is generated by the processor.

LTC operaton can be software-controlled by using the Line Clock Register on the UC01/L controller. This register has a memory address of 777546. The Line Clock Register is a one-bit, Write-only register; therefore, commands to read the contents of this register return unspecified data. The Line Clock Register uses bit 06 only. A Write command issued to this register when bit 06 is set to logic 1 enables the Line Clock pulse; conversely, if bit 06 is reset to logic 0, the Line Clock pulse is disabled. If an Interrupt condition occurs, bit 06 of the line clock register is reset, and the Interrupt condition condinues until bit 06 is set again, or until an INIT command is generated and executed.

To configure the CPU for use with the LTC feature, see paragraph 3.6.6.4.

4.4 CONTROLLER REGISTERS

The standard DEC RLV12 controller has five registers that are used to control and monitor operations within the controller and its associated drives. The Emulex UC01/L Universal Controller includes three additional registers that are used to enhance performance and extend functional capability of the controller: e.g., media formatting. This subsection defines the functions and bits in each of the eight registers for various operations performed by the UC01/L controller.

4.4.1 Control Status Register (CSR)

The CSR can be used for Normal Functions and for Extended Functions.

4.4.1 1 CSR Normal Functions

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	DE	NXM	E2	E1	E0	DS1	DS0	CRDY	IE	BA17	BA16	F2	F2	F0	DRDY

Composite Error (ERR) - Bit 15

When set, this bit indicates one or more of the error bits (bits <14:10>) is set. If the IE bit (bit 06 of CSR) is set and an error occurs (which sets bit 07 of CSR), an Interupt condition is initiated.

Drive Error (DE) - Bit 14

This bit reports error status directly form the emulated drive when set, it indicates the selected drive has flagged an error. The source of the error can be determined by executing a Get Status command. DE can be cleared by executing a Get Status command with DAR bit 03 set.

Non-Existent Memory (NXM) - Bit 13

This bit is set when the addressed memory does not respond within 10 to 20 microseconds from the beginning of a direct memory access (DMA) Read or Write operation.

NOTE

Bits 12, 11, and 10 are error code bits that may be used singly or in combination, as defined in the following Error Summary:

	Bits		
Error Name	12	11	10
Operation Incomplete (OPI)	0	0	1
Read Data CRC	0	1	0
Write Check	0	1	0
Header CRC	0	1	1
Data Late (DLT)	1	0	0
Header Not Found (HNF)	1	0	1

Data Late (DLT) or Header Not Found (HNF) - Bit 12 (E2)

This bit is set during a Write operation when the silo is empty while the word count has not yet reached zero (indicates Bus Request ignored for too long a time); however, OPI bit 10 is not set.

If this bit and the OPI bit are both set, the error code indicates the controller could not ifnd the correct data block to read from or write to; i.e., HNF and no header comparison could be made.

Read Data CRC (DCRC), or Write Check (WCE), or Header CRD (HCRD) - Bit 11 (E1)

If this bit is set and bits 12 and 10 are cleared, error code indicates a CRC error occurred when reading the data (DCRC). If this bit is set and bits 12 and 10 are cleared while a Write Check command is being executed, error code indicates a Write Check Error (WCE) has occurred.

If this bit and bit 10 are set, and bit 12 is cleared, error code indicates a CRC error occurred when reading the header (HCRC).

NOTE

Cyclic redundancy checking is performed on the first and second header words, even though the second header word always contains all zeros.

Operation Incomplete (OPI) - Bit 10 (E0)

When this bit is set, error code indicates the current command could not be completed.

Drive Select (DS0, DS1) - Bits <09:08>

The condition of these bits determines which logical drive unit is to communicate with the controller.

Controller Ready (CRDY) - Bit 07

When cleared by software, this bit indicates the command represented by function code bits <03:01> is being executed, and that the controller is busy and unable to accept another command. When set, this bit indicates the controller is not busy and is ready to accept another command.

Interrupt Enable (IE) - Bit 06

When this bit is set by software, the controller is allowed to interrupt the CPU immediately after a normal command or error recovery function is terminated.

Bus Address Extension Bits (BA16, BA17) - Bits <05:04>

These are the two most significant bus address bits. They are read and written as data bits 05 and 04 in the CSR but are considered as bits 16 and 17 of the Bus Address Register (BAR).

Function Code - Bits <03:01>

These bits are set by software to indicate the command to be executed. For a command selected by the function code to be executed, the CRDY bit 07 must be cleared by software. A logic zero in bit 07 of the CSR is therefore the GO bit that causes command execution. Like the error bits, the function code is shown in the following summary:

Function Code Summary

Function Code (Octal)	Function/CSR Bit F2/03	F1/02	F0/01	Command
0	0	0	0	Maintenance
1	0	0	1	Write Check
2	0	1	0	Get Status
3	0	1	1	Seek
4	1	0	0	Read Header
5	1	0	1	Write Data
6	1	1	0	Read Data
7	1	1	1	Read Data Without Header Check

Drive Ready (DRDY) - Bit 00)

When set, this bit indicates the selected drive is ready to receive a command. This bit is cleared when a Seek operation is initated, and set when the Seek operation is completed.

4.4.1.2 CSR Extended Functions

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	1	1	1	0	0	0	0	0	0	0	F3	F2	F1	F0

To enable the CSR extended function set, the BAR must be written with 100001_8. The command is immediately written into the CSR with bits <13:11> set to logic one, and with the extended command function code set into the CSR bits <03:00>.

Function Code (<F3:F0>) - Bits <03:00>

The function code selects one of the commands shown in the following summary:

Extended Function Code Summary

Function Code (Octal)	Function/CSR Bit F3/03	F2/02	F1/01	F0/00	Command
0	0	0	0	0	Write Switch Register
2	0	0	1	0	Read Firmware Register
4	0	1	0	0	Firmware Format
6	0	1	1	0	Write Bad Sector Files
10	1	0	0	0	Transfer SCSI Command Packet Without Data
12	1	0	1	0	Transfer SCSI Command Packet With Data

In the foregoing function code table, all codes have an even octal number. Codes 8, 14, and 16 are reserved.

4.4.2 Bus Address Register (BAR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bus Address															0

The BAR is a 16-bit register whose address is 774402. Bits <15:01> can be written to or read from; bit 00 is always logic zero. Bus Address bits 16 and 17 are contained in bits 05 and 04 of the CSR (see paragraph 4.4.1.1.).

The BAR indicates the memory location involved during a normal Read or Write operation. The contents of the BAR are automatically incremented by two as each word is transferred between the SCSI bus and the I/O buffer. This register overflows into CSR bits 05 and 04. The BAR is cleared by initializing the drive, or by loading the BAR with logic zeros in all bits.

Bus Address (<BA15:BA00>) - Bits <15:00>

These bits point to the Q-Bus address to/from which data are to be transferred (normally a memory address). Bit 00 is always logic zero. BA16 and BA17 are in CSR bits 05 and 04, respectively.

4.4.3 Drive Address Register (DAR)

The DAR is a 16-bit register whose address is 774404. Its contents can convey any one of four meanings, depending on the function being performed: Seek command, Read or Write command, set status

command, or Write Header command (extended). The DAR is cleared by initializing the drive, or by loading all bits in the DAR with logic zeros. The processor can read or write all 16 bits of the DAR contents.

4.4.3.1 DAR During Seek Command

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0	0	0	HS	0	DIR	0	1

To perform a SEEK command, cylinder address difference, head select, and head directional information for the selected drive must be provided in the DAR.

Cylinder Address Difference (<DF8:DF0>) - Bits <15:07>

These nine bits indicate an octal numer that represents the number of cylinders the heads are to move from/to during the the SEEK command execution.

Head Select (HS) - Bit 04

This bit indicates which head (disk surface) is selected. Logic one indicates lower head; logic zero indicates upper head.

Direction (DIR) - Bit 02

This bit indicates direction heads are to move during SEEK operation. When set (logic 1), heads move toward spindle (higher cylinder or track address number). When cleared (logic 0), heads move away from spindle toward outer edge of disk (lower cylinder or track address number). Actual number of tracks crossed (distance moved) depends on contents of DAR bits <15:07>.

4.4.3.2 DAR During Read or Write Command

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

For a Read or Write operation, the DAR is loaded with the address of the first data block (sector) to be transferred. As each successive data block is transferred, the DAR contents are automatically incremented.

Cylinder Address (<CA8:CA0>) - Bits <15:07>

These nine bits represent the cylinder (track) address that is being accessed for the Read or Write operation. The cylinder address is an octal number that can range from 000 to 777.

Head Select (HS) - Bit 06

This bit indicates the disk surface to be selected. Set (logic 1) is lower surface, and cleared (logic 0) is upper surface.

Sector Address (<SA05:SA00>) - Bits <05:00>

These six bits represent the sector (data block) address that is being accessed for the Read or Write operation. The sector address is an octal number that can range from 00 to 40, but since the system never uses more than 32 sectors/track on a disk drive the sector address for any particular track can never be more than 32 or the address is illegal and not recognized.

4.4.3 3 DAR During Get Status Command

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

For a Get Status command, the DAR bits must be programmed as shown in the above bit-configuration example.

Reset (RST) - Bit 03

When this bit is set, the drive clears its error register before sending a status word to the controller.

Get Status (GS) - Bit 01

Must be set (logic 1) to notify drive that status word is being requested. When Get Status command is completed, drive status word is loaded in controller's MPR and can be read by processor. When bit 01 is set, drive ignores contents of DAR bits <15:08>. (See paragraph 4.4.4.1.)

4.4.3.4 DAR During Write Header Command (Extended)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
First Header Word															

First Header Word - Bits <15:00>

Before executing a Write Header command, the first header word is loaded into DAR. See paragraph 2.4.4.1. for description of normal header format.

4.4.4 Multipurpose Register (MPR)

The MPR is a 16-bit register whose address is 744406. Its contents can convey any one of five meanings which depend on the function being performed:

a. After Get Status command
b. After Read Header command
c. During Read/Write Data commands
d. During Multipurpose command (extended)
e. During Write Header command (extended).

4.4.4.1 MPR After Get Status Command

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	WL	SKTO	SPE	WGE	VC	DSE	DT	HS	CO	HO	BH	State		

When a Get Status command (see paragraph 4.4.3.3) is executed, the status word is returned to the controller and transferred to the MPR. The contents of the MPR are defined in the following bit descriptions:

Write Lock (WL) - Bits 13

Set when the drive is logically or physically write protected.

Seek Time Out (SKTO) - Bit 12

Set when seek cannot be completed on a drive because of a drive fault or because it has gone off-line.

Write Gate Error (WGE) - Bit 10

Set if an attempt is made to write on a drive that is logically or physically write protected.

Volume Check (VC) - Bit 09

Set when physical drive becomes on-line and ready. Cleared by execution of a Get Status command with RST (bit 03) asserted.

Drive Type (DT) - Bit 07

A logic zero indicates an RL01 emulation; a logic one indicates an RL02 emulation.

Head Select (HS) - Bit 06)

Indicates the currently selected head. A logic zero indicates the upper head; a logic one, the lower head.

Cover Open (CO) - Bit 05

Set when physical drive is not on-line and ready.

Heads Out (HO) - Bit 04

Set when physical drive is on-line and ready.

Brush Home (BH) - Bit 03

Set when physical drive is not on-line and ready.

State (State) - Bits <02:00>

These bits define the state of the drive:

Bit			
02	01	00	
0	0	0	Load Cartridge - drive exists but not on line
1	0	0	Seek - Seek state
1	0	1	Lock On - normal Ready state

4.4.4.2 MPR After Read Header Command

When a Read Header command is executed, the three words of the next header (see example) are read, stored in the data buffer, and transferred to the MPR. Word one contains sector address, head select, and cylinder address information. Word two contains all zeros. Word three contains header CRC information. All three words are read sequentially by the program.

Word One

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

Word Two

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ZEROS															

Word Three

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CRC															

Cylinder Address (<CA8:CA0>) - Bits <15:07>

Address, in octal, of cylinder being accessed. Range is from cylinder 000 through 777.

Head Select (HS) - Bit 06

Indicates selected disk surface. Logic one is lower surface, and logic zero is upper surface.

Sector Address (<SA5:SA0>) - Bits <05:00>

Address, in octal, of one of up to 40 sectors on the addressed cylinder (see SA description in paragraph 4.4.3.2.).

4.4.4.3 MPR During Read/Write Data Commands

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	Word Count												

Before reading or writing data, the program should load the word count into the Word Count bit locations of the MPR in two's complement format. The word counter is incremented as each word is

transferred. The Read or Write operation is usually terminated when the word counter reaches zero (overflows). The word counter can count any number of data words, from one to a full count of 5120 (decimal) data words. Bits <15:13> must be always logic ones.

Word Count (<WC12:WC00>) - Bits <12:00>

Contains two's complement of total number of words to be transferred. Bit 00 is least significant bit (LSB).

NOTE

When programming the MPR, the user should be aware that RL01 and RL02 drives do not perform spiral Read/Write operations. If data are to be transferred past the end of the last sector (data block) on a track, the opeartion must be done by using the following event sequence:

a. Program Read or Write operation to terminate at end of last sector on track.

b. Program Seek operation to next track; can be head switch to other surface, but same cylinder, or head move to next cylinder without head switch.

c. Program Read or Write operation to start at first word of first sector at next track.

4.4.4.4 MPR During Multipurpose Command (Extended)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	HSL	0	0	0	0	0	0	0	0	WL3	WL2	WL1	WL0

Before the program issues a Multipurpose command, the bits in the MPR should be set as shown in the above configuration.

Header Search Limit (HSL) - Bit 12

When set (logic 1), this bit limits header search attempts to one disk revolution instead of three.

Write Locked (<WL03:WL00>) - Bits <03:00>

When any one of bits <03:00> is set, the correlating drive (drive 3 is bit 03, drive 1 is bit 01, etc.) is Write Locked. Each bit may

be set independently of the others. Write Locked drives reject Write commands.

4.4.4.5 MPR During Write Header Command (Extended)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Pack ID															

Before the program issues a Write Header command, the MPR should be loaded with the Pack ID that is used for the Bad Sector File.

Pack ID - Bits <15:00>

These bits represent the identification used for the Bad Sector File.

4.4.5 Bus Address Extension (BAE) Register

The BAE is a 16-bit register whose address is 744410. Its contents can convey either of two meanings, depending on the function being performed: Read Data or Write Data commands, or Write Header command (extended).

4.4.5.1 BAE During Read Data or Write Data Commands

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	Cylinder Address <15:09>							0	0	Bus Address <21:16>					

Cylinder Address (<CA15:CA09>) - Bits <14:08>

These bits function as an extension of the nine cylinder address bits <CA14:CA00> in the DAR when expanded logical drive units are configured in the subsystem. They are needed to specify the larger cylinder addresses of the expanded logical drive units.

Bus Address (<BA21:BA16>) - Bits <05:00>)

These six bits serve as an extension of the BAR to allow 22-bit bus addresses to be specified for DMA transfers. Bits 00 and 01 (BA16 and BA17) are the same as bits 04 and 05 of the CSR. Bits <05:02> function as bus address bits <18:21> only if the RLV12 mode is enabled; i.e., DIP switch SW2.7 ON.

4.4.5.2 BAE During Write Header Commands (Extended)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Second Header Word															

Second Header Word - Bits <15:00>

Before requesting a Write header command, the second word of the header that is to be written is loaded in the BAE Register. Normal format for the second header word is described in paragraph 2.4.3.1. and Figure 2-6.

4.4.6 Registers 5, 6, and 7

Each of these three registers contains 16 bits. Their addresses are 774412, 774414, and 774416, respectively. In normal functions they are extra "scratch pad" registers for reading and writing. Their contents may be read or written any time the controller is not otherwise busy. Data written to or read from these registers have no significance. In extended command functions, these registers are used as described in subsection 5.3.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Extra Register															

5.1 INTRODUCTION

This section describes the function codes used by the controller for performance of standard functions and extended commands. The function code number for a standard function may be the same as that for an extended command, but because of different context does not necessarily cause the same event sequence to occur.

5.2 STANDARD FUNCTIONS

The controller uses seven function codes to perform seven standard functions.

5.2.1 Write Check Operation - Function Code 1

The Write Check command is issued after writing a block of data on the media. It is used to compare the written data with the contents of the source data buffer in the main memory, and thus ascertain whether the data was or was not written correctly. Because this comparison is performed in the controller, the source data must be taken from the main memory in the CPU and transferred to the silo in the controller.

Before issuing the Write Check command, the BAR must be loaded with the address of the first location of the data block in the main memory. The Word Count portion of the MPR must be loaded with the length of that data block. The BAR is then loaded with the starting media address location. When these registers have thus been loaded with the appropriate address and word-count information, the Write Check command can be loaded into the CSR.

If a Compare Error or Data CRC Error occurs during the Write Check operation, CSR bit 11 is set (see paragraph 4.4.1.1.).

5.2.2 Get Status Operation - Function Code 2

The Get Status command causes the status word from a drive to be transferred to the controller where the software can access that status word through the MPR. The software sjpi;d then perform the following event sequence:

a. Verify controller is ready to perform an operation (no drive has to be ready).

b. Load DAR bits 01 and 00 with logic ones, a reset in bit 03, and a logic zero in each of the other DAR bit locations.

c. Load CSR with applicable drive select bits, a negative GO bit, IE bit (if desired), and a code of 2 in the function bits.

The controller then commands the selected drive to transfer its status word to the MPR in the controller. If the "Reset" bit 03 in the DAR was set, the drive would reset its status register first before transferring the contents of that register to the controller's MPR.

5.2.3 Seek Operation - Function Code 3

The Seek command causes the positioner motor on the selected disk drive to move the heads in the forward or reverse direction a specific number of cylinders. The software should first verify the drive is ready to accept a command, then load the DAR with the difference word; i.e., difference between current cylinder address (head position) and new cylinder address. This word contains an octal number that represents the number of cylinders which the head must move across (bits <15:07>), the head select bit (bit 04), and the direction (DIR) bit (bit 02). When the head select bit is set (logic one) the bottom disk surface is selected, when it is reset (logic zero), the upper disk surface is selected. When the direction bit is set (logic one) head motion is forward toward the spindle, and when it is reset (logic zero), head motion is reversed toward the outer edge of the disk. Also in the DAR, bits 06, 05, and 01 must be reset (logic zero), and bit 00 must be set (logic one).

After the DAR is loaded, the software should load the command word in the CSR. The command word should contain the drive select code (bits 09 and 08), the negative GO bit (bit 07), the IE bit (bit 06, if desired), and the three bits of the function code (bits (<03:01>). The controller then sends the Seek command to the selected drive, which should cause that drive to start the Seek operation. At this time, the controller attains Ready status (CRDY bit 07 in CSR set) and interrupts the CPU if IE (CSR bit 06) is set. The controller is then ready to receive another command that can perform another operation on another drive while the Seek command on the first drive is being executed.

If the difference word is so large that the heads attempt to move past the physical location of the inner or outer cylinder, the heads of the drive automatically stop at the guard band and then retreat to the first-encounted even-numbered cylinder (data tracks).

5.2.4 Read Header Operation - Function Code 4

When a Read Header function code is detected and decoded, the controller reads the first logical header address encountered in the selected drive and places the three words of that header in the silo. Those header words pass through the silo and stop with the first word of the MPR. Software can then access the first word to determine the current data block (sector) address, head selected, and cylinder address. When the software extracts the first-encountered logical header address word from the MPR, the third word of the first-encountered logical header address is automatically loaded into the MPR. This third word is the CRC word. When the CRC word is loaded into the MPR, the software can access and examine that word for checking purposes.

NOTE

Execution of the Read Header command is software simulated; i.e., no actual Read Header operation occurs. Each time the Read Header function is so simulated, the next sequential logical header data are used.

5.2.5 Write Data Operation - Function Code 5

When a Write Data function code is detected and decoded, while bit 07 (CRDY) in the CSR is cleared, the controller starts reading successive logical header address words and compares them with the contents of the DAR. When a match is found, the header CRC is checked, and if that CRC is correct, that data block (or sector) is written with the words from memory that are specified in the BAR. The word count portion (two's complement format) of the MPR and the address in the BAR are incremented, as applicable, for each word transferred during the Write Data operation. If a data block or sector is to be only partly filled by the Write Data operation, the remaining words in that data block or sector consist of all zeros. At the end of the data block or sector, the sector address portion (bits <05:00>) of the DAR is incremented. The next sector is then written, if all the words have not been written in the preceding sector. At the end of the Write Data operation, bit 07 (CRDY) in the CSR is set, and the CPU is interrupted if IE (CSR bit 06) is set. The controller is then ready to receive and execute another command.

5.2.6 Read Data Operation - Function Code 6

When a Read Data function code is detected and decoded, while bit 07 (CRDY) in the CSR is cleared, the controller starts reading successive logical header address words and compares them with the contents of the DAR. When a match is found, the header CRC is checked, and if that CRC is correct that data block or sector is read and the words are placed in the memory location specified by the contents of the BAR.

The word count portion (two's complement format) of the MPR and the address in the BAR are suitably incremented for each word transferred during the Read Data operation. The Read Data operation continues until the contents of the word-count portion of the MPR are all zeros. At the end of each data block or sector, the sector address portion (bits <05:00>) of the DAR is incremented. If the MPR word has not overflowed, the next data block or sector is read. At the end of the Read Data operation, with MPR word count zero, bit 07 (CRDY) in the CSR is set, and the CPU is interrupted if IE (CSR bit 06) is set. The controller is then ready to receive and execute another command.

5.2.7 Read Data Operation Without Header Check - Function Code 7

When the Read Data Without Header Check function code is detected and decoded, the data portion of the sector that follows the next Sector pulse is read and the requested data words are placed in the memory location specified by the contents of the BAR. The word count portion (two's complement format) of the MPR and the address in the BAR are suitably incremented for each word transferred during the operation. The header is not compared or checked for CRC errors; however, data CRC is checked at the end of a sector. If the MPR word count has not overflowed (is not zero), the data portion of the sector is read. At the end of this operation, with MPR word count zero, bit 07 (CRDY) in the CSR is set, and the CPU is interrupted, if IE (CSR bit 06) is set. The controller is then ready to receive and execute another command.

5.3 EXTENDED COMMANDS

The UC01/L controller can execute an extended set of commands not found in the repertoire of DEC RLV11 and RLV12 controllers. To enable the extended command function set, the BAR must be written with 100001_8. The command is written into the CSR with bits 13, 12, and 11 set to logic one, and with the appropriate extended command function code set in CSR bits <03:00>. The extended commands are needed to perform the six special tasks enabled by the extended command function codes (see paragraph 4.4.1.2).

Before attempting to execute an extended command, the drive must be selected and on line, and the Volume Check bit for each drive must be cleared. The Volume Check bit is cleared by setting RST (bit 03) in the DAR and issuing a Get Status command.

Whenever an extended command is completed, bit 07 (CRDY) in the CSR is set, and the CPU is interrupted if IE (CSR bit 06) is set. The controller is then ready to receive and execute another command.

5.3.1 Write Switch Register Command - Function Code 0

This command is used to Write settings in a firmware switch register so that any or all drives are Write Protected. Before issuing the command, load the MPR with desired data for the firmware register switches. When the MPR is used for the Write Protect or Write Lock feature, its bits have the functions shown in Figure 5-1.

```
MPR bits 15 and 08              ; not used
MPR bits <14:09 and <07:04>     ; not yet assigned a function
MPR bit 03                      ; when set, causes drive no. 3
                                  to be Write Locked
MPR bit 02                      ; when set, causes drive no. 2
                                  to be Write Locked
MPR bit 01                      ; when set, causes drive no. 1
                                  to be Write Locked
MPR bit 00                      ; when set, causes drive no. 0
                                  to be Write Locked.
```

Figure 5-1. MPR Bit Functions, Write Locked Feature

Write Lock bits that are cleared (i.e., reset) enable writing to the respective drive.

5.3.2 Read Firmware Register Command - Function Code 2

This command causes the contents of the Firmware Register that are selected by the MPR to be placed in the MPR. Before executing the command, the desired Firmware Register address from the BAR (see paragraph 4.4.2) must be entered in the MPR. Consecutive Firmware Register contents may be read without re-entering data in the MPR after initial address entry if commands are issued consecutively.

5.3.3 Firmware Format Command - Function Code 4

This command causes the physical drive to format the media. Before the command is issued, the selected sector-interlace ratio must be written into the MPR; a logic zero causes a 1:1 ratio to be used (the 1:1 ratio performs best in most systems).

NOTE

If media have already been formatted at the factory before shipment, no reformat of media is required.

After depositing 100001_8 in the BAR, select drive with Drive Select code (CSR bits 09 and 08), then deposit 34004_8 in the CSR. As each drive is formatted, change Drive Select code to select another drive; repeat for all drives that are to be formatted.

5.3.4 Write Bad Sector File Command - Function Code 6

DEC systems and diagnostics are designed to examine the Bad Sector Files on every media, even when no bad sectors exist. To satisfy system software requirements, this command is used to write an empty file format on all system media. A number to be used for the Pack Identification number (part of the empty Bad Sector File) must be deposited in the MPR before issuing the command.

After depositing 100001_8 in the BAR, select drive with Drive Select code (CSR bits 09 and 08), then deposit 34006_8 in the CSR. As writing of empty Bad Sector Files for each drive is completed, change Drive Select code to select another drive; continue until all drives are done.

5.3.5 Transfer SCSI Command Packet Without Data - Function Code 10

This command is used to transfer a user-defined command packet, via the UC01/L controller, between the memory and the SCSI drive. It should be used for commands which do not require data to be transferred from the controller during command execution. The command packet is taken from memory and sent to the logical drive unit which has been selected by the drive select code placed in CSR bits 09 and 08. Any data received by the controller during command execution are automatically transferred to the memory location specified for that data block.

Before loading the CSR and BAR to execute the command, use the following procedure:

a. Set aside a data block (number of bytes used must be exactly equal to data expectation) to hold any data generated by command.

b. If no data are to be generated by the command, set the word count (two's complement) for the data block to zero; i.e., load Register 6 with all zeros.

c. Load the command (maximum 12_{10} bytes) into memory.

d. Registers in controller should be loaded with the following contents:

BAR	100001_8 just before CSR is loaded.
DAR	Bus address of start of command block for SCSI command packet to be transferred.
MPR	Number of words (not bytes) in command block, in two's complement form.
BAE	22-bit address extension bits for data block address, if 22-bit address mode is to be used; otherwise all zeros.
Register 5	Bus address of data block.
Register 6	Number of words in data block in two's complement form (step b).
Register 7	22-bit address extension bits for command block address, if 22-bit address mode is to be used; otherwise all zeros.
CSR	3401_8 plus Drive Select bits 09 and 08 (load CSR last).

To properly execute the command, word counts (not byte counts) must be correctly entered for data blocks and command blocks.

After successful completion of the command, the ERR bit (CSR bit 15) should not be set, the DAR should contain the SCSI command-termination status byte(s) with LSB first, and the BAR should contain the address of the next data block location to be accessed.

5.3.6 Transfer SCSI Command Packet With Data - Function Code 12

This command is used to transfer a user-defined command packet plus associated data between the memory and SCSI drive via the UCO1/L controller. It is executed in the same way as Function Code 10 is executed (see paragraph 5.3.5), except the data block protion of the command is transferred from the addressed data block in the memory to the SCSI drive, rather than being filled with data from the SCSI drive.

5.3.7 Reserved Commands - Function Codes 8, 14, and 16

These Function Codes are reserved for extended commands that have not yet been specified. Any attempt to execute commands with these Function Codes set results in no operation performed, except CSR bit 07 (CRDY) is set and CPU is interrupted if IE (CSR bit 06) is set. The controller is then ready to receive and execute another command.

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Appendix A
UC01/L CONFIGURATION SELECTION

A.1 INTRODUCTION

To allow the user of the UC01/L controller the most flexibility in selection of SCSI drives, the UC01/L controller supports a variety of drive types and offers some user-selectable options. This appendix is intended as a quick reference to requirements for configurations in different installations, and to switch settings for user-selectable options.

A.2 CONTROLLER CONFIGURATION

The UC01/L controller can control SCSI-compatible drives of various types and capacities. The drives, which the controller can support, are defined by the parameters incorporated in the Configuration PROM (IC socket U64). Table A-1 lists and describes the types, sizes, and capacities of drives that are supported by the UC01/L controller. The user may choose available options by setting switches in applicable DIP switch packs to appropriate positions. Switch settings for selectable configuration are listed and described in Table A-2.

Table A-1. Drives Supported

Mfg.	Model	Cyl	Tracks	256 Byte Sectors	Key	Config.
Iomega	Alpha-10.5	306	1	134	I10	0-3
Xebec	ATASI-3046	645	7	32	X3046	1
Adaptec	ATASI-3046	645	7	32	A3046	2
Adaptec	FUJI- 2235	320	8	32	F2235	3

Table A-2. Drive Configurations

CONF NO.	SW4- 7	6	5	4	3	2	1	SW2- 8	RLV11 #	SCSI ADDRESS	DRIVE ADDRESS	Logical Units = Dr Type	KEY	Rev
00	C	C	C	C	C	C	C	C	0	0000001	0-3	0-3 = RL02	I10	A
									1	0000010	0-3	0-3 = RL02	I10	A
01	C	C	C	C	C	O	C	O	0	0000001	0	0-2 = RL02	X3046	B
									0	0000010	0	3 = RL02	I10	B
									1	0000100	0	0-2 = RL02	X3046	B
									1	0001000	0	3 = RL02	I10	B
02	C	C	C	C	C	O	C	O	0	0000001	0	0-2 = RL02	A3046	C
									0	0000010	0	3 = RL02	I10	C
									1	0000100	0	0-2 = RL02	A3046	C
									1	0001000	0	3 = RL02	I10	C
03	C	C	C	C	C	O	O	O	0	0000001	0	0,1 = RL02	F2235	D
									0	0000010	0	2 = RL02	I10	D
									0	0000100	0	0,1 = RL02	F2235	D
									0	0001000	0	2 = RL02	I10	D

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