μA9708

6-CHANNEL, 8-BIT, MICROPROCESSOR COMPATIBLE

ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM*

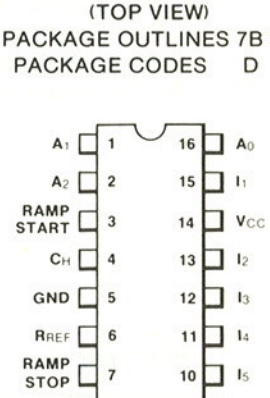
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA9708 is a single slope 8-bit, 6-channel ADC subsystem that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses a microprocessor system like the F3870 or F6800 to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

- **MPU COMPATIBLE**
- **EXCELLENT LINEARITY OVER FULL TEMP RANGE - ±0.2% MAX**
- **TYPICAL 300 μs CONVERSION TIME PER CHANNEL**
- **WIDE DYNAMIC RANGE INCLUDES GROUND**
- **AUTO-ZERO AND FULL-SCALE CORRECTION CAPABILITY**
- **RATIOMETRIC CONVERSION — NO PRECISION REFERENCE REQUIRED**
- **SINGLE-SUPPLY OPERATION**
- **TTL COMPATIBLE**
- **DOES NOT REQUIRE ACCESS TO DATA BUS OR ADDRESS BUS**

CONNECTION DIAGRAM
16-PIN DUAL IN-LINE

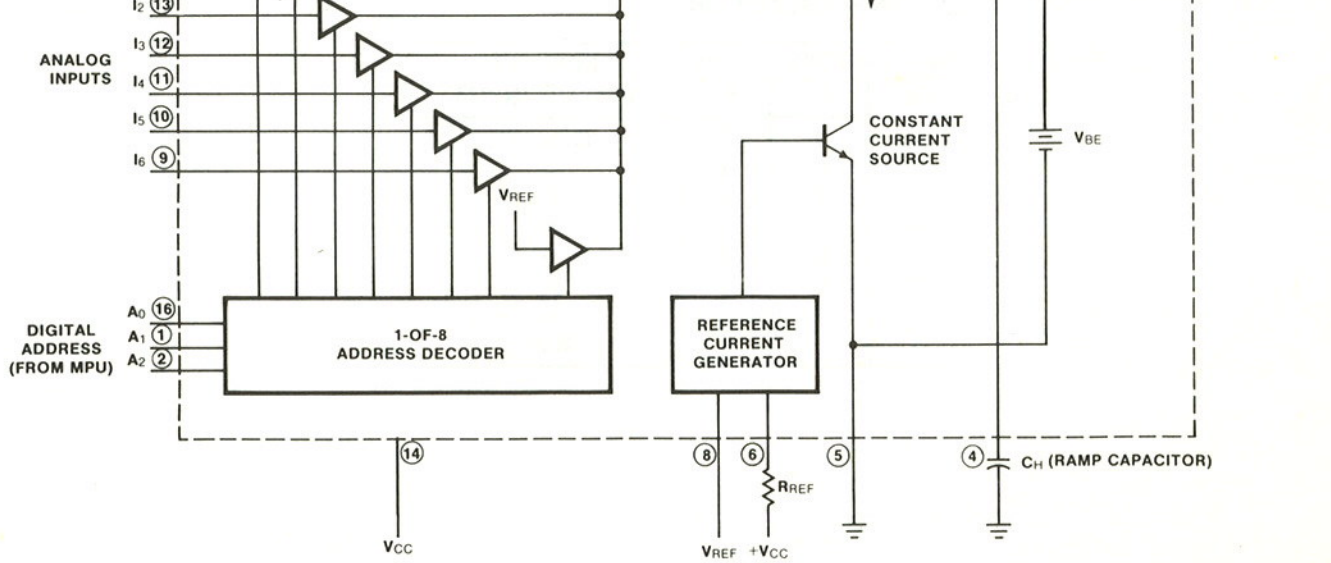
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA9708	μA9708DM
μA9708	μA9708DC
μA9708	μA9708PC

BLOCK DIAGRAM



 234-11-0016-118 15M

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	18 V
Comparator Output (Ramp Stop)	-0.3 V to +18 V
Analog Input Range	-0.3 V to 30 V
Digital Input Range	-0.3 V to 30 V
Output Sink Current	10 mA
Operating Temperature Range	
μA9708PC, μA9708DC	0° C to 70° C
μA9708DM	-55° C to 125° C
Storage Temperature Range	-65° C to +150° C
Continuous Total Dissipation	
Ceramic DIP Package	900 mW
Plastic DIP Package	1000 mW
Pin Temperature, Ceramic DIP (Soldering, 60 s)	300° C
Plastic DIP (Soldering, 10 s)	260° C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.0	15	V
Reference Voltage (V_{REF})*	2.8		5.25	V
Ramp Capacitor (C_H)	300			pF
Reference Current (I_R)	12		50	μA
Analog Input Range	0		V_{REF}	V
Ramp Stop Output Current			1.6	mA

*$2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$

CHANNEL SELECTION

INPUT ADDRESS LINE			SELECTED ANALOG INPUT
A_2	A_1	A_0	
0	0	0	Ground
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

ELECTRICAL CHARACTERISTICS: Over recommended operating conditions, -55° C ≤ T_A ≤ +125° C, for μA9708DM and 0° C ≤ T_A ≤ +70° C for μA9708DC or μA9708PC; unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Conversion Accuracy	E_A	Over entire temperature range (Note 1)		±0.2	±0.3	%
Linearity	E_R	Applies to any one channel (Note 2)		±0.08	±0.2	%
Multiplexer Input Offset Voltage	V_{OSM}	Channel ON		2.0	4.0	mV
Conversion Time Per Channel	t_C	Analog Input = 0v to V_{REF} C_H = 300 pF, I_{REF} = 50 μA		296	350	μs
Acquisition Time	t_A	C_H = 1000 pF		20	40	μs
Acquistion Current	I_A		150			μA
Ramp Start Delay Time	t_O			100		ns
Multiplexer Address Time	t_M			1.0		μs
Digital Input HIGH Voltage	V_{IH}	A_0, A_1, A_2, ramp start	2.0			V
Digital Input LOW Voltage	V_{IL}	A_0, A_1, A_2, ramp start			0.8	V
Analog Input Current	I_B	Channel ON or OFF	-3.0	-1.0		μA
Input LOW Current	I_{IL}	A_0, A_1, A_2, ramp start = 0.4 V	-15	-5		μA
Input HIGH Current	I_{IH}	A_0, A_1, A_2, ramp start = 5.5 V			1.0	μA
Input Offset Current	I_{OS}			1.0	3.0	μA
Comparator Logic "1" Output Leakage Current	I_{OH}	V_{OH} = 15 V			10	μA
Comparator Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Power Supply Rejection Ratio	PSRR	(Note 3)	40			dB
Crosstalk Between Any Two Channels		(Note 4)	60			dB
Power Supply Current	I_{CC}	V_{CC} = 5 V to 15 V, I_0 = 0		7.5	15	mA
Input Capacitance	C_{IN}			3.0		pF
Comparator Output Capacitance	C_{OUT}			5.0		pF

NOTES:
1. Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.
2. Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.
3. Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.
4. Crosstalk between channels = 20 log $\frac{\Delta V_{CH}}{\Delta V_i}$

FUNCTIONAL DESCRIPTION

This Analog to Digital Converter is a single-slope 8-bit, 6-channel A/D converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

For applications that require auto-zero or auto-calibration, *(See Figures 2-5)* line select address 0, 0, 0 and 1, 1, 1 may be used in conjunction with the arithmetic capability of the microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1 internally connects the input of the ramp generator, to the voltage reference, V_{REF}, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I_1-I_6 and the specific analog input to be converted is selected via address terminals A_0-A_2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 *(See Figure 1)*. The time to charge the capacitor is the acquisition time

which is a function of the output impedance of an amplifier internal to the A/D and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the A/D. Connected to the capacitor terminal is a comparator internal to the A/D with its output going to the ramp stop terminal (pin 7). The comparator output is a logical one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is the time from when ramp start goes high (logic "1") to when ramp stop goes low (logic "0"). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows.

$$\text{Ramp Time} = V_1 \frac{C_H}{I_R}$$

Where V_1 = Analog Input Voltage being measured

C_H = External Ramp Capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

Where V_{CC} = Power Supply Voltage

V_{REF} = Reference Voltage

R_{REF} = Reference Resistor

In actual use the errors due to a nonideal A/D can be minimized by using a microprocessor to make the calculations. *(See Figures 2 through 5)*

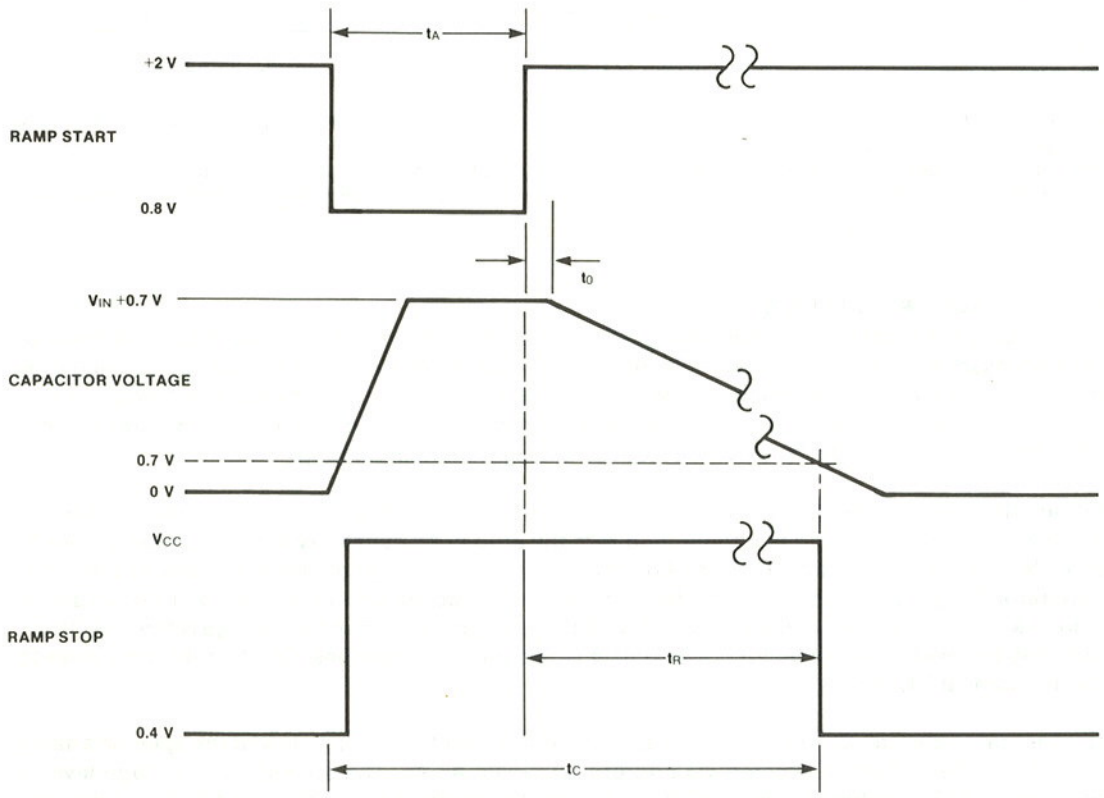
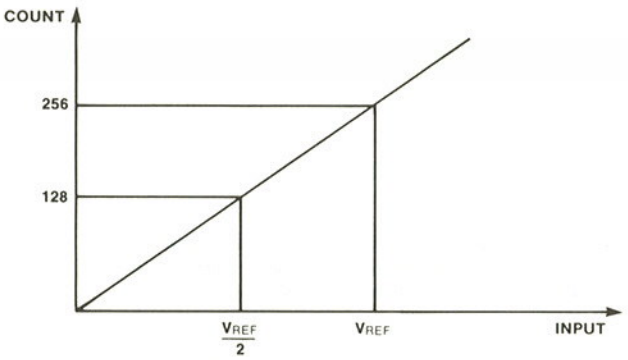


Fig. 1 Equivalent Timing Waveform for Test Circuits and Applications

APPLICATION HINTS AND FORMULAS

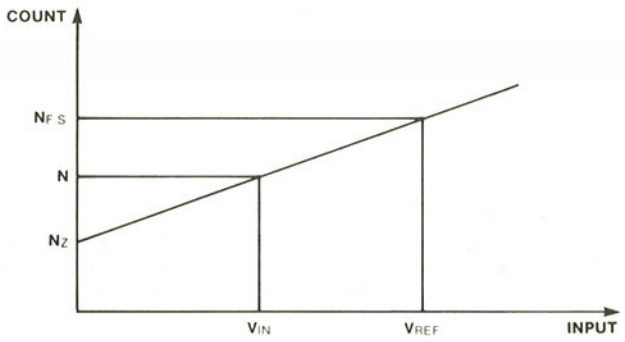
1. The capacitor node impedance is approximately 30 μΩ and should have no parallel resistance for proper operation.
2. t_R when $V_{IN} = 0$ V will be finite (i.e., the comparator will always toggle for $V_{IN} \geq 0$ V.)
3. The ramp stop output is open collector, and an external pull up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. $t_A \geq \frac{C_H}{150\ \mu A - I_R} \times V_{REF}$
7. t_R (ramp time) $= \frac{C_H}{I_R} \times V_{IN}$, $t_R\big|_{max} = \frac{C_H}{I_R} \times V_{REF}$
8. $I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$
9. $2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$
10. Address lines A_0, A_1, A_2 must be stable throughout the sampling interval, t_A.
11. Pin 6 (R_{REF}) should be bypassed to ground via a 0.02 μF capacitor.

AUTO-ZERO AND FULL-SCALE FEATURES



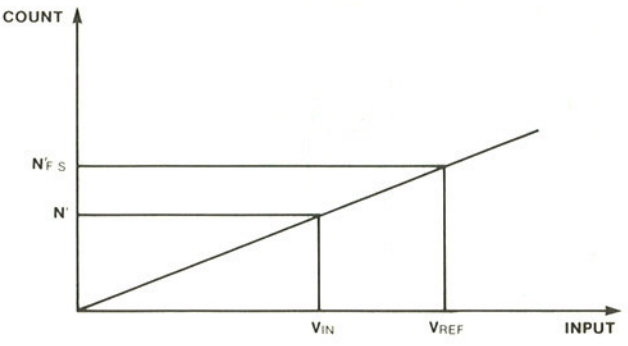
- NO ZERO OFFSET
- NO FULL-SCALE ERROR
- COUNT (N) = $\frac{V_{IN}}{V_{REF}} = 256$

Fig. 2 Ideal Transfer Function



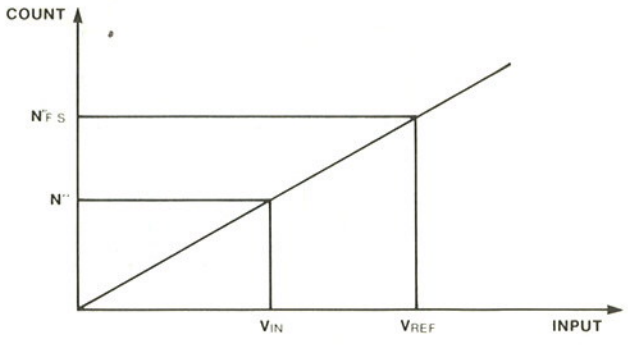
- $N_{F.S.} \neq 256$
- $N_Z \neq 0$
- (N) HAS BOTH FULL-SCALE AND ZERO ERRORS

Fig. 3 Transfer Function with Zero and Full-Scale Error



- $N' = N - N_Z$
- N' HAS FULL-SCALE ERROR

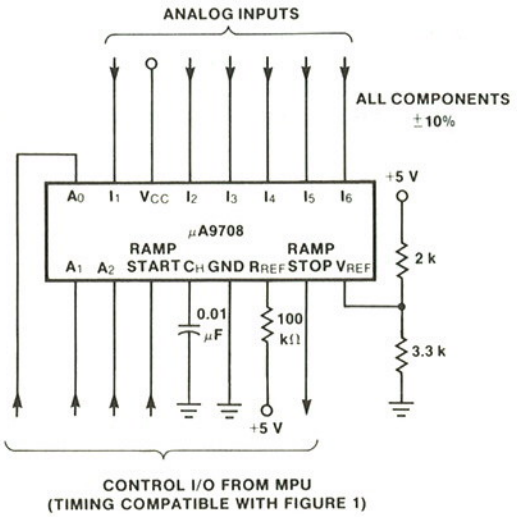
Fig. 4 Zero-Correction Added



- $N'' = (N - N_Z) \times \frac{256}{(N_{F.S.} - N_Z)}$

Fig. 5 Both Zero and Full-Scale Correction Added

TEST CIRCUITS



INPUT TIMING:

$t_A > 400\ \mu s$

$$V_{REF} = \left(\frac{3.3\ k\Omega}{2\ k\Omega + 3.3\ k\Omega}\right) 5\ V = 3.1\ V$$

$$I_R = \frac{5\text{-}3.1}{100\ k\Omega} = 19\ \mu A$$

$$t_R\Big|_{max} = \text{full scale ramp time} = \frac{0.01 \times 10^{-6}}{19 \times 10^{-6}} \times 3.1 = 1.6\ ms$$

NOTE:
For evaluation purposes, the ramp start timing generation can be implemented with a μA555 timer (astable operation) or MPU evaluation kit, and a time internal meter for ramp time measurement. The TIM meter will measure the time between the 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull up resistor to V_{CC}.

Fig. 6 Slow Speed Evaluation Circuit for Ratiometric Operation

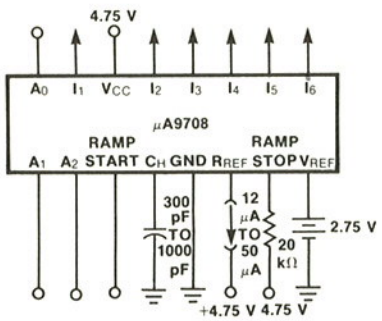


Fig. 7 Linearity/Acquisition Time/Conversion Time Test Circuit

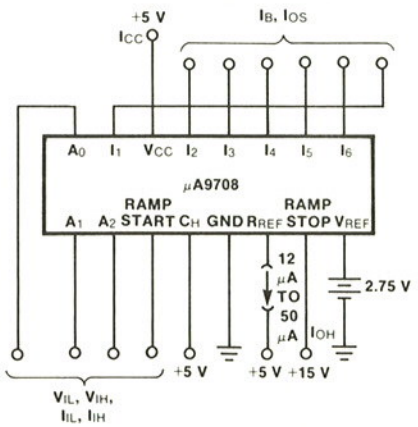
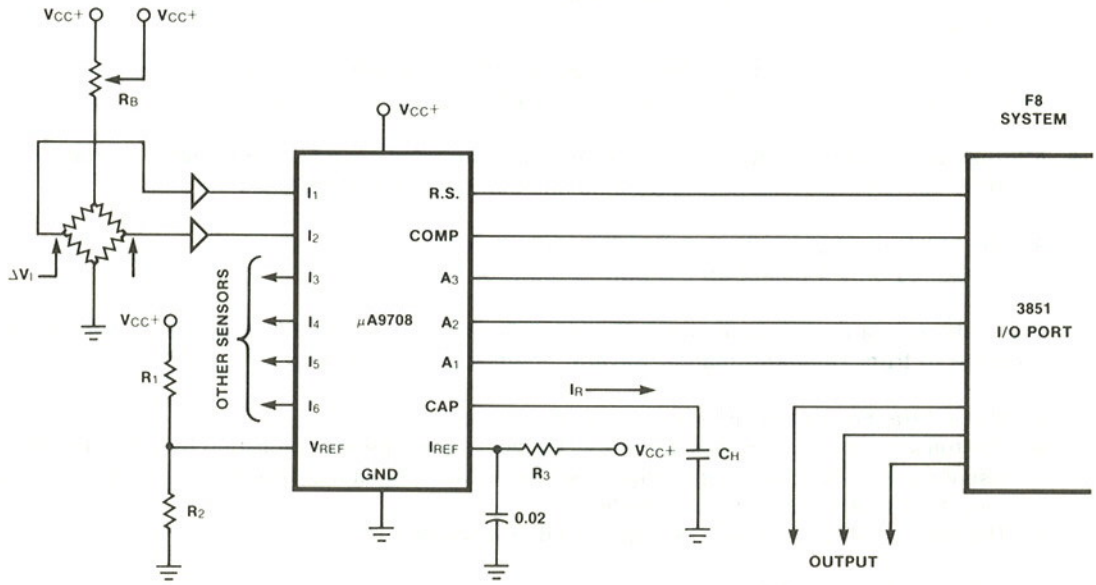


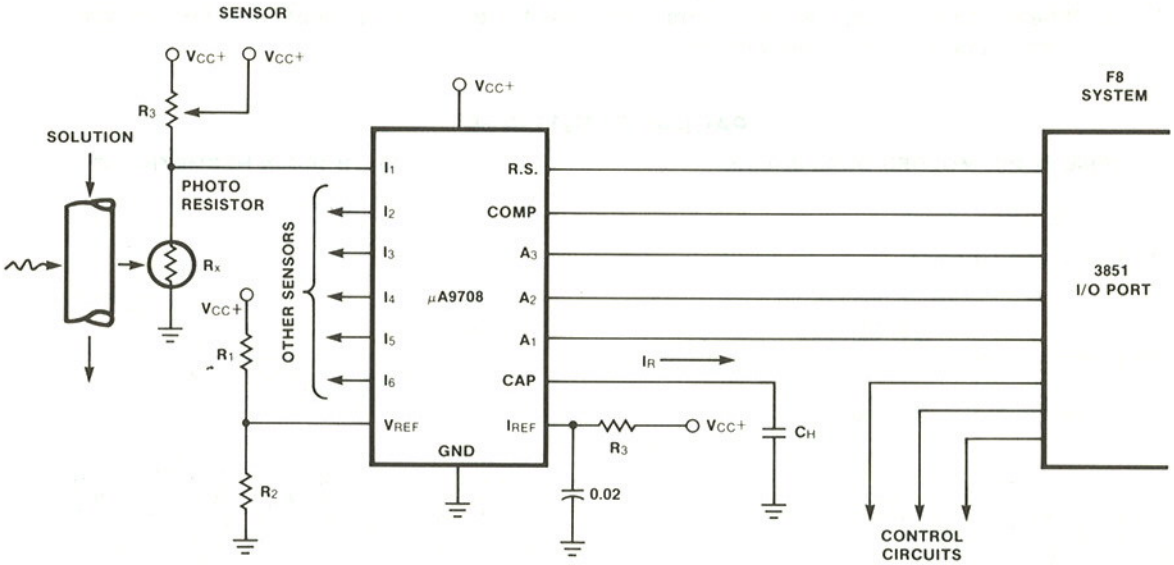
Fig. 8 Static Measurements

TYPICAL APPLICATIONS



ΔV_I = (Applied Force) and can be Linearized (if necessary) in F8 Software.

Ratiometric Strain Gage Sensor/Controller



APPLICATIONS:

- **BEVERAGE BREWERS/DISPENSERS**
- **CHEMICAL SOLUTION CONTROL**
- **AUTOMATIC LIQUID MIXING CONTROL**

$$\text{RAMP CURRENT} = I_R = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{1}{R_3}\right)$$

$$V_I = \left(\frac{R_X}{R_X + R_B}\right) V_{CC+}$$

$$\text{RAMP TIME} = V_I \frac{C_H}{I_R} = \left(\frac{R_X}{R_X + R_B}\right)\left(1 + \frac{R_2}{R_1}\right)\left(C_H R_3\right)$$

Opaque Solution Controller

SYSTEM HINTS:

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the μA9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.

2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:

   A. The CPU is not committed during the ramp time interval.
   B. It requires only 4 bits of an I/O port for control signals.

3. The auto-zero/auto-full-scale (see *Figures 2-5*) should use double precision, rounded (as opposed to truncated) arithmatics. Several points are worth noting:

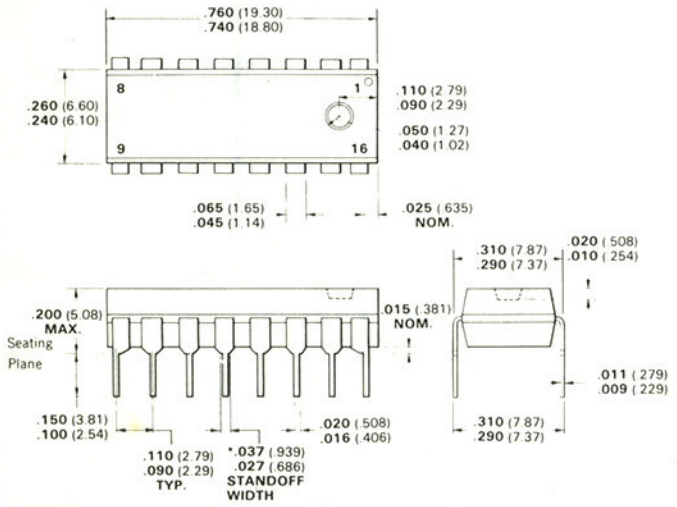
   A. The subtractions are single op code instructions.
   B. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing (N-Nz) in the MSB register and setting the LSB register to zero, for the double precision divide.
   C. The divisor ($N_{F.S.}$ - Nz) MSB's register will always be zero.

These schemes have the following advantages:

A. No access to the data buss or address buss is required, by the A/D system.
B. 4 I/O bits completely support the A/D system.
C. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
D. Software overhead is minimal (typically 30 bytes).
E. Where ratiometric operation is permissible, the 4 external components may be ±5% tolerance, including the power supply.

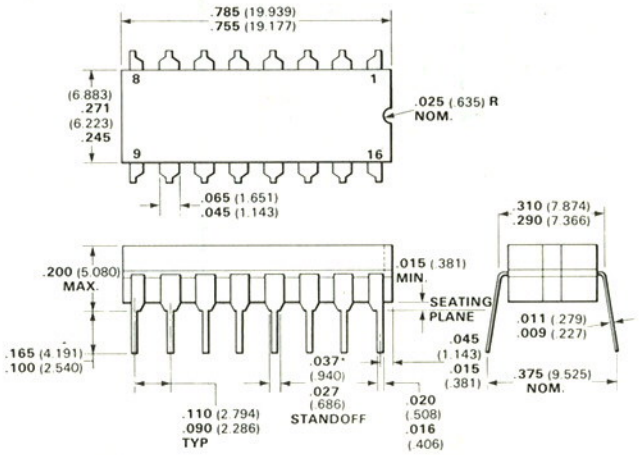
PACKAGE OUTLINES

(P)9B 16-PIN MOLDED DUAL IN-LINE



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
*The .037/.027 dimension does not apply to the corner pins
Package weight is 0.9 gram

(D) 7B 16-PIN HERMETIC DIP



NOTES:
All dimensions in inches
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Hermetically sealed alumina package
*The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams