1984
Storage Management
Products Handbook

Making The Leading Edge Work For You.

This handbook is designed for you, the engineer. It's intended to be a useful tool, enabling you to make a preliminary evaluation of our products and later, with samples in hand, design our products into your own systems.

The data in these pages have been reviewed by our Marketing, Engineering, Manufacturing, and Quality groups. Now we would like you to review the information we've provided and tell us how we can improve it. Please feel free to suggest any changes, additions, or clarifications that occur to you. And don't hesitate to call to our attention any sins of omission or commission we may have made.

We're eager to help upgrade the quality of information our industry provides to its customers. So, please, help us. Direct your comments to:

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Advance Information: This product has not been produced in volume and is subject to functional and timing revisions. Prior to designing with the product, it is necessary to contact Western Digital Corporation for current information.

Preliminary: This product is in limited production and may be subject to change after device characterization has been completed. Prior to designing with the product, it is necessary to contact Western Digital Corporation for current information.

Data sheets without one of the above headings are in full production and intended for normal commercial applications. For military, extended temperature, burn-in, or hi-rel applications, contact Western Digital Corporation for information regarding further processing.

Functional Index

STORAGE MANAGEMENT PRODUCTS

WINCHESTER BOARD PRODUCTS

MAIN MEMORY DEVICES

Numerical Index

WESTERN DIGITAL
CORPORATION

System Product Quality/Reliability

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown on the attached organization chart (Figure 2) reports directly to the President of Western Digital. It assures compliance to design control, quality and reliability specifications pursuant to corporate policy. Quality assurance provisions are derived in part from MIL-Q-9858, as applied to high grade commercial products.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution of the quality program rests with functional organizations to design, produce, and market high quality and high reliability products specified to our customers.

DESIGNING FOR RELIABILITY

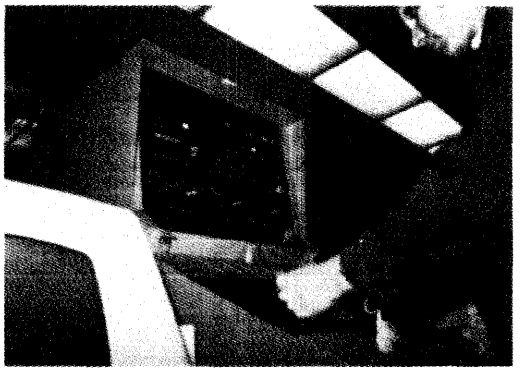
The premise upon which board and system manufacturing operations are based is that quality is planned and designed-in, not screened-in or selected. A well-tested, high-quality design is far more reliable than a marginal design with any amount of burn-in or fixes. To assure top quality design, Western Digital maintains one of the most experienced board/system design staffs in the industry. A tightly controlled design review team comprising members from Quality Assurance, Marketing, Manufacturing and several experienced design engineers, provides review of each new design several times during its development to ensure widest possible performance margins. The production release procedure assures a checklist for:

- Test Method/Program Qualifications
- Characterization Report
- Field Test (Beta Test) Report
- Product Qualification Audit
- Documentation Package Release for Document Control
- Software/Diagnostics Qualification

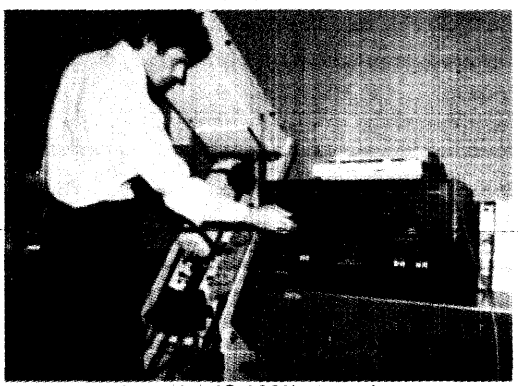
MAINTAINING QUALITY/RELIABILITY IN PRODUCTION

The Quality Control Testing Flow Chart shown on Figure 1 defines the exact stages contained in the production process. Internally manufactured LSI components undergo 100% testing at maximum specified operating temperatures as well as strict quality controls defined to assure high quality and reliability. Components not designed and manufactured by Western Digital are also 100% screened as shown in photos during incoming inspection at 70°C. The tests performed include selective active component burn-in performed at 125°C for 160 hours to insure guaranteed levels of reliability. This 125°C accelerated testing eliminates defects that cannot effectively be accelerated by burning-in boards and systems which have temperature limitations. Key quality control procedures include:

- Incoming Inspection Procedure
- In-Process Travel Card Traceability
- Workmanship Standards
- Quality Corrective Action Notice/MRB Procedure
- Quality Audit Procedure



Bare board test

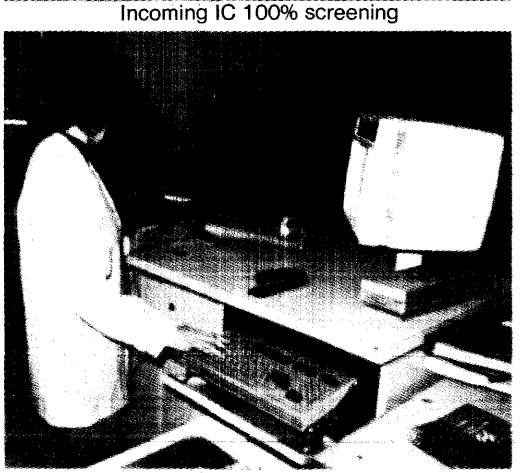


Incoming IC 100% screening

PRODUCT FINAL TEST/CORRECTIVE ACTION

All boards are 100% in-circuit tested and 100% functional tested for acceptable performance according to applicable test specifications on testers qualified by QA. Products are tested at maximum specified temperature and voltage margins using diagnostic software to ensure greater performance margins. Failures are logged on a travel card specifically designed to insure traceability to manufacturing steps and to maintain failure records for QA corrective action.

If the board is designed to perform in a host system, further diagnostics are performed in an environment configured to actual customer requirements.



In-circuit test

PRODUCT ACCEPTANCE

Upon completing the final test, the board/system undergoes QC final workmanship standards inspection and selective samples are audited to the functional product specification to guarantee quality at specified operating margins to the customer.

Complete documentation available for you at our facility.

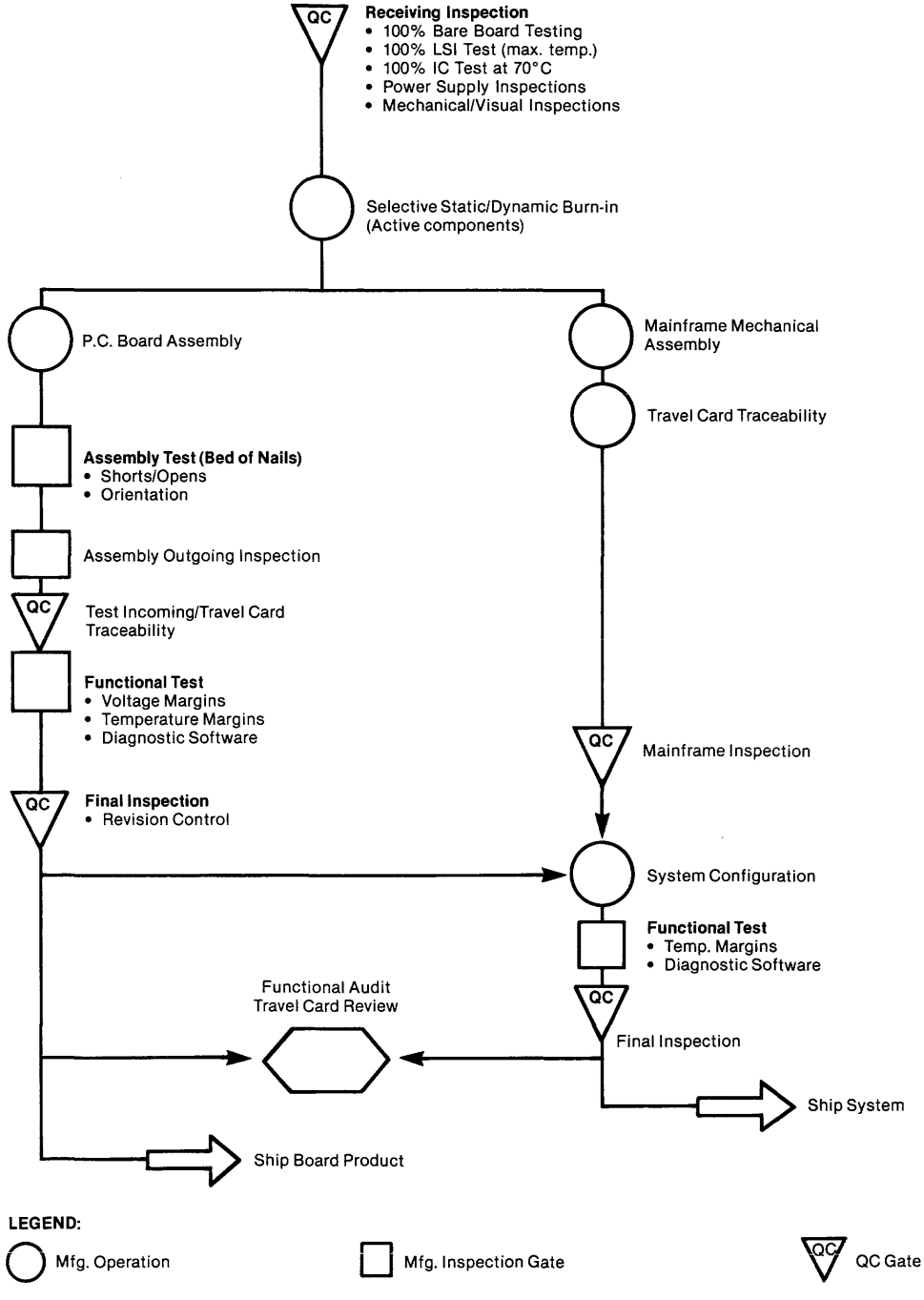


Figure 1. QUALITY CONTROL TESTING FLOW CHART

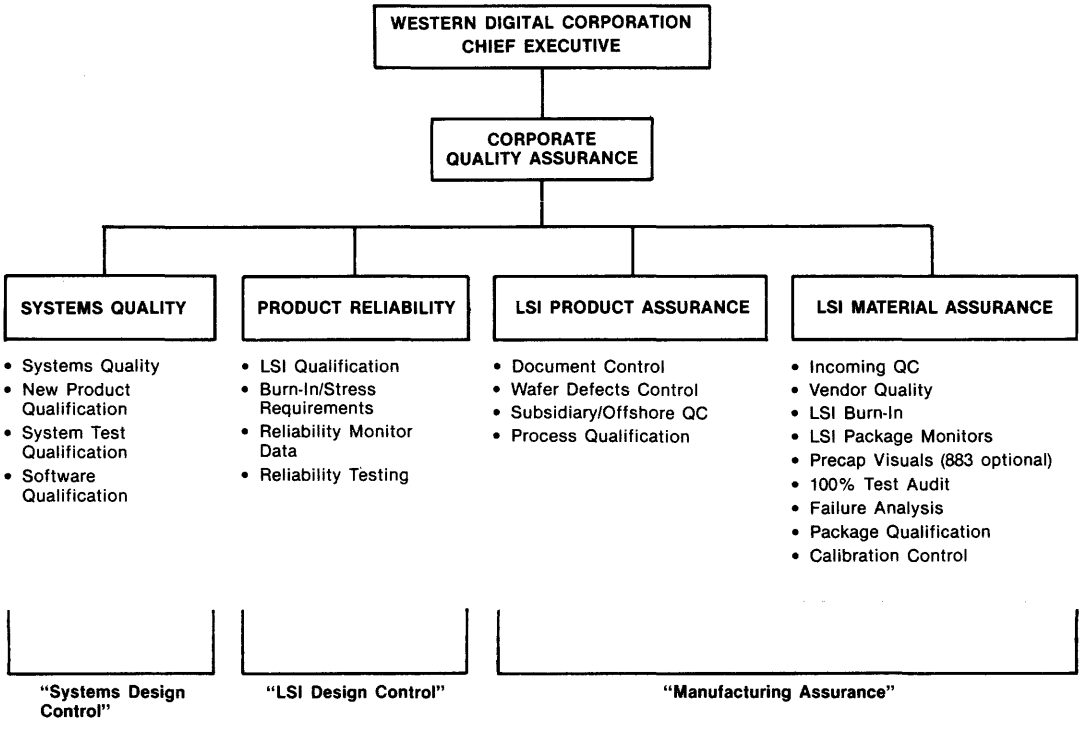


Figure 2. QUALITY ORGANIZATION

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Quality/Reliability To Leading Edge Technology

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown in Figure 2 assures compliance to design control, quality and reliability specifications, pursuant to corporate policy.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution for the quality program rests with functional organizations to design, produce and market high quality and high reliability products specified to our customers.

LSI QUALITY ASSURANCE PROGRAM HIGHLIGHTS

- LSI manufacturing assurance provisions are derived in part from MIL-M-38510 and MIL-STD-883B as applied to high grade commercial components.
- All process raw materials used in the Mask/Wafer fabrication and assembly operations are monitored by Material Assurance.
- Material Assurance maintains a thorough control of incoming material and has developed unique "use/stress tests" (look ahead sample build acceptance) which critical material must pass before acceptance.
- The Product Assurance Department continuously monitors the internal and external manufacturing flow (shown in Figure 1) and issues process control reports displaying detailed data and trends for the associated areas.
  - — Document control is an integral part of Product Assurance. All specifications are issued and controlled by this activity.
  - — The Western Digital Malaysian assembly operation uses specifications and quality control provisions controlled by Document Control. Indicators of Malaysia quality are reviewed weekly.
  - — Purchased FAB and assembly operations are individually qualified and are certified against standard specifications during vendor qualification and monitored against reliability criteria.
  - — Defect control within the process assures the highest levels of built-in reliability.
- Quality audits and gates are located throughout the manufacturing process in order to assure a stable process and thus, a quality product to our customers. Figure 1 illustrates the manufacturing/screening/inspection flow diagram and identifies the steps as they relate to the production of LSI devices.
- Testing assures quality margins through 100% testing by manufacturing and, in addition, all products must pass a specified AQL sample test performed by QA at maximum operating temperature as follows:

Outgoing Quality Levels

SUBGROUPS	INSPECTION LEVEL
Subgroup 1 — Final 100% Electrical Audit @ Max °C	0.5 AQL*
Subgroup 2 — Visual (Marking, Lead Integrity, Package, Verify customer shipper)	1.0 AQL
Subgroup 3 — Shipping Visual Audit	1.0 AQL

*The double sampling techniques used allow considerably better AQL's in most all cases.

- LSI devices are 100% tested on industry standard test systems like that shown below. Quality outgoing testing (auditing) is done on the Fairchild Sentry Series 20 where possible to allow better correlation with customers.

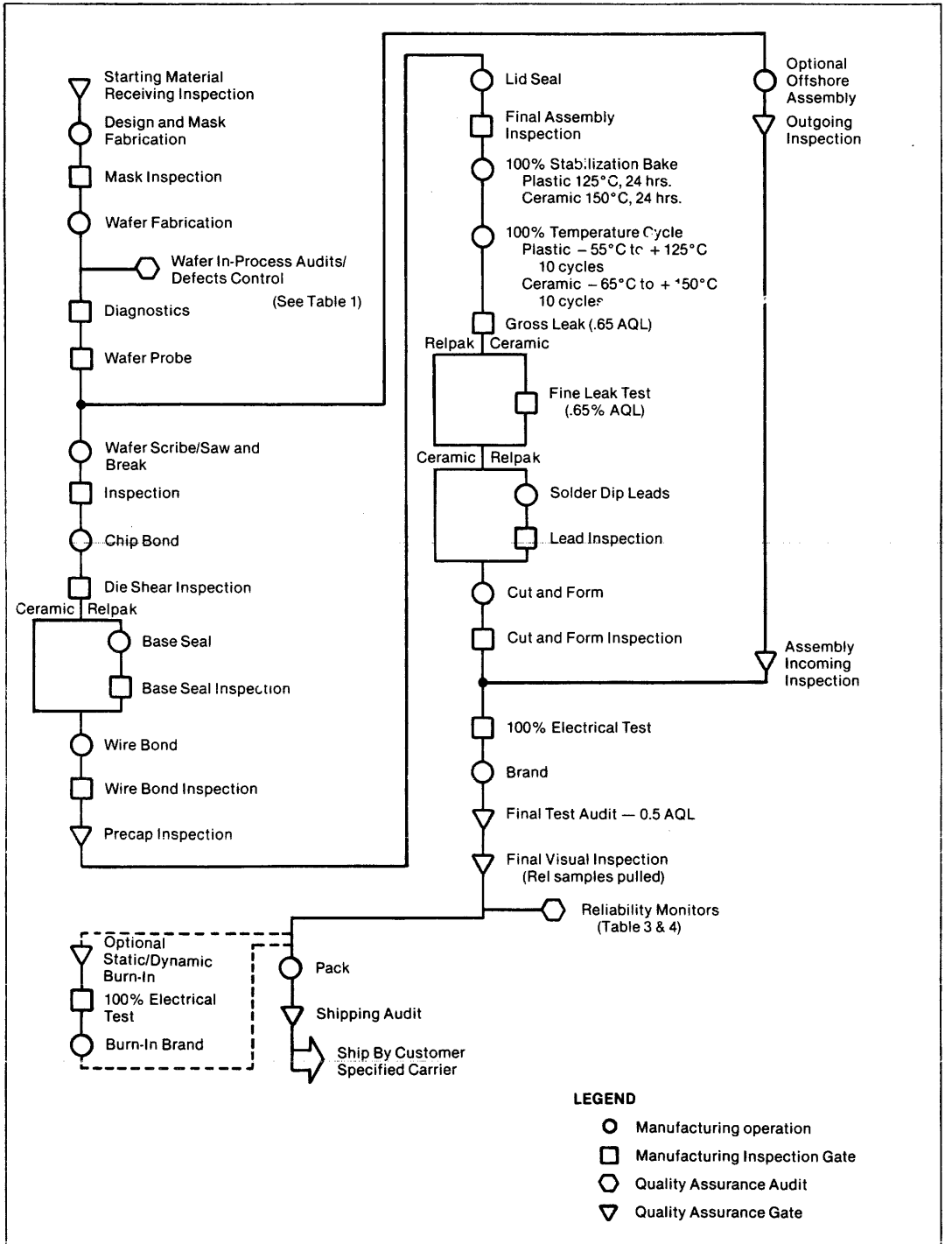


Figure 1 LSI PRODUCTION FLOW

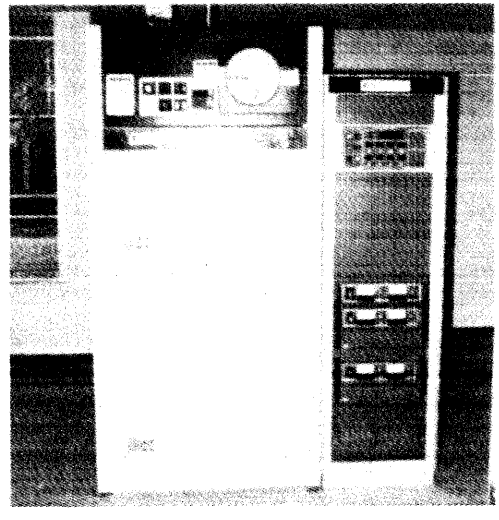
Reliability Means Lasting Value

• DESIGNING FOR RELIABILITY

The production release procedure for an LSI device is designed to assure maximum reliability with a Quality checklist for:

- Test program qualifications
- Characterization report
- Field test (Beta Test) report
- Reliability Lifetest Qualifications
- Infrared Thermal Analysis
- Static Protection

All new devices and major process changes must pass reliability qualification before incorporation into production using the criteria defined in Tables 2-4. The infrared microscope shown on the right assures optimum burn-in temperatures and margins of safety. The dynamic burn-in system shown on the right is one of two custom designed systems which assure protective device isolation during burn-in.



• MAINTAINING RELIABILITY IN PRODUCTION

Process defects control are defined to continually measure built-in reliability, as measured by the following criteria:

TABLE 1

PROCESS RELIABILITY CONTROL	METHOD	CONDITION	SAMPLE*
Subgroup 1 — Defects Control			
a. Oxide Integrity	Non-destructive bubble test	Pinhole defect density	5 wafers
b. Polysilicon Integrity	SEM Analysis	Visual	5 wafers
Subgroup 2 — Electro-Migration Control			
Metal Step Coverage	MIL-STD-883 Method 2018	SEM Analysis	5 wafers
Subgroup 3 — Defect Density	Critical layers Field Gate Contact Metal	Visual of Photo defects (Defects/in^2)	8 wafers each layer
Subgroup 4 — Passivation/Insulation Integrity	MIL-STD-883 Method 2021	Visual of Pinhole defect density	Final Silox 5 wafers Intermediate 5 wafers

*Inspection intervals are defined by the in-line process control data reviewed on a lot-by-lot basis.

• PROGRAMS TO ASSURE OPTIMUM RELIABILITY

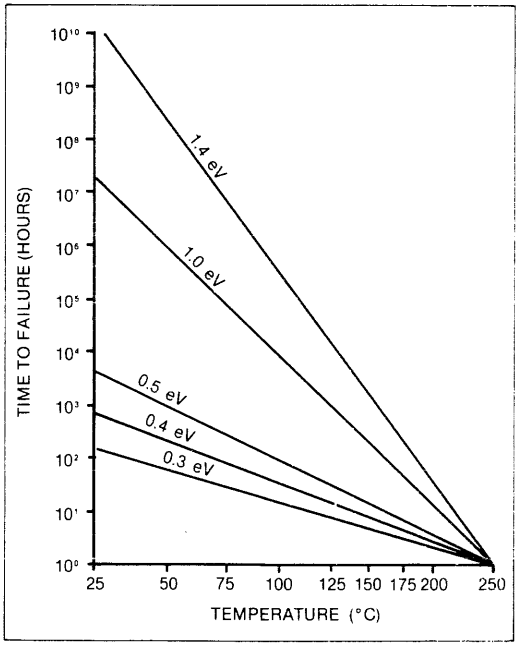
Improved levels of reliability are available under custom reliability programs using static and dynamic burn-in to further improve reliability. These programs focus on MOS failure mechanisms as follows:

FAILURE MECHANISMS IN MOS

FAILURE MECHANISM	EFFECT ON DEVICE	ESTIMATED ACTIVATION ENERGY	SCREENING METHOD
Slow Trapping	Wearout	1.0 eV	Static Burn-In
Contamination	Wearout/ Infant	1.4 eV	Static Burn-In
Surface Charge	Wearout	0.5-1.0 eV	Static Burn-In
Polarization	Wearout	1.0 eV	Static Burn-In
Electromigration	Wearout	1.0 eV	Dynamic Burn-In
Microcracks	Random	—	100% Temp. Cycling
Contacts	Wearout/ Infant	—	Dynamic Burn-In
Oxide Defects	Infant/ Random	0.3 eV	Dynamic Burn-In at max. voltage
Electron Injection	Wearout	—	Low Temp. Voltage Operating Life

Temperature Acceleration of Failure

The Arrhenius Plot defines a failure rate proportional to exp(– Ea/kt) where Ea is the activation energy for the failure mechanism. The figure on the right indicates that lower activation energy failures are **not** effectively accelerated by temperature alone; hense, maximum voltage operation is selectively applied to optimize the burn-in process.



Static Burn-In (125°C — 48 hours or 160 hours)

Provided on a sample basis for process monitor/control of 0.5 eV — 1.0 eV failure mechanisms. 100% static burn-in may be specified at an additional cost. However, static burn-in is considered only partially effective for internal LSI gates at logic "O" levels.

Dynamic Burn-In (Pattern test/125°C — 8 hours to 160 hours)

Accelerated functional dynamic operating life effectively controls internal MOS gate defects buried from external pin access. The input pattern is optionally pseudo-random or fixed pattern programmable to simulate 1000-3000 hours of field operation at maximum operating voltage(s).

High-Rel "K" Testing Program

General conformance to MIL-STD-883B method 5004.4, Class B with static Burn-In (Dynamic Burn-In may be specified as an option).

LSI RELIABILITY STANDARDS

TABLE 2 STANDARD RELIABILITY LEVELS

TEST	METHOD	CONDITION	FAILURE
Infant Mortality (see note)	Static Burn-In	125°C — 160 hrs.	<0.5%
Long Term Failure Rate	Dynamic Life Test	125°C — 1000 hrs.	<.05%/1000 hrs. @ 55°C 60% Confidence

*NOTE: Devices failing the infant mortality target remain on burn-in until acceptable failure rates are obtained.

TABLE 3 GROUP A DEVICE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Internal Visual			15
b. Thermal Shock	1011	Test Failure Used (cond. B or C)	
c. Bond Strength	2011	Test Failures (cond. B)	
d. Die Shear Strength	2019	Test Failures	
Subgroup 2			
a. Seal — Gross Leak		Fluorocarbon detection 10^{-3} atm/cc/sec	15
b. Seal — Fine Leak	1014	Test Condition A	
Subgroup 3			
a. Rotating Steady State Life Test	1005	Static 160 hr. Burn-In 125°C plus 125°C Lifetest — 1000 hrs.	5
b. Electrical Parameters	—	Final electrical @ 25°C (with data @ 70°C)	

TABLE 4 GROUP B PACKAGE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Thermal Shock	1011	Test Condition B or C	15
b. Temperature Cycling	1010	Test Condition B or C	
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Electrical at max -C	
f. 85/85 Moisture Resistance (plastic only)	—	85% RH/85°C for 1000 hours PDA = 10%	
g. Electrical Parameters	—	Final electrical @ 25°C	
Subgroup 2			
a. High Temp. Storage	1008	Test Condition B or C	
b. Mechanical Shock	2002	Test Condition B	15
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Final electrical @ 25°C/max. C	
Subgroup 3			
a. Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
b. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
c. Seal — Fine Leak (ceramic)	1014	Test Condition A	

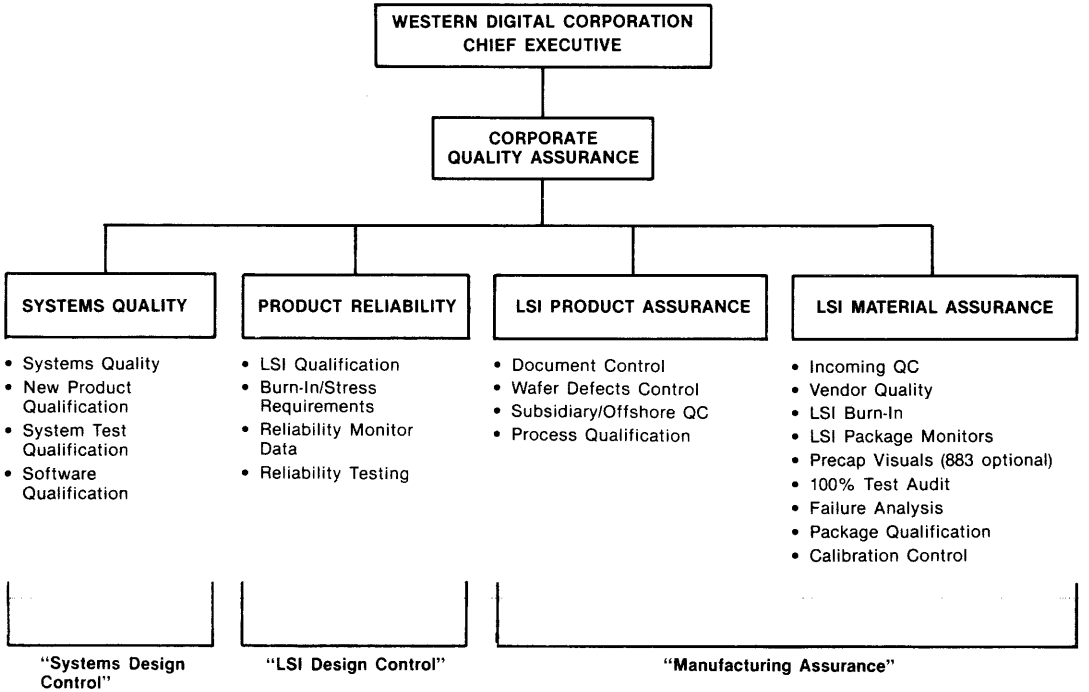


Figure 2 QUALITY ORGANIZATION

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Announcing Burn-In Program Availability/Warranties

Western Digital now supports customer burn-in requirements for both static and dynamic burn-in under the strict control of the QA-Reliability organization.

This burn-in provides high performance 125°C static and dynamic burn-in for 8-160 hours to eliminate infant mortality and improve reliability. This process is executed using custom modified 32Bit AEHR test commercial burn-in equipment which provide monitored fixed pattern or pseudorandom burn-in with power supply and resistor device pin isolation.

LSI dynamic burn-in is verified in all cases by the design engineer for proper functioning. LSI Chip sets are also individually burned-in with dynamic equivalency to assure high performance bundled reliability.

The warranty on the program will optionally provide certificate of compliance to standard or custom designed burn-in programs and guarantee <.05%/Khrs failure rate.

CAUTION

Using outside burn-in methods not certified as acceptable by Western Digital may result in voided warranty, due to mishandling, junction temperature stress, or electrical damage. Further, since most burn-in houses do not support testing, catastrophic system condition can result in substantial damage before a problem is identified.

One consistent problem experienced with outside LSI burn-in houses can cause reliability problems; namely, parallelling totem pole MOS outputs, where the output states are not predictable, can cause a single (or a few) device(s) to sink all the current from the other devices on the burn-in tray — electromigration or current zaps are both possible.

Western Digital burn-in diagrams, dated after 1/1/82, must be used exactly as shown and will be provided upon request.

SEE YOUR LOCAL REPRESENTATIVE FOR COSTS AND ORDERING INFORMATION ON THIS NEW PROGRAM.

Hi-Rel "K" Testing Program

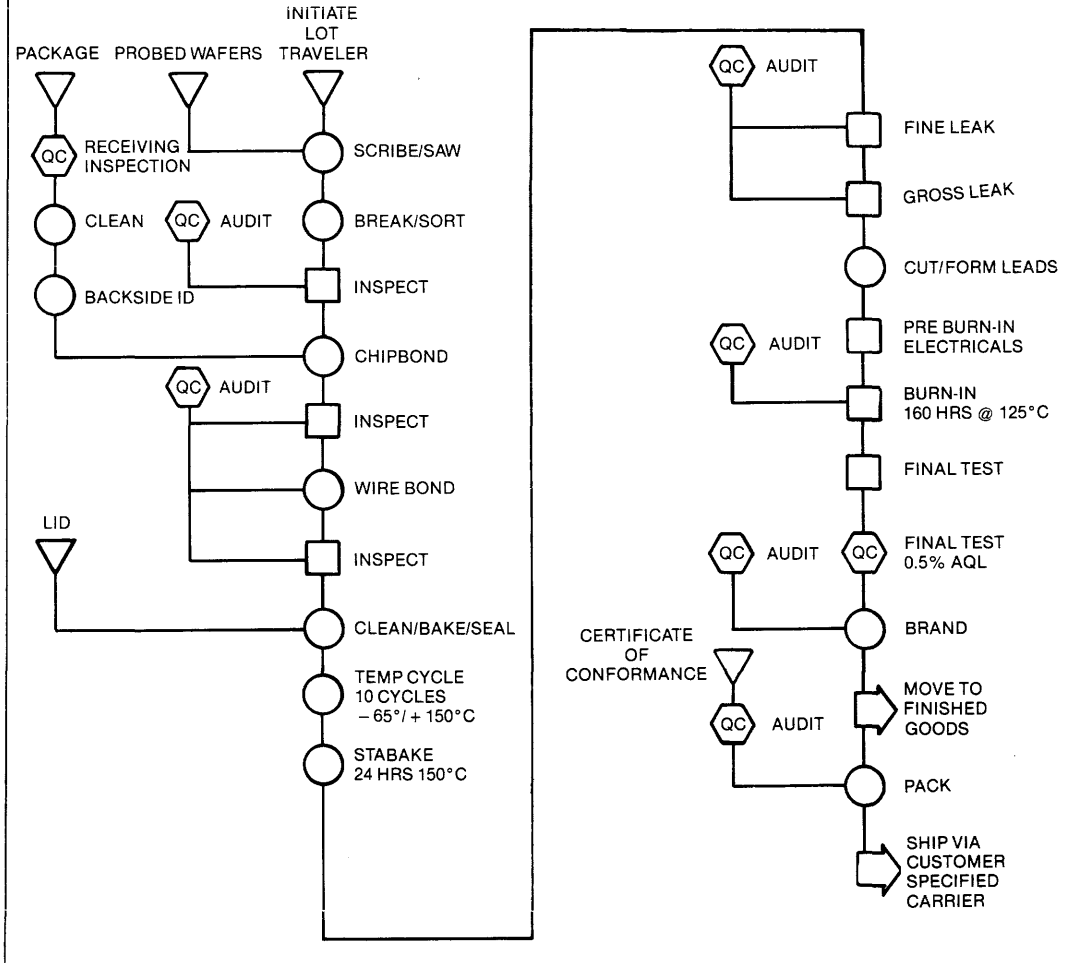
FEATURES

GENERAL CONFORMANCE TO MIL-STD-883B, METHOD 5004.4, CLASS B (SEE COMPARISON ON FOLLOWING PAGES)

- INCLUDES:
  - PRECAP VISUALS
  - SEAL INTEGRITY
  - POWER CONDITIONING
  - ENHANCEMENT OPTIONS

GENERAL DESCRIPTION

Western Digital's Hi-Rel "K" program is designed to provide high reliability devices for extended temperature environments. Individual enhancements may be specified to meet a customer's requirements.



HI-REL "K" PROGRAM FLOW DIAGRAM

COMPARISON OF MIL-STD-883 AND HI-REL "K" TEST PROGRAM

MIL-STD-883B, METHOD 5004.4, CLASS B	HI-REL "K" TEST
3.1.1 Internal Visual Method 2010.3 Test condition B	All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.
3.1.2 Stabilization Bake Method 1008.1 Test condition C 24 hours at 150°C	Same
3.1.3 Temperature Cycling Method 1010.2, Test condition C −65°C to 150°C for 10 cycles, with 10 minutes dwell and 5 minutes maximum transfer time	Same
3.1.4 Constant Acceleration Method 2001.2, Test condition E. 30,000 G stress level	Not Done Unless Specified
3.1.5 Visual Inspection Visual inspection for catastrophic failures after screens	Same
3.1.6 Seal Method 1014.2 (a) Helium fine leak — Test condition A_1. Bomb condition 2 hours at 60 psig. Reject limit 5×10^{-8} torr	Same
(b) Flourocarbon gross leak — Test condition C	Same
3.1.9 Interim (pre-burn-in) Electricals Per applicable device specification	Preburn-in test at 25°C. Must meet requirements of device data sheets.
3.1.10 Burn-in Test Method 1015.2 160 hours @ 125°C	Same
3.1.13 Interim (Post burn-in) electricals Per applicable device specification	Burn-in equipment isolate failures automatically to assure no harmful interaction.
3.1.15 Final Electrical Test (a) Static Tests (1) 25°C (2) Minimum and Maximum Operating Temperatures (b) Dynamic and Switching Tests at 25°C (c) Functional Tests at 25°C	Same
3.1.17 Qualification or Quality Conformance Inspection and Test Sample Selection	Not done unless defined using method 5005 as a guide.
3.1.18 External Visual Method 2009.2	Same

WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS

100% Temperature Testing

Level ..... −40° to +85°C
..... −55° to +125°C

Thermal, Shock (Liquid to Liquid)

Level..... 0° to +100°C, 15 cycles
..... −55° to +125°C
..... −65° to +150°C

Extended High Temperature Storage

+150°C for 24 hours standard, other time/temperature storage requirements available as required.

Dynamic Burn-In

Per note previously supplied.

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FD1771-01 Floppy Disk Formatter/Controller

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- READ MODE
  - Single/Multiple Sector Write with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- PROGRAMMABLE CONTROLS
  - Selectable Track-to-Track Stepping Time
  - Selectable Head Settling and Head Engage Times
  - Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8-Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE

SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER

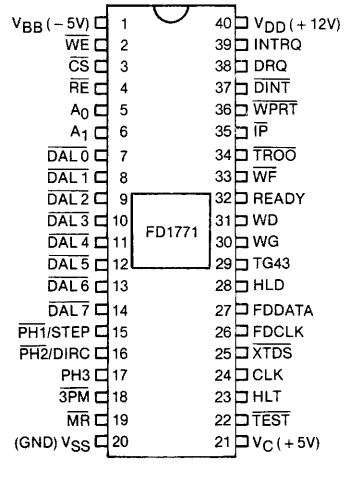
NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

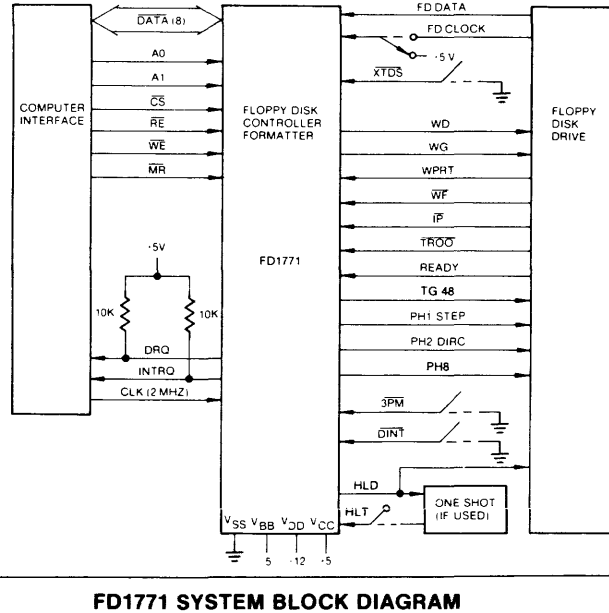
The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The A and B suffixes are for ceramic and plastic packages, respectively.



PIN DESIGNATION



FD1771 SYSTEM BLOCK DIAGRAM

PIN OUTS

Pin No.	Pin Name	Symbol	Function
1	Power Supplies	V_{BB}/NC	-5V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high, a Restore Command is executed, regardless of the state of the Ready signal from the drive.
20		V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
Computer Interface			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A_0, A_1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A_1 A_0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Register Command Register 0 1 Track Register Track Register 1 0 Sector Register Sector Register 1 1 Data Register Data Register
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
24	CLOCK	CLK	This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
Floppy Disk Interface:			
15	Phase 1/Step	$\overline{PH1}$/STEP	If the $\overline{3PM}$ input is a logic low the three-phase motor control is selected and $\overline{PH1}$, $\overline{PH2}$, and PH3 outputs form a one active low signal out of three. $\overline{PH1}$ is active low after $\overline{MR}$. If the $\overline{3PM}$ input is a logic high the step and direction motor control is selected. The step output contains a 4 usec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
16	Phase 2/Direction	$\overline{PH2}$/DIRC	
17	Phase 3	PH3	
18	3-Phase Motor Select	$\overline{3PM}$	

Pin No.	Pin Name	Symbol	Function
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user.
23	HEAD LOAD TIMING	HLT	The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
25	$\overline{\text{EXTERNAL DATA SEPARATION}}$	$\overline{\text{XTDS}}$	A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	This input receives the externally separated clock when $\overline{\text{XTDS}}$ = 0. If $\overline{\text{XTDS}}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	This input receives the raw read disk data if $\overline{\text{XTDS}}$=1, or the externally separated data if $\overline{\text{XTDS}}$=0.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	Track Greater than 43	TG43	This output informs the drive that the Read-Write head is positioned between tracks44-76. This output is valid only during Read and Write commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
31	WRITE DATA	WD	This output contains both clock and data bits of 500 ns duration.
32	Ready	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects wiring faults indications from the drive. When WG=1 and $\overline{\text{WF}}$ goes low, the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write command is received. A logic low terminates the command and sets the Write Protect status bit.
37	$\overline{\text{DISK INITIALIZATION}}$	$\overline{\text{DINT}}$	The iput is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$=0, the operation is terminated and the Write Protect status bit is set.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register: This 8-bit register assembles serial data from the Read Data input (FDDATA) duriing Read operations and transfers serial data to the Write Data output during Write operations.

Data Register: This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register: This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

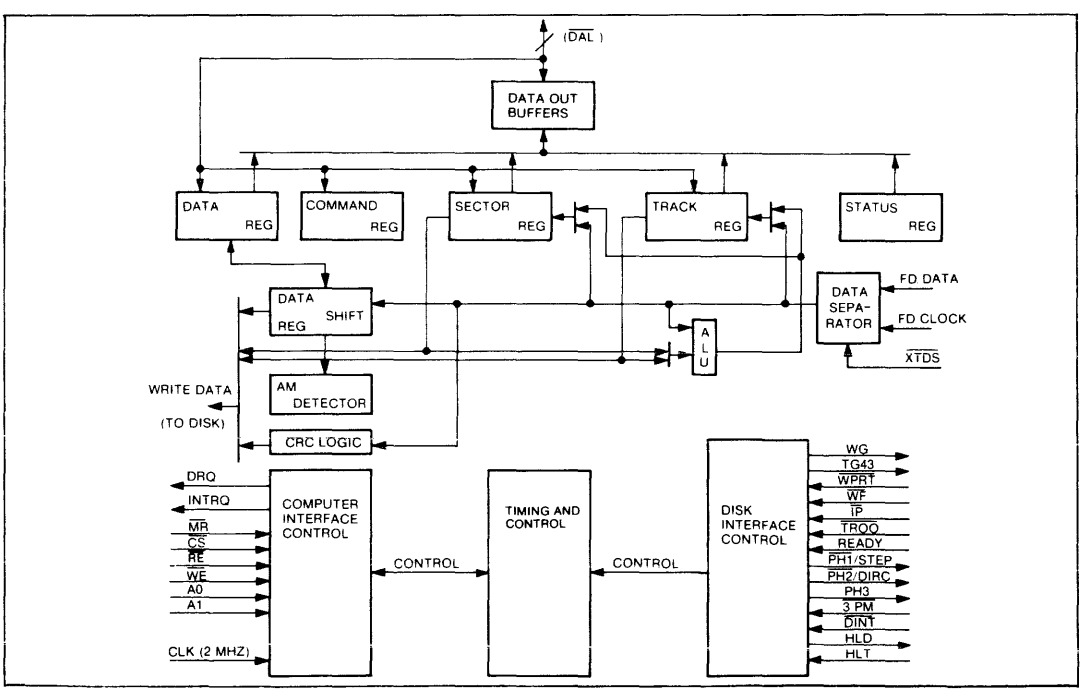
Sector Register (SR): This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR): This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR): This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic: This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.



FD1771 BLOCK DIAGRAM

Arithmetic/Logic Unit (ALU): The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector: The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control: All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three-state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the Processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is requred at the CLK input for internal control timing (may be 1.0 MHz for mini floppy).

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three-Phase Motor or a Step-Direction Motor through the device interface. When the $\overline{3PM}$ input is connected to ground, the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals $\overline{PH1}$, $\overline{PH2}$, and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5V. The Phase 1 pin $\overline{PH1}$ becomes a Step pulse of 4 microseconds width. The Phase 2 pin $\overline{PH2}$ becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 μs prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not

made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

Table 1. STEPPING RATES

r_1 r_0	1771-X1 CLK = 2 MHz $\overline{TEST}$ = 1	1771-X1 CLK = 1 MHz $\overline{TEST}$ = 1	1771 or −X1 CLK = 2 MHz $\overline{TEST}$ = 0	1771 or −X1 CLK = 1 MHz $\overline{TEST}$ = 0
0 0	6ms	12ms	Approx. 400μs*	Approx. 800μs*
0 1	6ms	12ms		
1 0	10ms	20ms		
1 1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{XTDS}$) INPUT. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands, respectively, by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 μsec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the $\overline{\text{Write Fault}}$ bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK, STEP, STEP-IN, and STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page 4.

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_4

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Do not load head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

Table 4. FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)
- m = 0, Single Record
- m = 1, Multiple Records

b = Block length flag (Bit 3)
- b = 1, IBM format (128 to 1024 bytes)
- b = 0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)
- a_1a_0 = 00, FB (Data Mark)
- a_1a_0 = 01, FA (User defined)
- a_1a_0 = 10, F9 (User defined)
- a_1a_0 = 11, F8 (Deleted Data Mark)

Table 5. FLAG SUMMARY

TYPE III

s = Synchronize flag (Bit 0)
- $\bar{s}$ = 0, Synchronize to AM
- $\bar{s}$ = 1, Do Not Synchronize to AM

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)
- I_0 = 1, Not Ready to Ready Transition
- I_1 = 1, Ready to Not Ready Transition
- I_2 = 1, Index Pulse
- I_3 = 1, Immediate interrupt

E = Enable HLD and 10 msec Delay
- E = 1, Enable HLD, HLT and 10 msec Delay
- E = 0, Head is assumed Engaged and there is no 10 msec Delay

Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed; if V=0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID Field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is

valid ID CRC, an interrupt is generated, the Seek Error status bit (Status Bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation. If an ID Field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sents an interrupt (INTRQ).

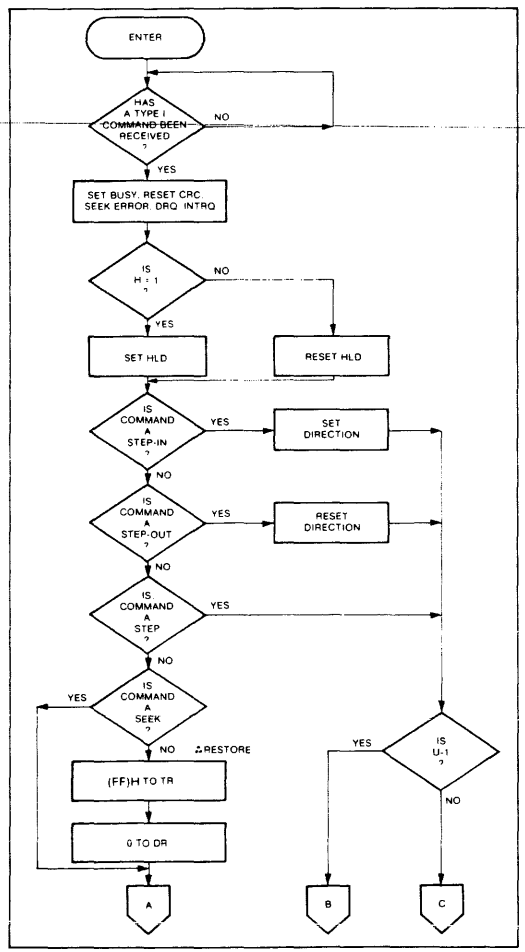
The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U=1, the track register is updated by one for each step. Whe U=0, the track register is not updated.

RESTORE (SEEK TRACK 0)

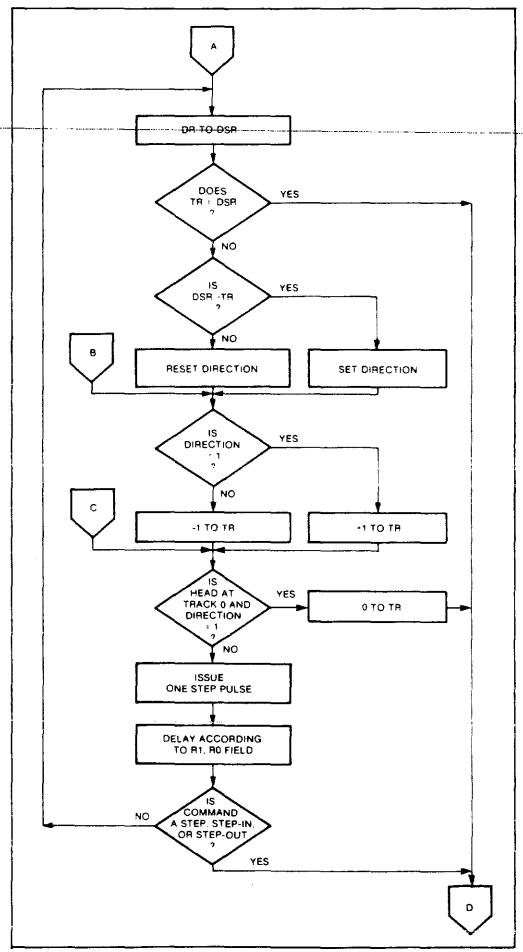
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when $\overline{MR}$ goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the



TYPE I COMMAND FLOW

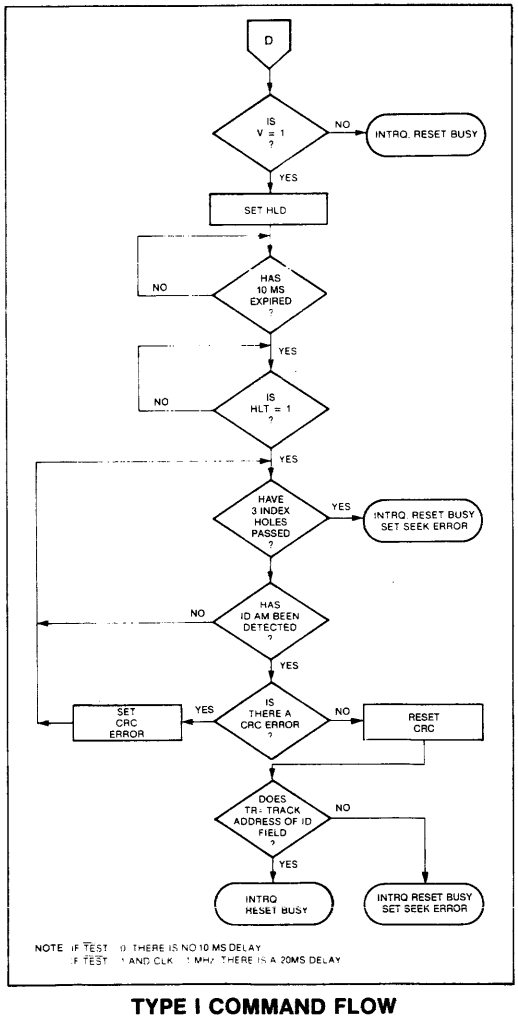


TYPE I COMMAND FLOW

Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



TYPE I COMMAND FLOW

STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector(s) and Write Sector(s) commands. Prior to loading the Type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag=1 (this is the normal case), HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and the Data Field format are shown below.

When an ID field is located on the disk, the FD1771 compares the track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending on the command. The FD1771 must find an ID field with a track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, 3.

GAP	ID AM	TRACK NUMBER	ZERO	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA = $(FE)_{16}$ CLK = $(C7)_{16}$

Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = $(C7)_{16}$

For b = 1

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below.

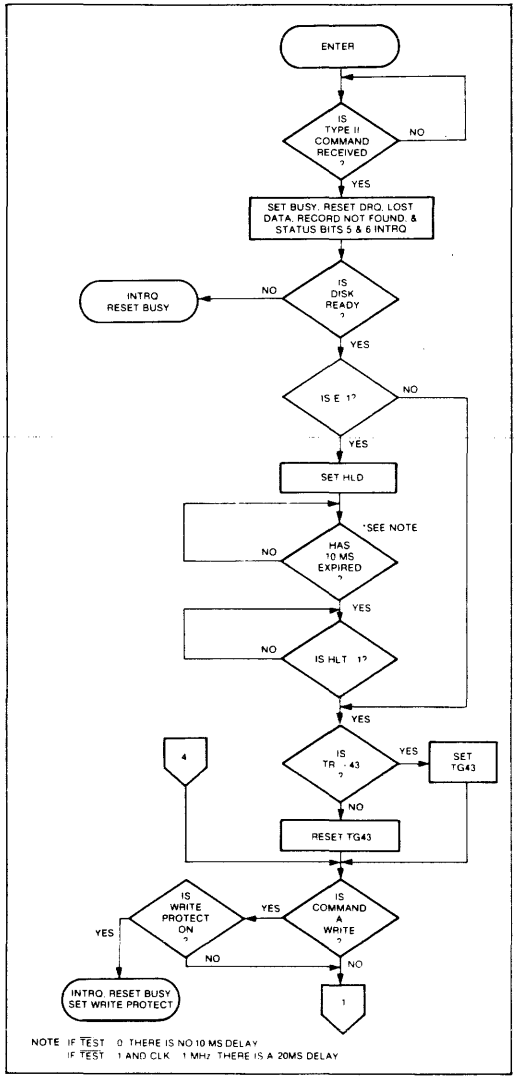
For b = 0

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II commands also contain a (m) flag which determines if the multiple records (sectors) are to be read or written, depending upon the command. If m=0 a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

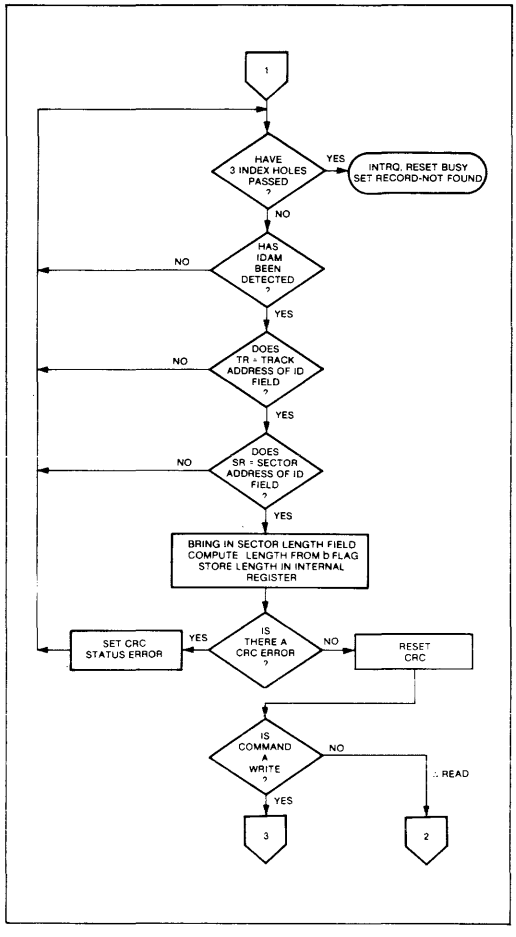
READ COMMAND

Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been

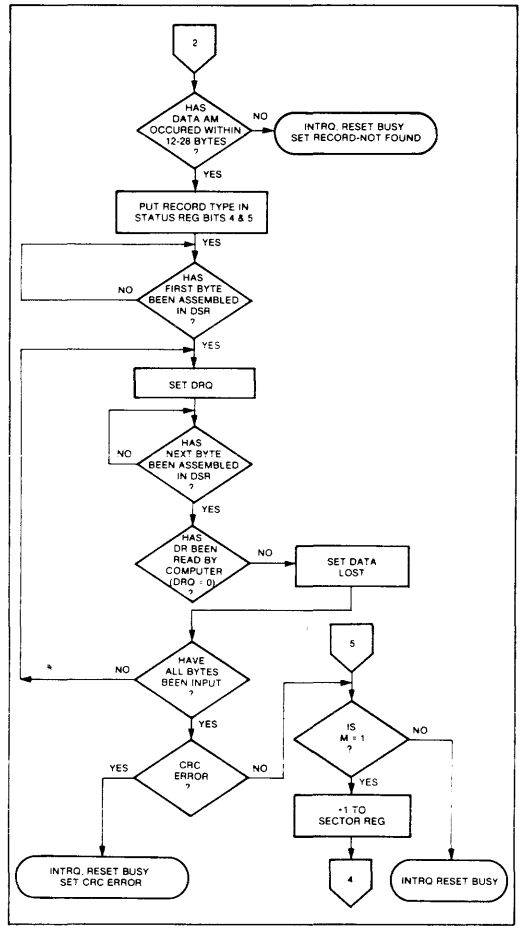


TYPE II COMMAND FLOW

shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the



TYPE II COMMAND FLOW



TYPE II COMMAND FLOW

Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a mulltiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below.

Status Bit 6	Status Bit 5	Data AM (Hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

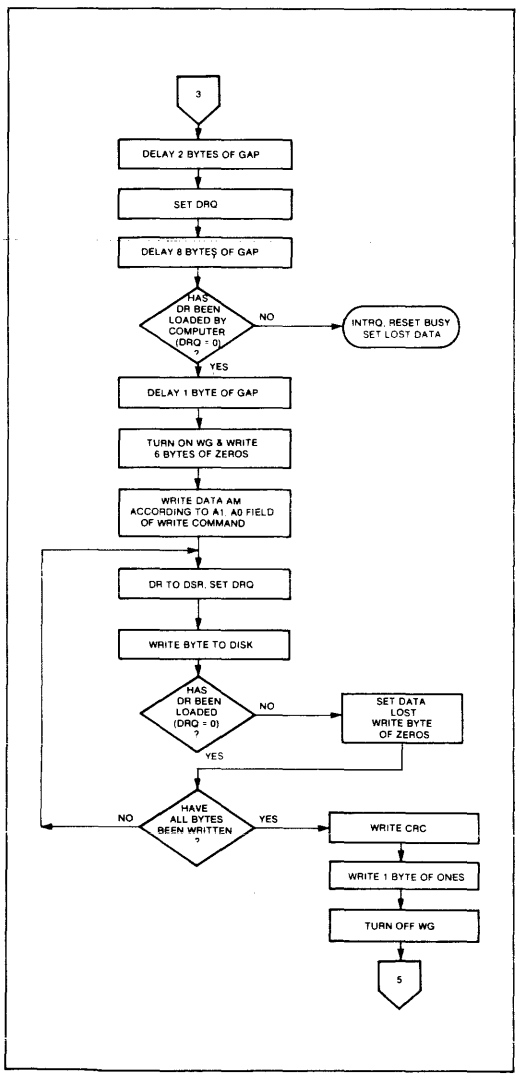
WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the BUSY status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $a_1 a_0$ field of the command as shown on next page.

The FD1771 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in

a_1	a_0	Data Mark (Hex)	Clock Mark (Hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

time for continuous writing the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.



TYPE II COMMAND FLOW

TYPE III COMMANDS

READ Address

Upon receipt of the Read Address command, the head is loaded and the BUSY Status bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below.

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

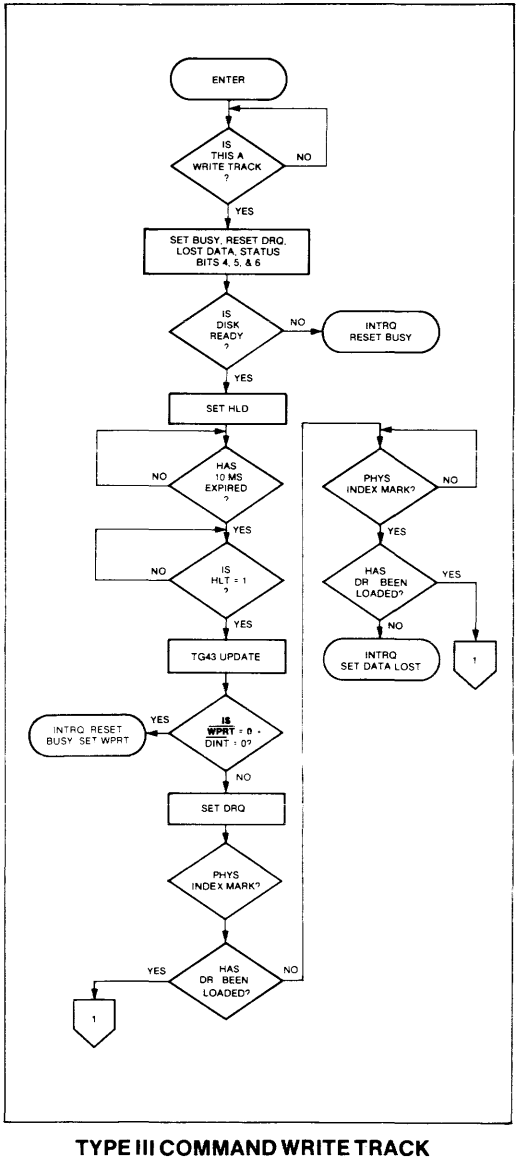
Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0(S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

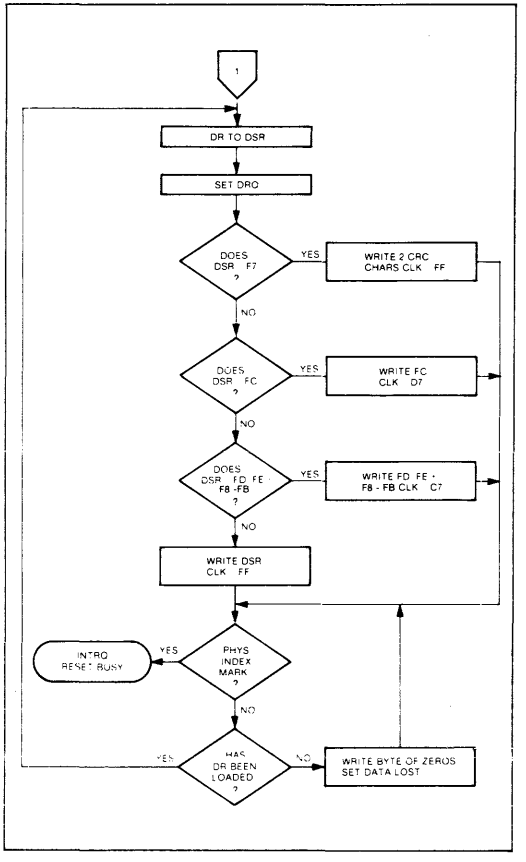
Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data status bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Character	FF
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7



TYPE III COMMAND WRITE TRACK

The Write Track Command will not execute if the $\overline{DINT}$ input is grounded; instead, the Write Protect status bit is set and the interrupt is activated. Note that one F7 pattern generates two CRC characters.

TYPE IV COMMAND

Force Interrupt

This command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0= Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (Requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2	TRACK 00	When set, indicates Read-Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and "ored" with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6	RECORD TYPE/ WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Ready operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK (Refer to section on Type III Commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1771 raises the Data Request signal. At this point in time, the user loads the Data Register with desired data to be written on the disk. For every byte of information to be written on the disk, a Data Request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1771 detects a data pattern on F7 through FE in the Data Register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128,256,512, or 1024 bytes, or may be formatted in non-IBM format with sector lengths of 16 to 4096 bytes in 16-byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes-/sector. The next section deals with the IBM 3740 format with 128 bytes/sector followed by a section of non-IBM formats.

IBM 3740 Formats — 128 Bytes/Sector

The IBM format with 128 bytes/sector is depicted in the Track Format figure on the following page. In order to create this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	Number of Bytes	Hex Value of Byte Written
	40	00 or FF
	6	00
	1	FC (Index Mark)
*	26	00 or FF
	6	00
	1	FE (ID Address Mark)
	1	Track Number (0 through 4C)
	1	00
	1	Sector Number (1 through 1A)
	1	00
	1	F7 (two CRCs written)
	11	00 or FF
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (two CRCs written)
	27	00 or FF
**	247	00 or FF

*Write bracketed field 26 times.
**Continue writing until FD1771 interrupts out. Approximately 247 bytes.

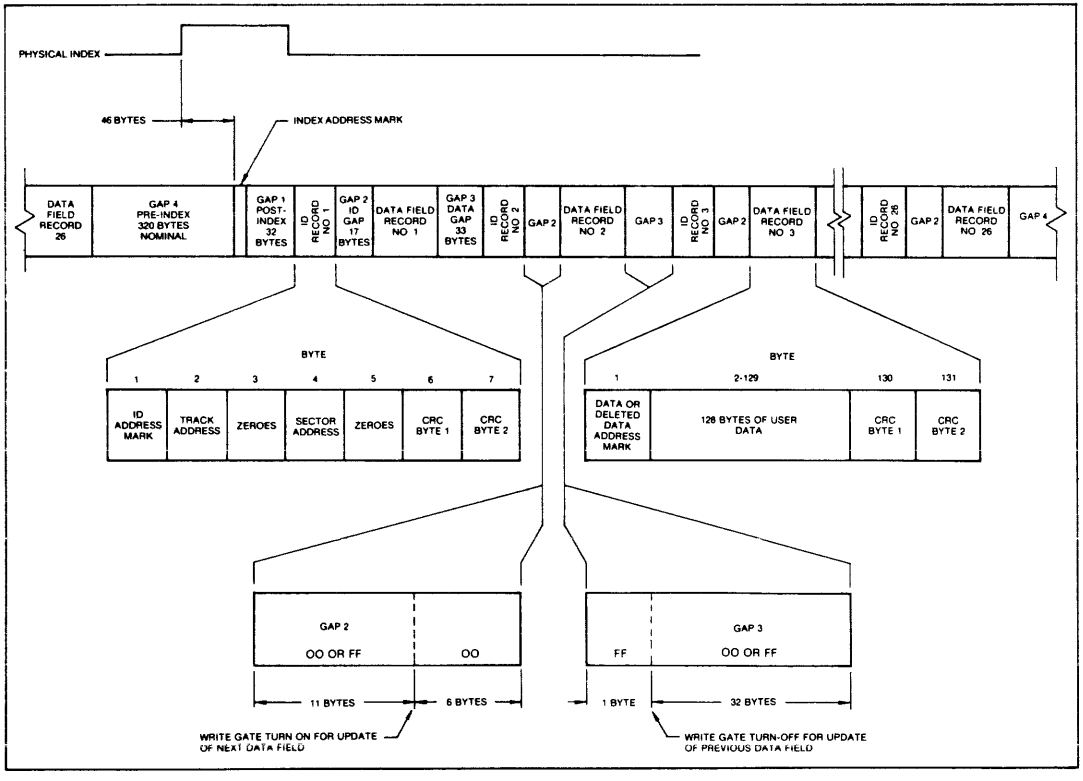
Non-IBM Formats

Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II commands with b flag equal to zero. Note that F7 through FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

1) IBM Diskette OEM Information GA21-9190-1.
2) SA900 IBM Compatibility Reference Manual — Shugart Associates.



TRACK FORMAT

ELECTRICAL CHARACTERISTICS

Maxium Ratings

V_{DD} with respect to V_{BB} (Ground)	+20 to -0.3V
Max Voltage to any input with respect to V_{BB}	+20 to -0.3V
Operating Temperature	0° C to 70° C
Storage Temperature	-55° C to +125° C

OPERATING CHARACTERISTICS (DC)

T_A = 0° C to 70° C, V_{DD} = +12.0V ± .6V, V_{BB} = -5.0 ± .5V, V_{SS} = 0V, V_{CC} = +5V ± .25V I_{DD} = 10 ma Nominal, I_{CC} = 30 ma Nominal, I_{BB} = 0.4 μa Nominal

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = -100 uA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.0 mA

TIMING CHARACTERISTICS

TA = 0° C to 70° C, V_{DD} = +12V ± .6V, V_{BB} = -5V ± .25V, V_{SS} = 0V, V_{CC} = +5V ± .25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz. Use 1 MHz when using mini-floppy.

Read Operations

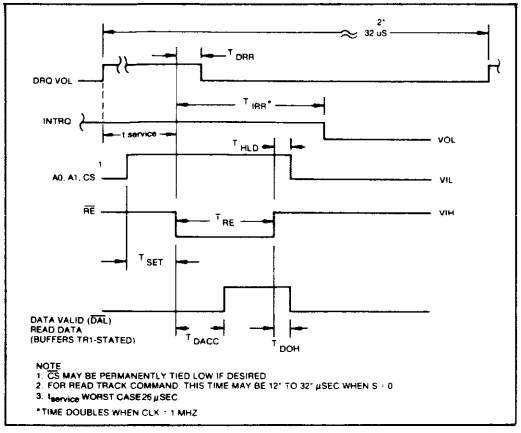
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR and CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	450			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			750	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			3000	nsec	
TDACC	Data Access from $\overline{RE}$			450	nsec	C_L = 25 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 25 pf

Write Operations

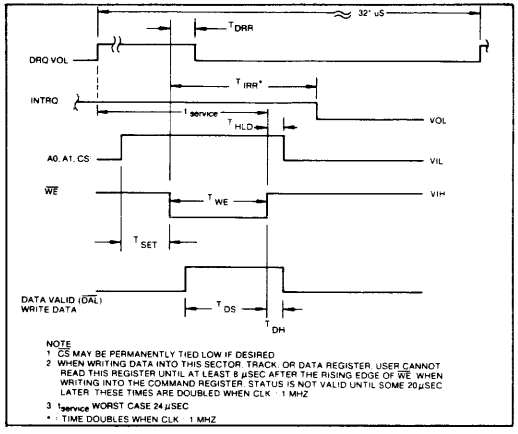
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR and CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	450	300		nsec	
TDRR	DRQ Reset from $\overline{WE}$			750	nsec	
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	350			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

External Data Separation ($\overline{XTDS}$ = 0)

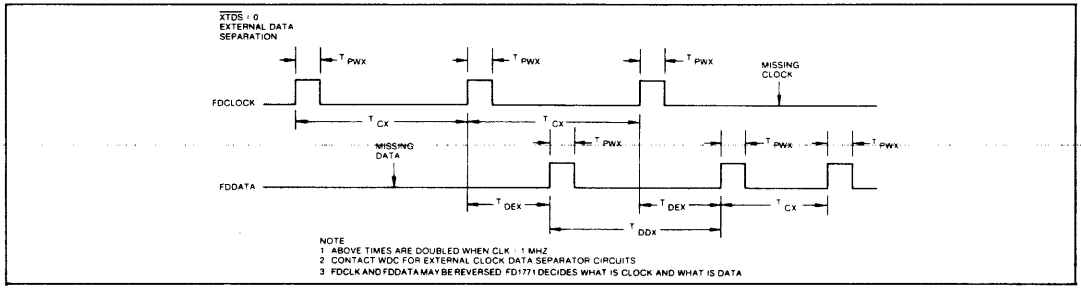
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWX	Pulse Width Read Data & Read Clock	150		350	nsec	
TCX	Clock Cycle External	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING



READ TIMING ($\overline{XTDS}$ = 0)

Internal Data Separation ($\overline{XTDS}$ = 1)

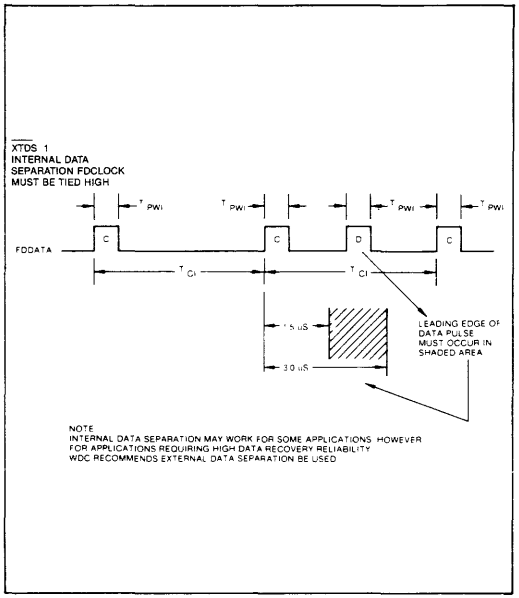
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWI	Pulse Width Data and Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

Write Data Timing

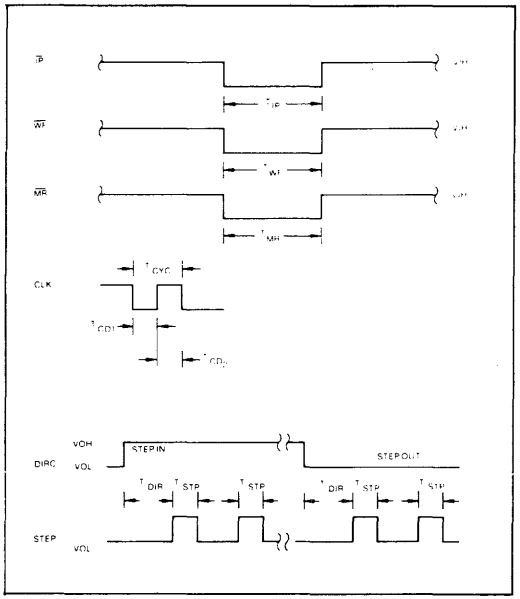
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

Miscellaneous Timing

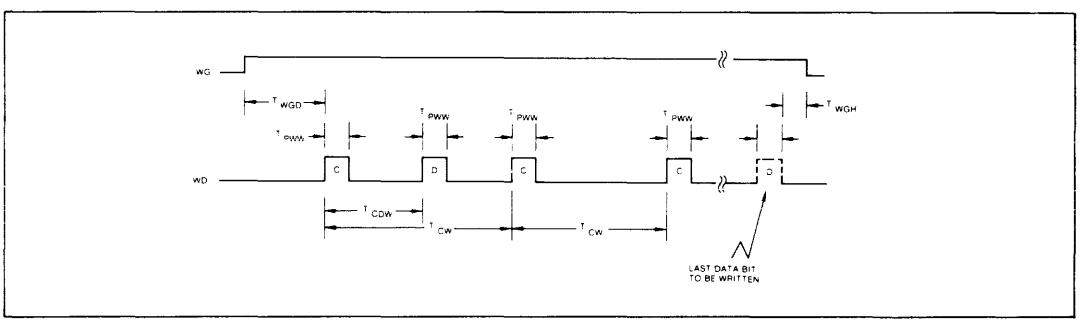
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TCD_1	Clock Duty	175			nsec	2 MHz ± 1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	These times doubled when CLK = 1 MHz
TDIR	Direct Setup to Step	24			nsec	
TMR	Master Reset Pulse Width	10			nsec	
TIP	Index Pulse Width	10			nsec	
TWF	Write Fault Pulse Width	10			nsec	



READ TIMING ($\overline{XTDS}$ = 1)



MISCELLANEOUS TIMING



WRITE DATA TIMING

See page 481 for ordering information.

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1771-01 Application Notes

INTRODUCTION

The FD1771-01 Floppy Disk Formatter/Controller is a MOS/LSI device designed to ease the task of interfacing the 8" or 5¼ (mini-floppy) disk drive to a host processor. It is ideally suited for a wide range of microprocessors, providing an 8-bit bi-directional interface to the CPU for all control and data transfers. Requiring standard + 12, ±5V power supplies, the 1771 is available in ceramic or plastic 40 pin dual-in-line packages.

The 1771 has been designed to be compatible with the IBM 3740 standard. This single-density Frequency Modulated (FM) recording technique, records a clock bit between a data bit serially on each track. Figure 1 illustrates how a HEX "D2" is recorded. Note that when the data bit to be written is zero, no pulse or flux transition is recorded. For the 8" drive, there are 77 tracks, with 26 sectors on each track. Each sector contains 128 bytes of data. Although there is no "standard" format for the mini-floppy, most manufacturers utilize either 35 or 40 tracks per side, wtih 16 sectors of 128 bytes each per track. Both the 8" and 5¼" formats must be soft-sectored, i.e., there are no physical holes to denote sector locations. The hard-sectored disk has been losing popularity, mainly due to the fact that the sector lengths cannot be increased.

Being soft-sector compatible, the 1771 must know where each sector begins on the track. This is performed by using Address Marks. These bytes are recorded on the disk with certain clock pulses missing, and are unique from all other data and gap bytes recorded on the track. Six distinct Address Marks can be used:

Description	Data	Clock Pattern
Index Address Mark	FC	D7
ID Address Mark	FE	C7
Data Address Mark	FB	C7
User defined	FA	C7
User Defined	F9	C7
Deleted Address Mark	F8	C7

The two "User Defined" Address Marks are unique to the 1771, and do not appear in the IBM 3740 standard. These Address Marks can be used to define the type of data i.e., "object" or "text" data, alternate sector data, or any other purpose the user chooses.

PROCESSOR INTERFACE

The 1771 contains five internal registers that can be accessed via the 8-bit DAL lines by the CPU. These registers are used to control the movement of the head, read and write sectors, and perform all other functions at the drive. Regardless of the operation performed, it must be initiated through one or more of these registers. They are selected by a proper binary code on the A0, A1 lines in conjunction with the $\overline{RE}$ and $\overline{WE}$ lines when the device is selected. The registers and their addresses are:

$\overline{CS}$	A_1	A_0	$\overline{RE}$ = 0	$\overline{WE}$ = 0
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	Deselected	Deselected

Command Register: This is a write-only register used to send all commands to the 1771.

Status Register: This is a read-only register that must be read at the completion of every command to determine whether execution was successful. It may also be used to monitor command execution, and to sense when data is required by the drive for read or write operations.

Track Register: This R/W register holds the current position of the R/W head.

Sector Register: This R/W register holds the desired sector number for read and write commands.

Data Register: This R/W register contains the data to be read or written to a particular sector.

INTERRUPTS

There are two INTERRUPT lines for CPU use. These are the DRQ (Data Request) and INTRQ (Interrupt Request). These are active high, open drain outputs and require a pull-up resistor of 10K or greater to +5V. Both of these signals also appear in the status register as the Busy (INTRQ) and the data request (DRQ) bits. The user has the option of utilizing these hardware lines for system interrupts, or through

software by polling the status register. The choice is dependent upon the particular microprocessor and support hardware of the system.

INTRQ: This line is used to signify the completion of any command. It is reset low when a new command is loaded into the command register, or when the status register is read.

DRQ: This line is active high whenever the data register requires servicing. During a read command, it signifies that the data register contains a byte of data from the disk and may be read by the CPU. During a write command, it signifies that the data register is empty and may be loaded with the next byte to be written on the disk. The DRQ line is reset whenever the data register is read or written to. It is also reset when a new command is loaded into the command register, providing the new command is not a Forced Interrupt, and the 1771 is not busy (Busy Bit = 0).

WRITE SECTOR

With the use of the WRITE SECTOR command, the CPU can access any desired sector(s) in a track. Prior to loading this command, the R/W head of the drive must be positioned over the specific track. This can be first accomplished with the use of any of the Type I commands. Once positioned, the CPU must load the desired sector number into the sector register, then issue the command. The head will load, and the 1771 will begin searching for the correct ID field. If the correct sector and track is not found within 2 revolutions of the disk, the RECORD-NOT-FOUND bit will be set in the status register, and the command will be terminated. Once found, the 1771 will issue a DRQ in request of the first data byte to be written. Once the data register is loaded, the 1771 will issue a DRQ for each byte to be recorded, until the entire sector is written. For the 8" drive, the user must load the data register 24 microseconds after a DRQ is generated. Failure to meet this time will cause the lost data bit to be set, and a byte of zeros substituted and written on the disk.

READ SECTOR

The READ SECTOR command functions in much the same way as the WRITE SECTOR command. The sector register must again be loaded with the desired sector number, before the read command can be loaded. After the ID field has been found, the 1771 will begin generating DRQ's, with the data register being loaded with each byte of the sector field. For the 8" drive, the user must read the data register at least 26 microseconds after the DRQ is generated. Failure to meet this time will cause the lost data bit to be set in the status register, while the next assembled byte will overwrite the contents of the data register.

Both the Read and Write sector commands also contain an "m" flag for accessing multiple sectors. The sector register is incremented internally after each sector is read or written to. Eventually the sector register will exceed the physical number of sectors on the track. The user can either issue the Forced Interrupt command after the last sector, or wait for the 1771 to interrupt out. In the latter case, the RECORD-NOT-FOUND status bit will be set.

FLOPPY DISK INTERFACE

For the most part, the actual Floppy Disk Interface will consist mainly of Buffer/Drivers. Most drives manufactured today require an open collector TTL interface, with appropriate resistor terminal networks. Figure 2 shows the interface of the 1771 to a Shugart SA400 Drive. Aside from the data seperator, the interface consists mainly of 7438's and 7414 TTL gates. A 9602 one-shot is used for the desired head load delay. In this illustration, the 6800 microprocessor is used via a 6820 Peripheral Interface Adapter to control all functions of the 1771. Similarly, other parallel port devices (such as the 8255 for 8080 systems) can be used for the interface, or the 1771 may simply be tied directly to the systems data bus and control lines, providing TTL loading factors are observed.

DATA SEPERATION

The internal DATA SEPERATOR of the 1771 can be used by tying the $\overline{\text{XTDS}}$ line high, and supplying the combined clock and data pulses on the FD data line. In order to maintain an error rate better than 1 in 10^8, and external data seperator is recommended.

Since the 1771 system clock is at 2 MHz, this allows for a 500 ns resolution. The internal data window will move 500 ns with respect to the incoming data bit. On the inner tracks of the drive, the bit shift is more severe and may occasionally cause a data or clock bit to fall outside of this data window. Since the 1771 will perform up to 5 retries, this error rate may be acceptable for some applications.

When the $\overline{\text{XTDS}}$ line is forced low, the 1771 will accept seperated clock and data on the FDCLOCK and FDDATA lines. Figure 3 illustrates the timing of these signals. The actual FDCLOCK and FDDATA lines may be reversed; the 1771 will determine which line is clock and which is data when an Address Mark is detected. This feature greatly simplifies the design of the data seperator.

Figure 4 illustrates the Phase-Lock Loop method for data seperation. The circuit operates at 8 MHz, or 32 times the frequency of a received bit cell. The MC4024 VCO is used to supply the nominal clock frequency. The first 74LS161 counter provides a divide by 16 frequency and a carry to one side of the MC4044 phase detector. The other input of the MC4044 is tied to another 74LS161 counter which is affected by the incoming data stream. The output of

the phase detector is a signal proportional to the differences of the incoming pulses. This is then fed through a low pass filter, and to the input of the MC4024 to adjust the output frequency. Figures 5 thru 8 illustrate other types of data seperators. These employ the "Counter Seperator" techniques and are quite different from the Phase-Lock-Loop method. With the addition of "One-Shot" delay element or an input clock, most of the complexity of the PPL circuit can be eliminated.

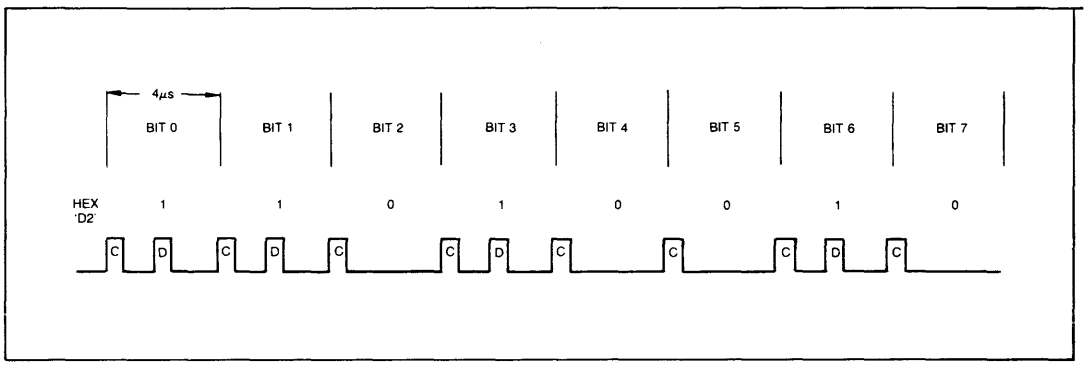

FIGURE 1. FM RECORDING.

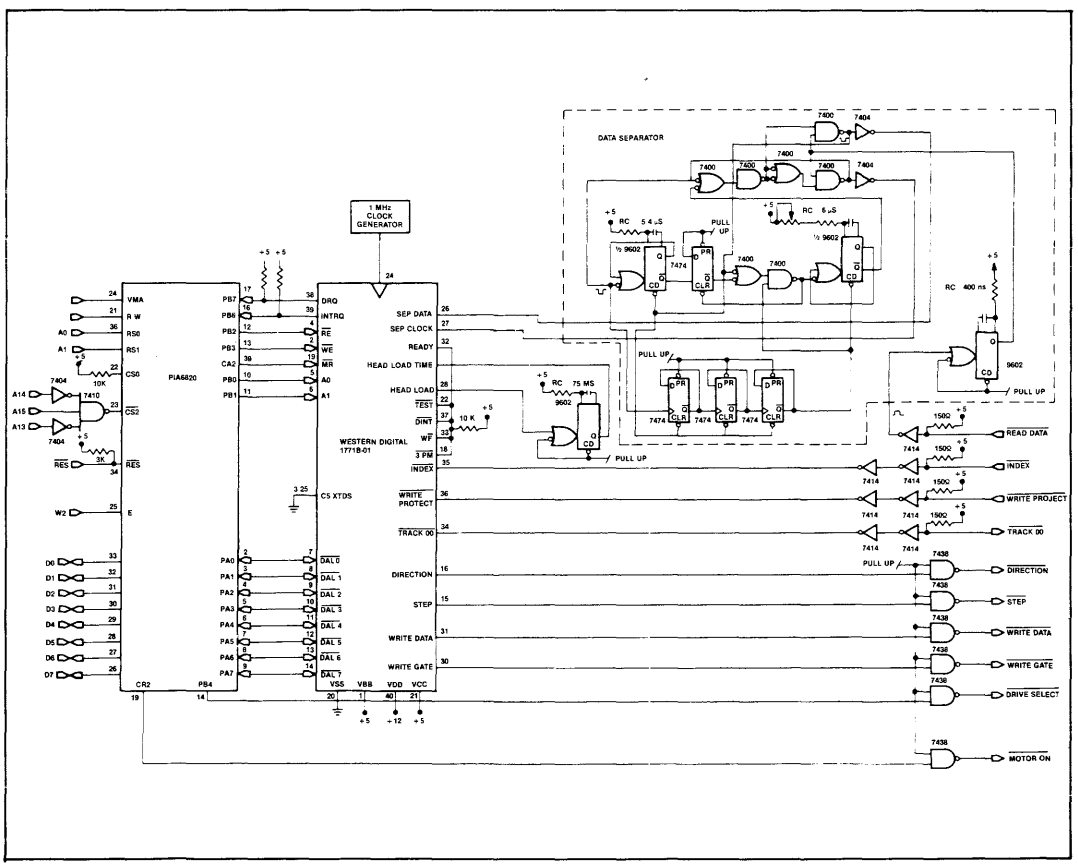

FIGURE 2. 1771 TO SHUGART SA400 DRIVE

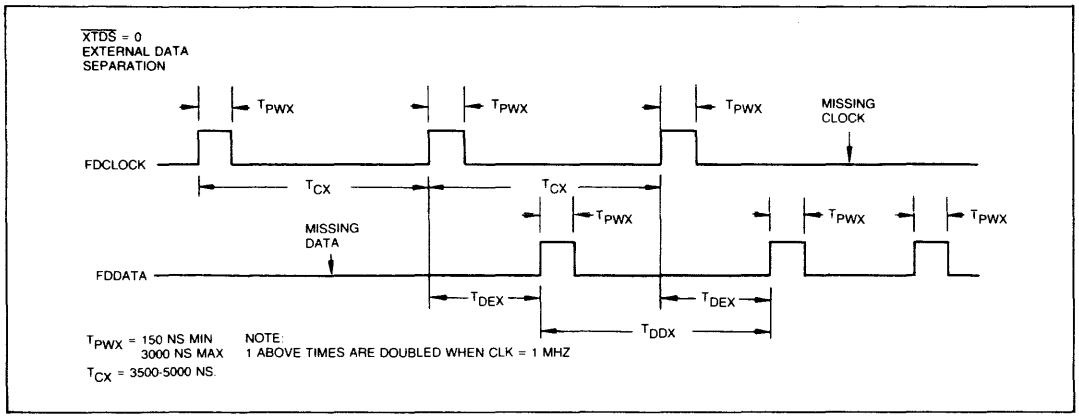

FIGURE 3. EXTERNAL DATA SEPERATOR TIMING.

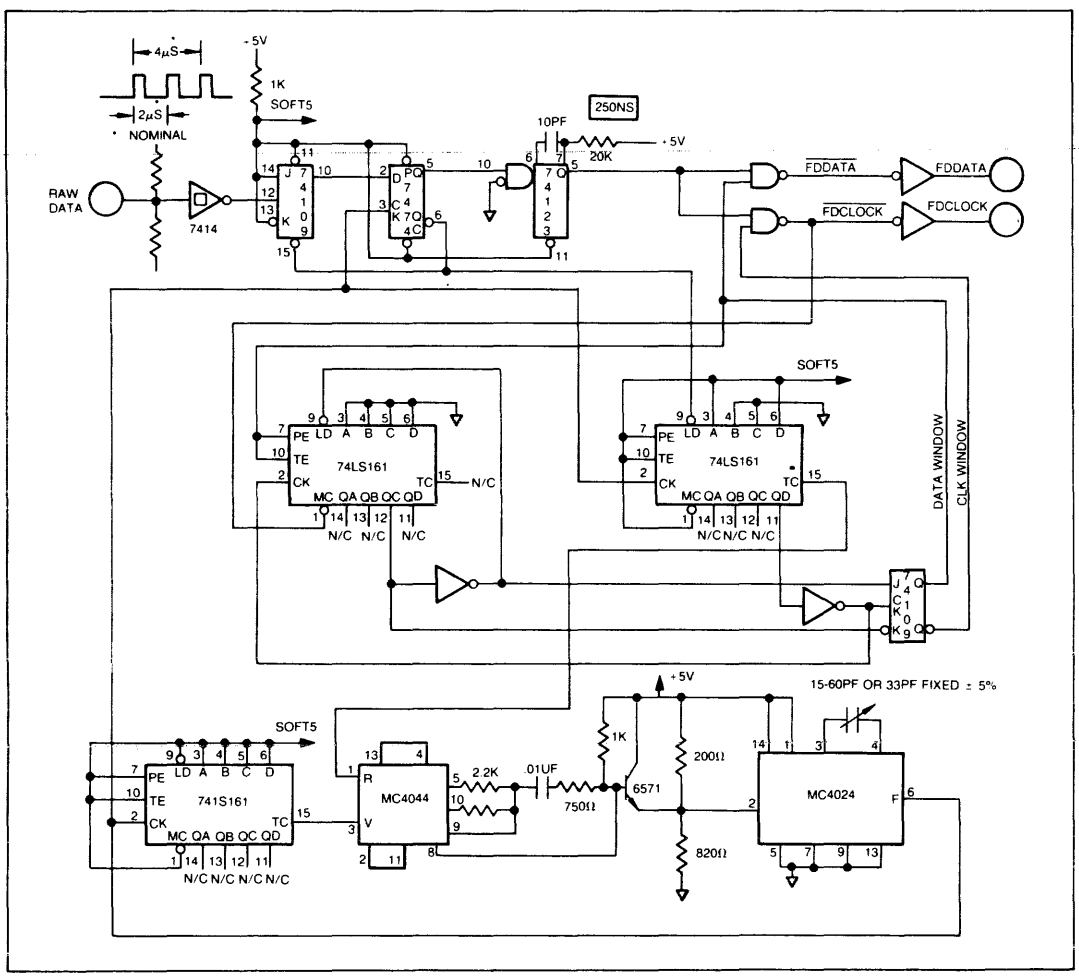

FIGURE 4. CIRCUIT PROVIDED COURTESY OF MOTOROLA AND ICOM CORPS.

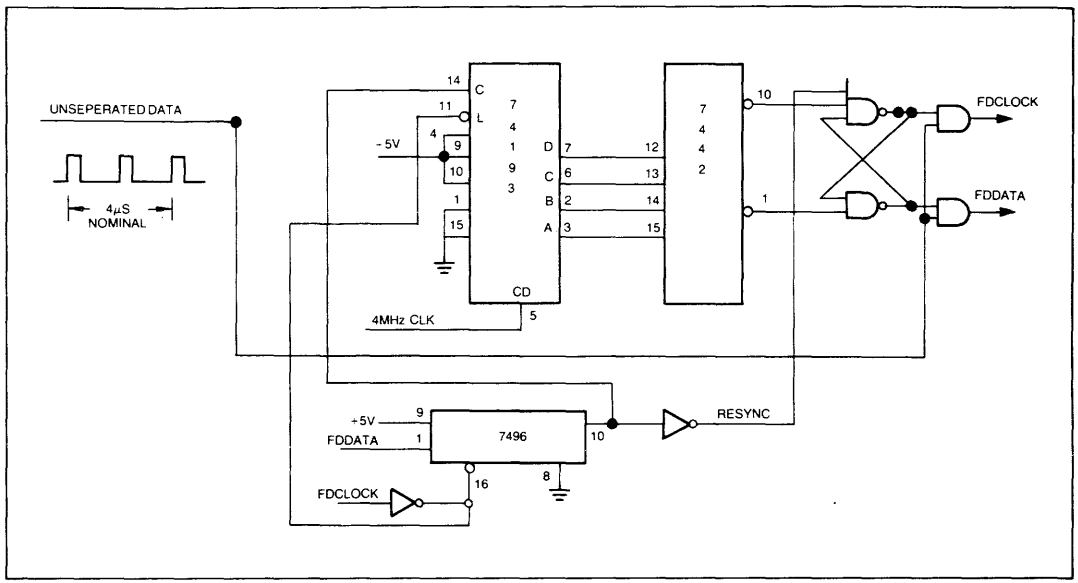

FIGURE 5. CIRCUIT PROVIDED COURTESY OF PROCESSOR APPLICATIONS LTD.

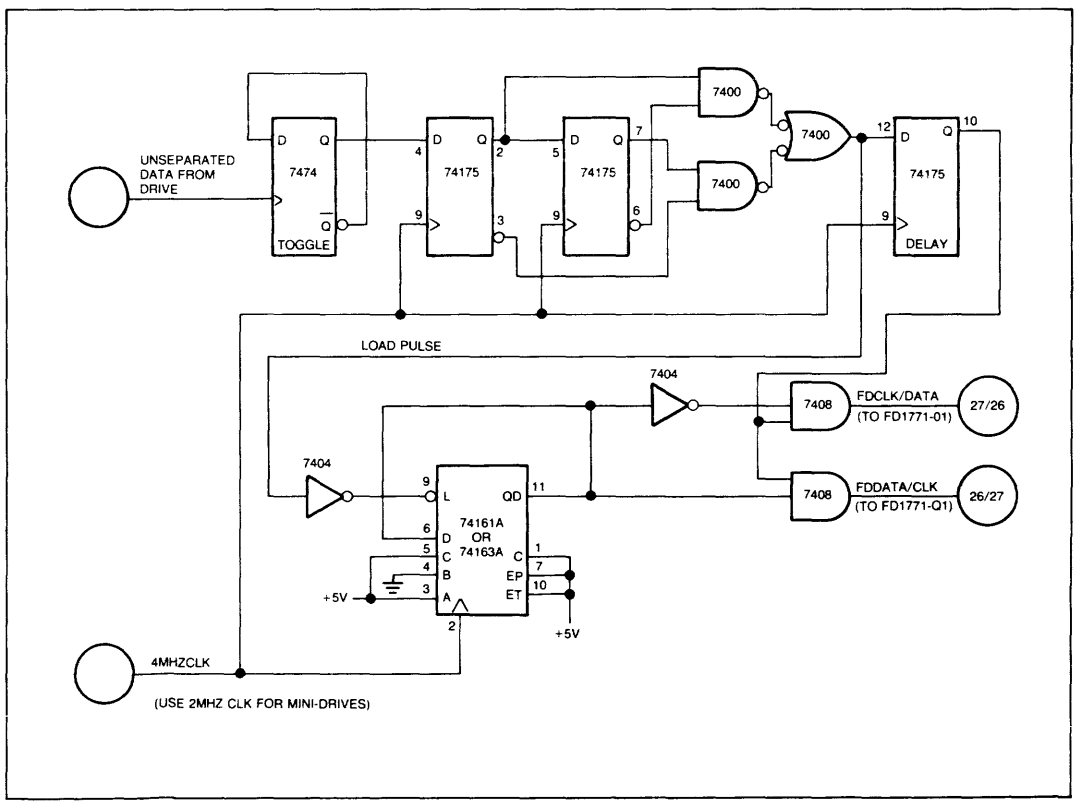

FIGURE 6.

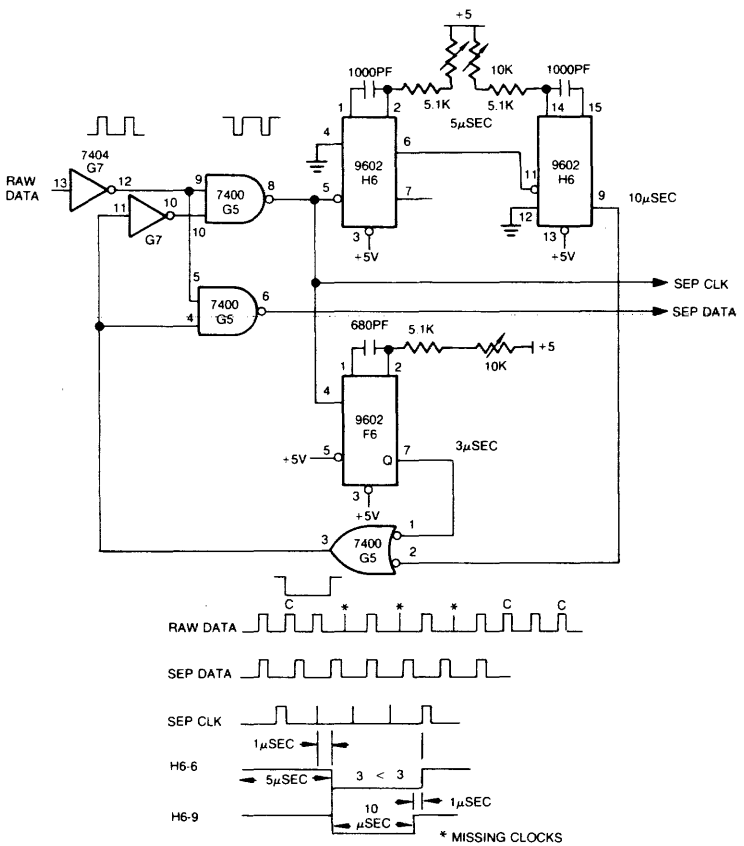

FIGURE 7. CIRCUIT PROVIDED COURTESY OF ACUTEST CORP.

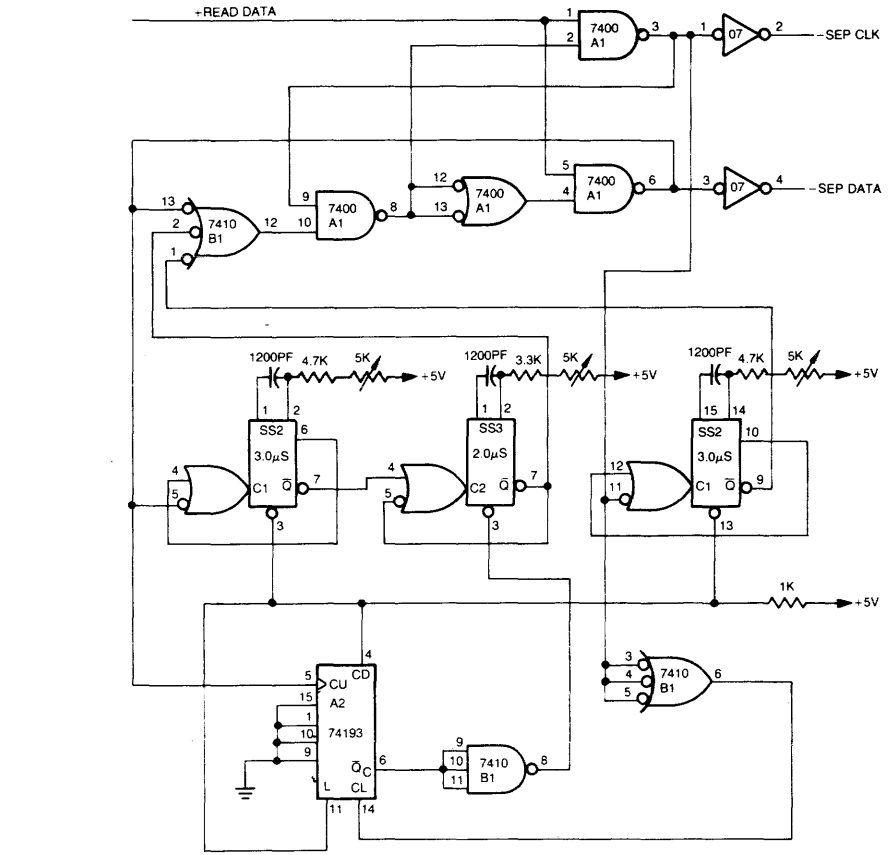

FIGURE 8. CIRCUIT PROVIDED COURTESY OF SHUGART ASSOCIATES.

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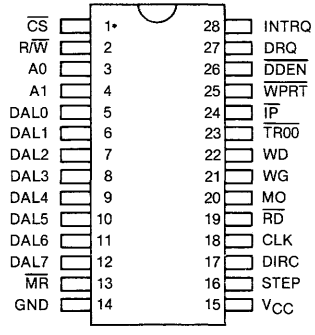
PRELIMINARY

WD1770/1772 5¼" Floppy Disk Controller/Formatter

FEATURES

- 28 PIN DIP
- SINGLE 5V SUPPLY
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- 5¼" SINGLE AND DOUBLE DENSITY
- MOTOR CONTROL
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- TTL COMPATIBLE
- 8 BIT BIDIRECTIONAL DATA BUS
- TWO VERSIONS AVAILABLE
  WD1770 = STANDARD 179X STEP RATES
  WD1772 = FASTER STEP RATES



PIN DESIGNATION

DESCRIPTION

The WD1770 is a MOS/LSI device which performs the functions of a 5¼" Floppy Disk Controller/Formatter. It is similar to its predecessor, the WD179X, but also contains a digital data separator and write precompensation circuitry. The drive side of the interface needs no additional logic except for buffers/receivers. Designed for 5¼" single or double density operation, the device contains a programmable Motor On signal.

The WD1770 is implemented in NMOS silicon gate technology and is available in a 28 pin dual-in-line.

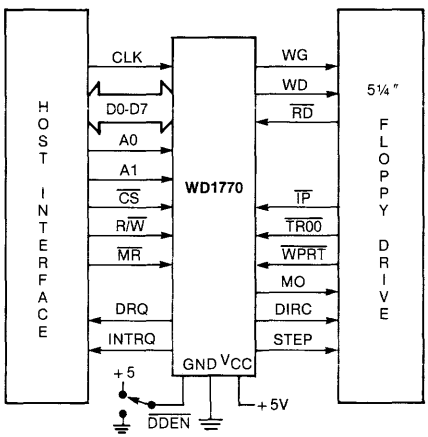
The WD1770 is a low cost version of the FD179X Floppy Disk Controller/Formatter. It is compatible with the 179X, but has a built-in digital data separator and write precompensation circuits. A single read line (RD, Pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device has been specifically designed for control of 5¼" floppy disk drives with data rates of 125 KBits/Sec (single density) and 250 KBits/Sec (double density). In addition, write precompensation of 125 Nsec from nominal can be enabled at any point through simple software commands. Another programmable feature, Motor On, has been incorporated to enable the spindle motor automatically prior to operating a selected drive.

Two versions of the WD1770 are available. The standard version is compatible with the 179X stepping rates, while the WD1772 offers stepping rates of 2, 3, 5 and 6 msec.

The processor interface consists of an 8-bit bidirectional bus for transfer of status, data, and commands. All host communication with the drive occurs through these data lines. They are capable of driving one standard TTL load or three "LS" loads.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enable Host communication with the device.
2	READ/WRITE	R/$\overline{W}$	A logic high on this input controls the placement of data on the $\overline{D0}$-$\overline{D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	ADDRESS 0,1	A0, A1	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DATA ACCESS LINES 0 THROUGH 7	DAL0-DAL7	Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line will drive one TTL load.
13	MASTER RESET	$\overline{MR}$	A logic low pulse on this line resets the device and initializes the status register (internal pull-up).
14	GROUND	GND	Ground.
15	POWER SUPPLY	V_{CC}	+5V ±5% power supply input.
16	STEP	STEP	The Step output contains a pulse for each step of the drive's R/$\overline{W}$ head. The WD1770 and WD1772 offer different step rates.
17	DIRECTION	DIRC	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLOCK	CLK	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHZ ±1%.
19	READ DATA	$\overline{RD}$	This active low input is the raw data line containing both clock and data pulses from the drive.
20	MOTOR ON	MO	Active high output used to enable the spindle motor prior to read, write or stepping operations.
21	WRITE GATE	WG	This output is made valid prior to writing on the diskette.
22	WRITE DATA	WD	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	TRACK 00	$\overline{TR00}$	This active low input informs the WD1770 that the drive's R/$\overline{W}$ heads are positioned over Track zero (internal pull-up).
24	INDEX PULSE	$\overline{IP}$	This active low input informs the WD1770 when the physical index hole has been encountered on the diskette (internal pull-up).
25	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).
26	DOUBLE DENSITY ENABLE	$\overline{DDEN}$	This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN}$ = 0, double density is selected (internal pull-up).

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	DATA REQUEST	DRQ	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTERRUPT REQUEST	INTRQ	This active high output is set at the completion of any command or reset a read of the Status Register.



WD1770 SYSTEM BLOCK DIAGRAM

ARCHITECTURE

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RD) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

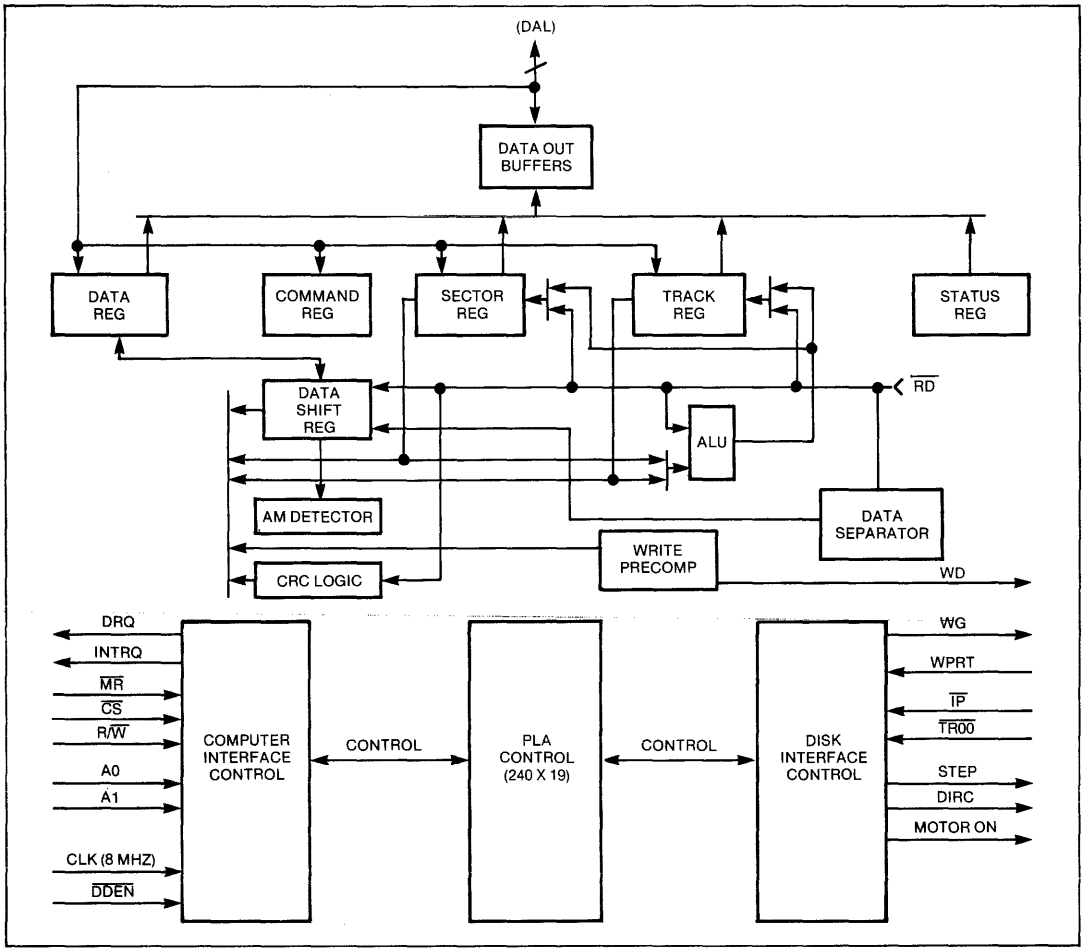
Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:
$G(x) = x^{16} + x^{12} + x^5 + 1$.
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.



WD1770 BLOCK DIAGRAM

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The FD1770 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0, double density (MFM) is enabled. When $\overline{DDEN}$ = 1, single density is enabled.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Data Separator — A digital data separator consisting of a ring shift register and data window detection logic provides read data and a recovery clock to the AM detector.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD1770. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and R/$\overline{W}$ = 1 are active or act as input receivers when $\overline{CS}$ and R/$\overline{W}$ = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signal R/$\overline{W}$ during a Read operation or Write operation are interpreted as selecting the following registers:

A1 · A0	READ (R/$\overline{W}$ = 1)	WRITE (R/$\overline{W}$ = 0)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD1770 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operations continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The WD1770 has two modes of operation according to the state $\overline{DDEN}$ (Pin 26). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 18) is at 8 MHZ.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

The number of sectors per tract as far as the WD1770 is concerned can be from 1 to 255 sectors. The number of tracks as far as the WD1770 is concerned is from 0 to 255 tracks.

GENERAL DISK WRITE OPERATION

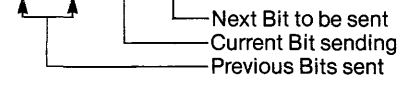
When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For Write operations, the WD1770 provides Write Gate (Pin 21) to enable a Write condition, and Write Data (Pin 22) which consists of a series of active high pulses. These pulses contain both Clock and Data information in FM and MFM. Write Data provides the unique missing clock patterns for recording Address Marks.

The Precomp Enable bit in Write commands allow automatic Write precompensation to take place. The outgoing Write Data stream is delayed or advanced from nominal by 125 nanoseconds according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A



Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximun.

COMMAND DESCRIPTION

The WD1770 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-in	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	h	E	0	0
II	Write Sector	1	0	1	m	h	E	P	a_0
III	Read Address	1	1	0	0	h	E	0	0
III	Read Track	1	1	1	0	h	E	0	0
III	Write Track	1	1	1	1	h	E	P	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3)

h = 0, Enable Spin-Up Sequence
h = 1, Disable Spin-Up Sequence

V = Verify Flag (Bit 2)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1, 0)

r_1	r_0	WD1770	WD1772
0	0	6 ms	2 ms
0	1	12 ms	3 ms
1	0	20 ms	5 ms
1	1	30 ms	6 ms

u = Update Flag (Bit 4)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

a_0 = Data Address Mark (Bit 0)

a_0 = 0, Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

E = 30ms Settling Delay (Bit 2)

E = 0, No Delay
E = 1, Add 30ms Delay

P = Write Precompensation (Bit 1)

P = 0, Enable Write Precomp
P = 1, Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = 1, Don't Care
I_1 = 1, Don't Care
I_2 = 1, Interrupt on Index Pulse
I_3 = 1, Immediate Interrupt
I_3-I_0 = 0, Terminate without Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0,r_1), which determines the stepping motor rate.

A 4μs (MFM) or 8 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24μs before the first stepping pulse is generated.

After the last directional step an additional 30 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 30 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID field is read from the disk for the verification operation.

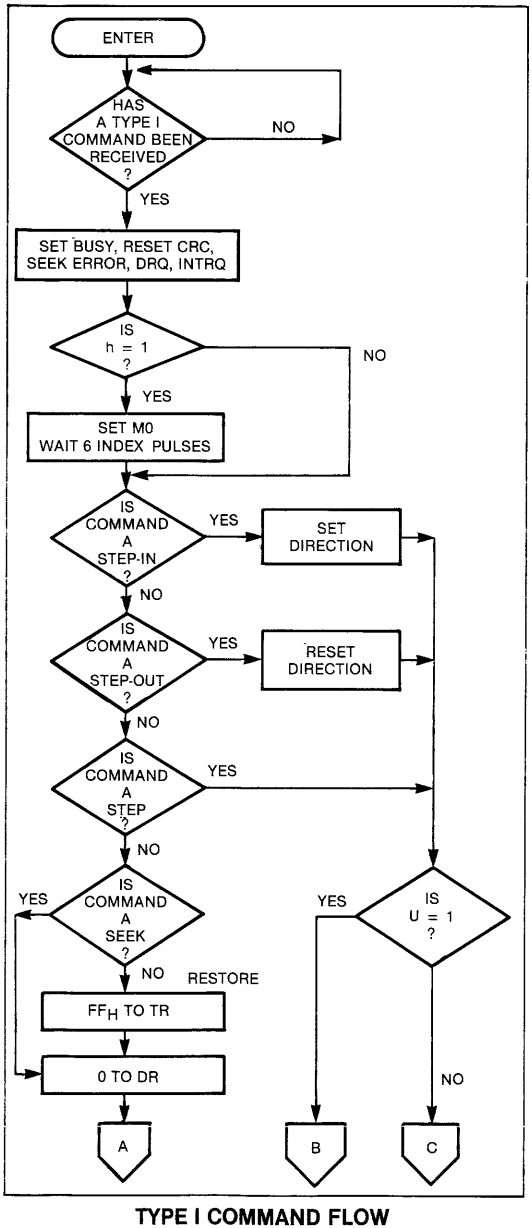
The WD1770 must find an ID field with correct track number and correct CRC within 5 revolutions of the media, otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

All commands, except the Force Interrupt command, may be programmed via the h Flag to delay for spindle motor start up time. If the h Flag is set and the Motor On line (Pin 20) is low when a command is received, the WD1770 will force Motor On to a logic 1 and wait 6 revolutions before executing the command. At 300 RPM, this guarantees a one second spindle start up time. If after finishing the command, the device remains idle for 10 revolutions, the Motor

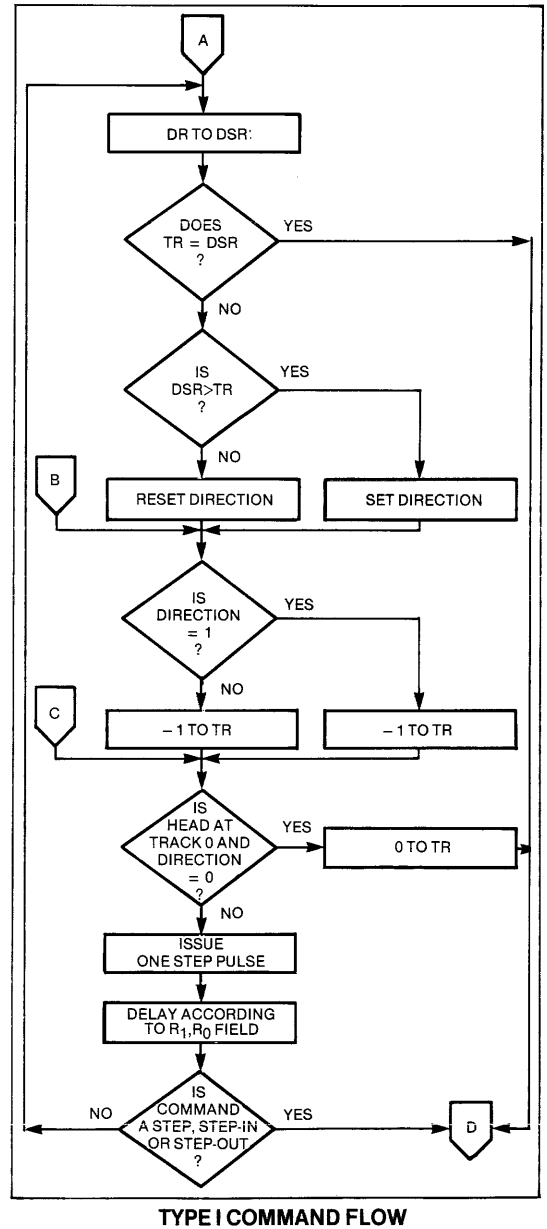
On line will go back to a logic 0. If a command is issued while Motor On is high, the command will execute immediately, defeating the 6 revolution start up. This feature allows consecutive Read or Write commands without waiting for motor start up each time; the WD1770 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (Pin 16) at a rate specified by the r_1,r_0 field are issued until the $\overline{TR00}$ input is activated.



TYPE I COMMAND FLOW

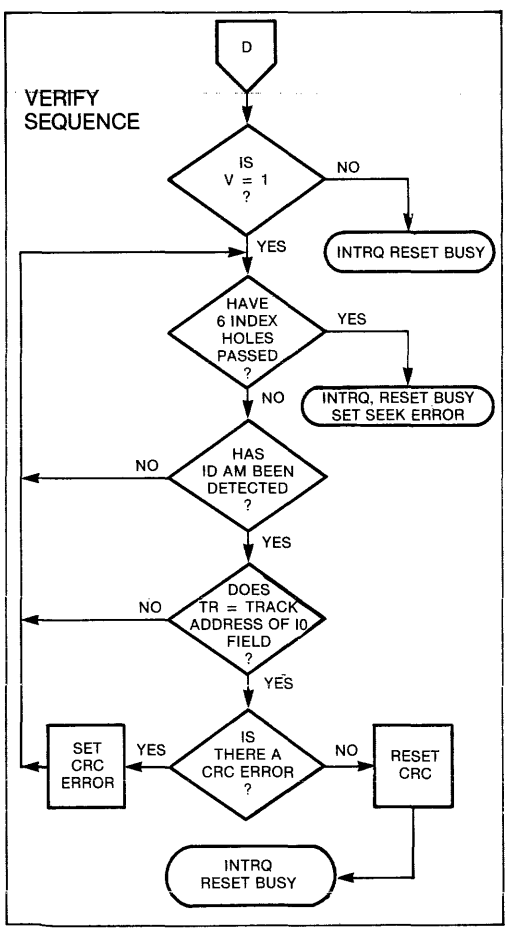


TYPE I COMMAND FLOW

At this time, the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the WD1770 terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD1770 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.



TYPE I COMMAND FLOW

STEP

Upon receipt of this command, the WD1770 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD1770 issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

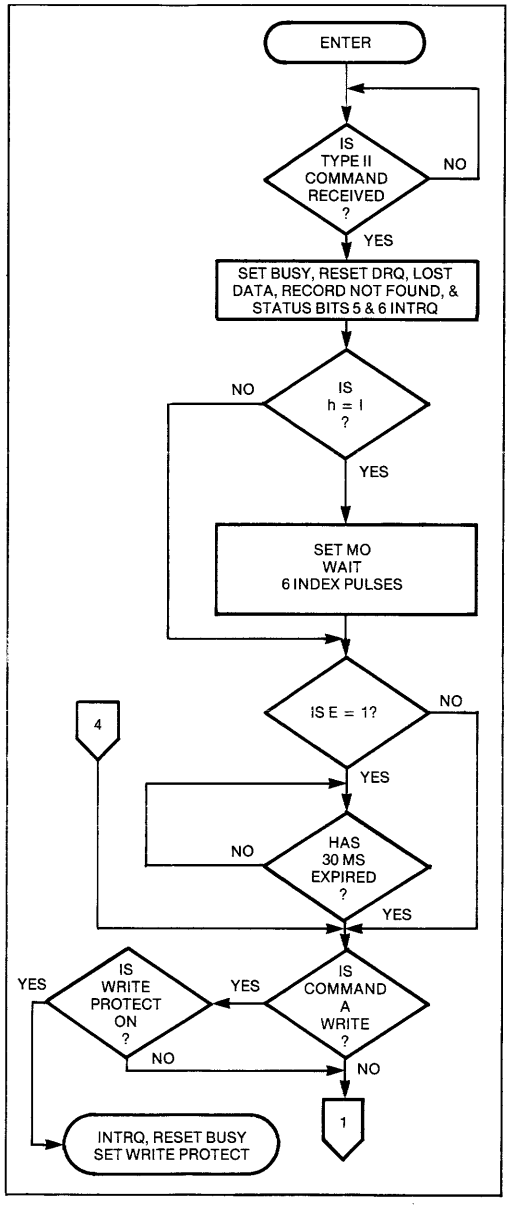
STEP-OUT

Upon receipt of this command, the WD1770 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status bit is set. If the E flag = 1 the command will execute after a 30 msec delay.

When an ID field is located on the disk, the WD1770 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The WD1770 must find an ID field with a Track number, Sector number, and CRC within four revolutions of the disk, other-



TYPE II COMMAND

wise, the Record not found status bit is set (Status Bit 4) and the command is terminated with an interrupt (INTRQ).

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The WD1770 will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD1770 is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The WD1770 will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

READ SECTOR

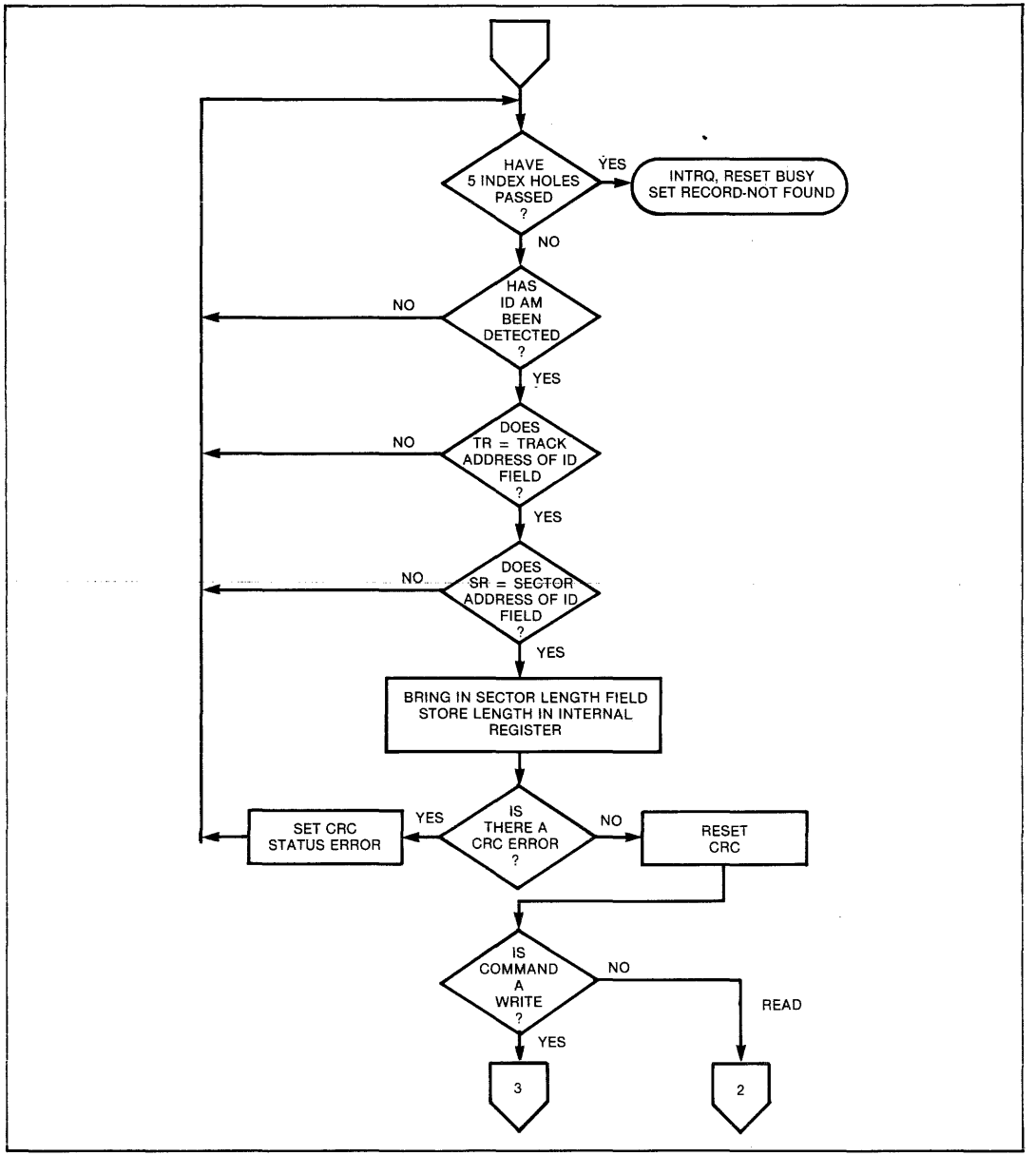
Upon receipt of the Read Sector command, the Busy status bit is set, and when a ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The WD1770 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated

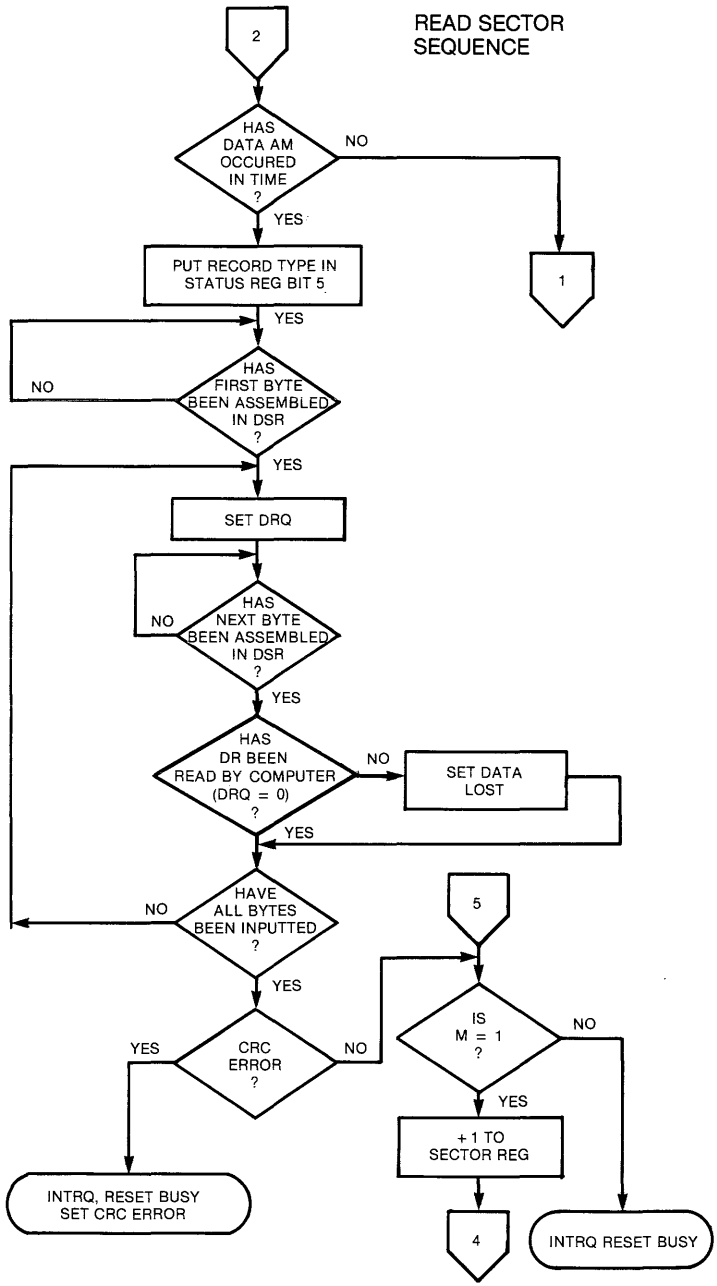


TYPE II COMMAND

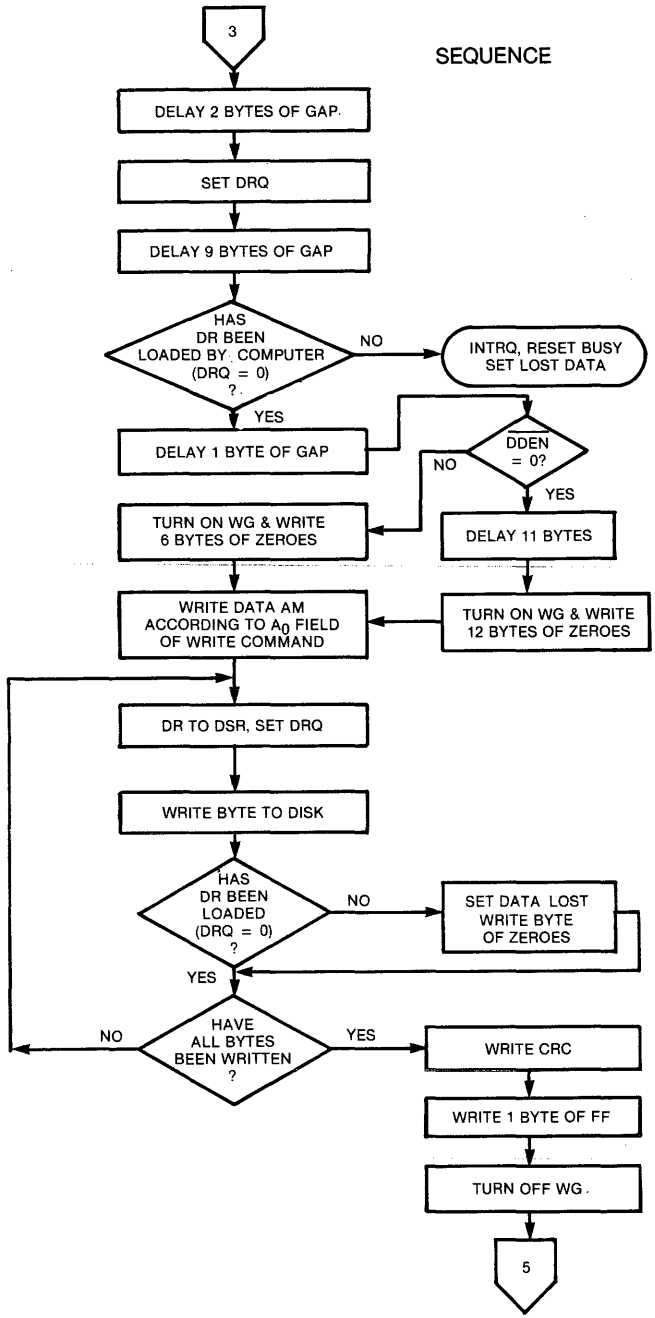
and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time, the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The WD1770 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit



TYPE II COMMAND



TYPE II COMMAND

is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. INTRQ will set 24μsec (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeroes.

TYPE III COMMANDS

Read Address

Upon receipt of the Read Address command, the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD1770 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the READ track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

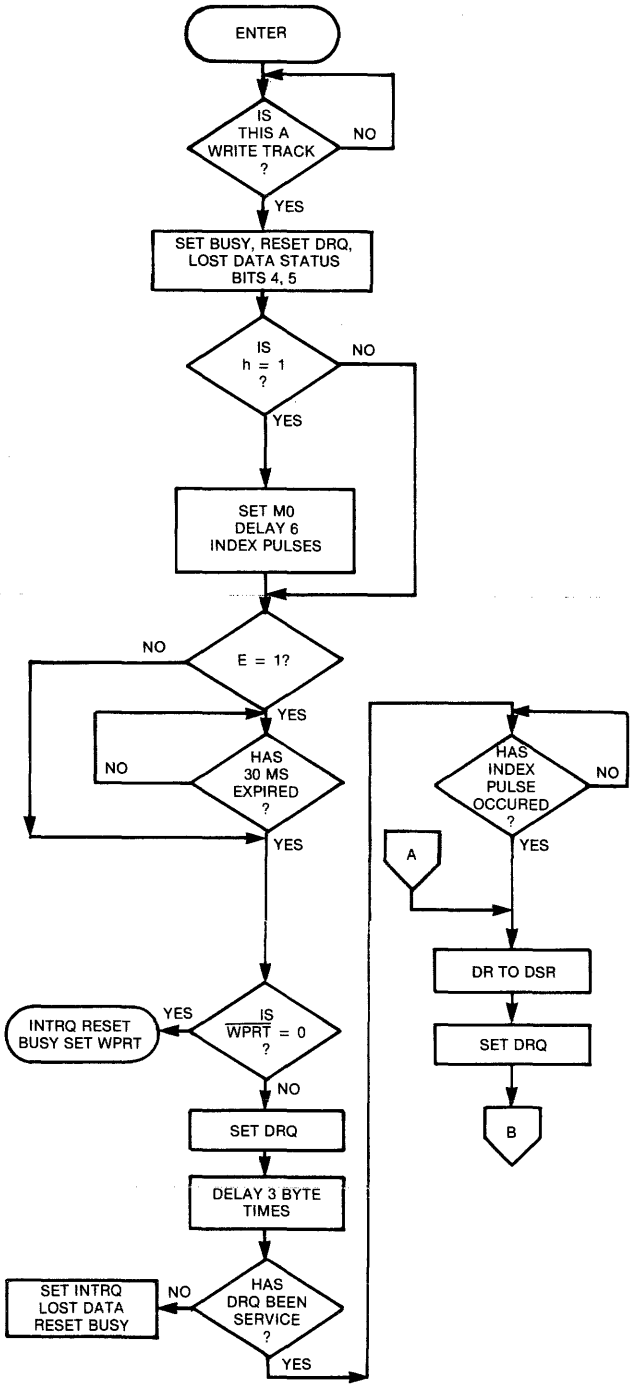
Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded within 3 byte times, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

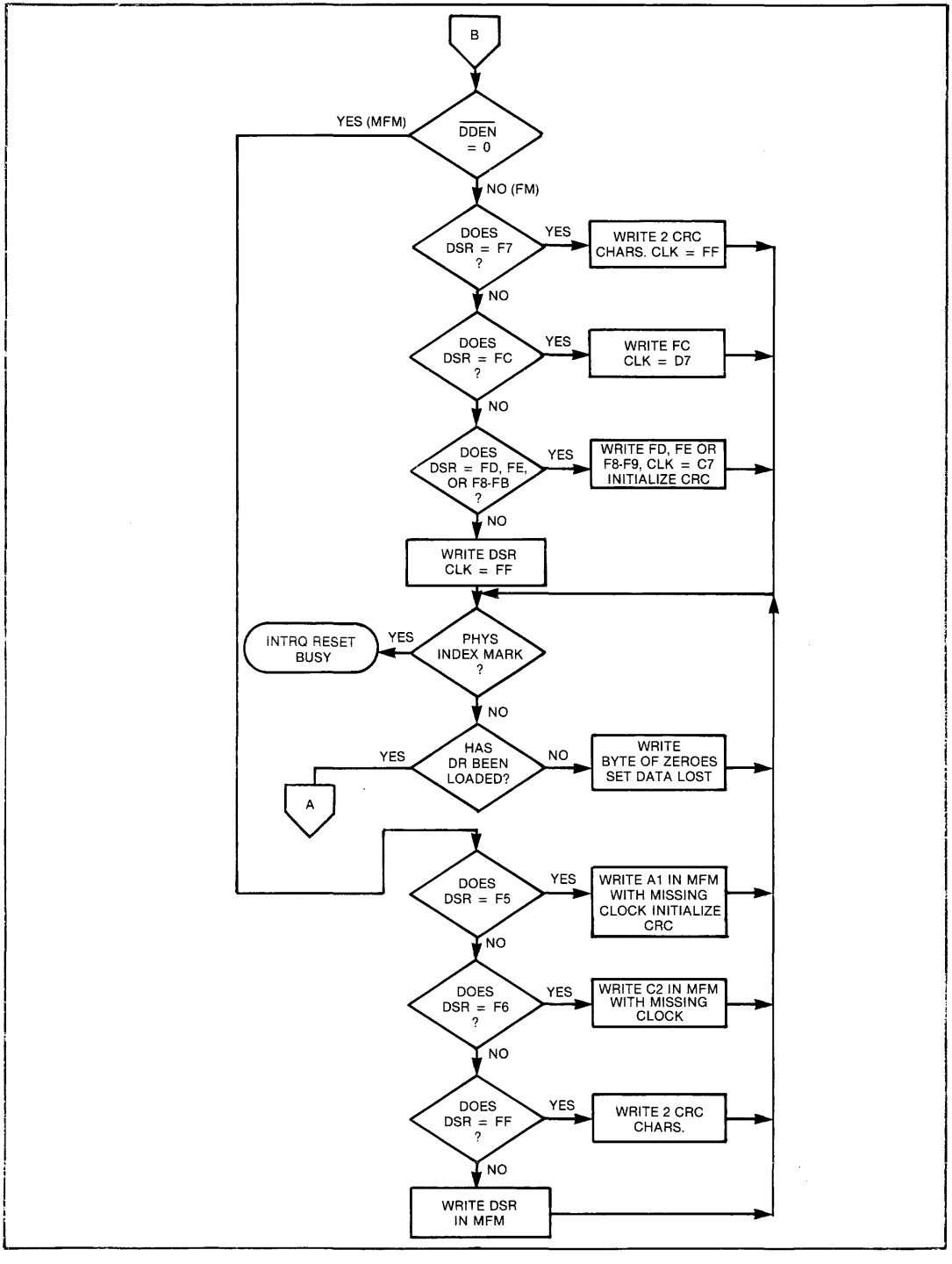
This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the WD1770 detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

DATA PATTERN IN DR (HEX)	IN FM ($\overline{DDEN}$ = 1)	IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.
**Missing clock transition between bits 3 and 4.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Don't Care
I_1 = Don't Care
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 micro sec (double density) or 32 micro sec (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

RECOMMENDED — 128 BYTES/SECTOR

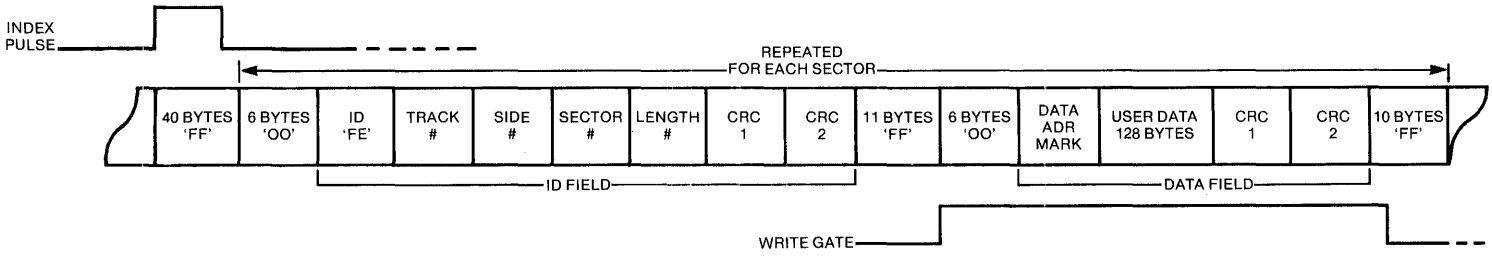
Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

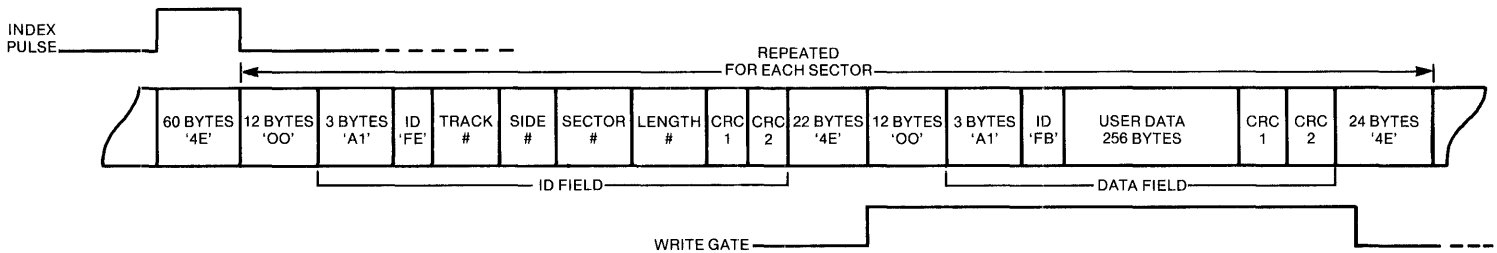
*Write bracketed field 16 times.
**Continue writing until WD1770 interrupts out. Approx. 369 bytes.

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.



SINGLE DENSITY FORMAT



DOUBLE DENSITY FORMAT

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRC's written)
24	4E
668**	4E

*Write bracketed field 16 times.
**Continue writing until WD1770 interrupts out. Approx. 668 bytes.

1. Non-Standard Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD1770 Gap 1, 3, and 4 lengths can be as short as 2 bytes for WD1770 operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

STATUS REGISTER DESCRIPTION

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (6 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA/ TRACK 00	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when update. On Type I commands, this bit reflects the status of the TRACK 00 Pin.
S1 DATA REQUEST/ INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type I commands, this bit indicates the status of the Index Pin.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to 70°C Ambient

Maximum Voltage to Any Input with Respect to V_{SS} ..... (−15 to −0.3V)

DC OPERATING CHARACTERISTICS

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_0 = -100\,\mu A$
V_{OL}	Output Low Voltage		0.40	V	$I_0 = 1.6$ mA
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	μA	$V_{IN} = 0V$
I_{CC}	Supply Current	75 (Typ)	150	mA	

AC TIMING CHARACTERISTICS

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ±.25V

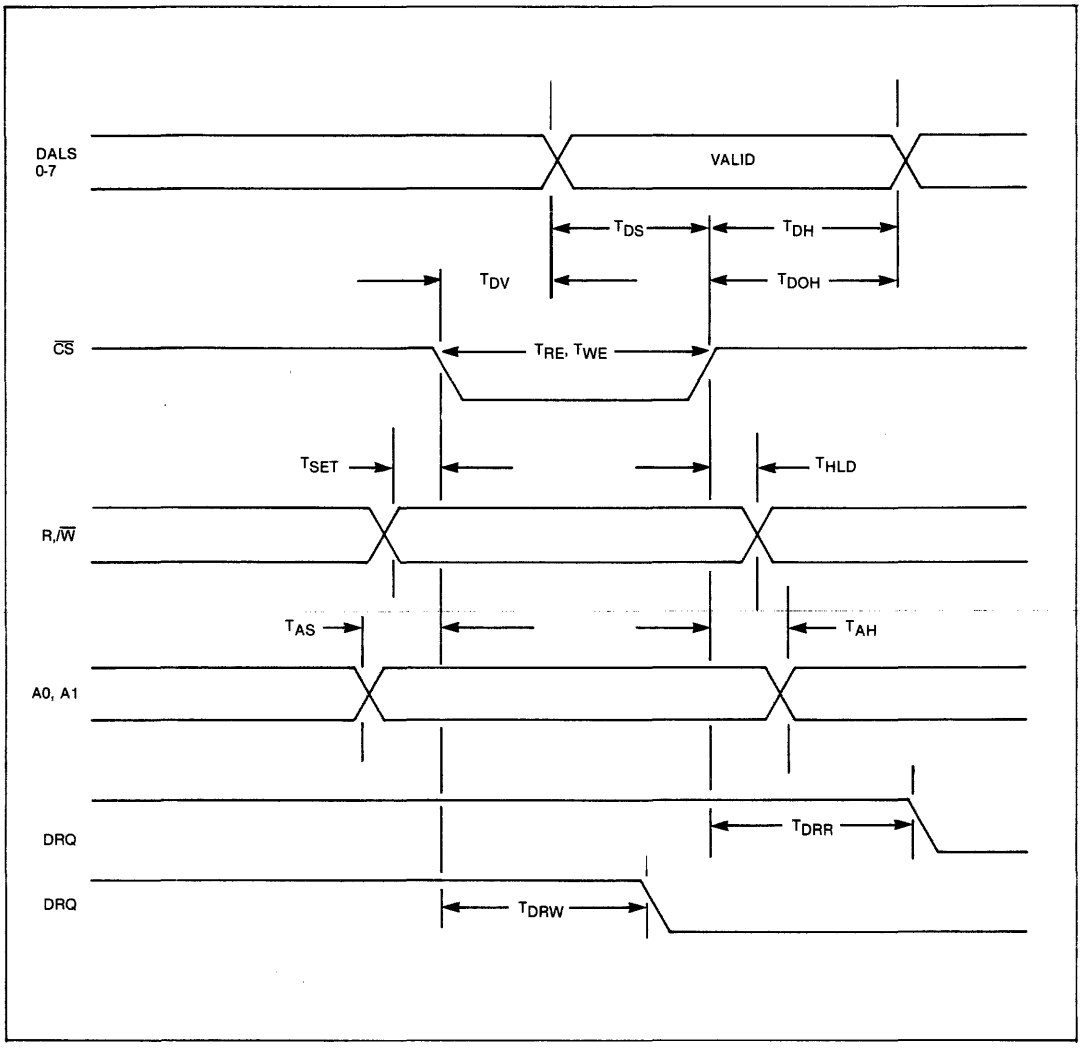
READ ENABLE TIMING — $\overline{RE}$ such that: R/$\overline{W}$ = 1, $\overline{CS}$ = 0.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TRE	RE Pulse Width of $\overline{CS}$	150			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		25	100	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			8000	nsec	
TDV	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 50 pf

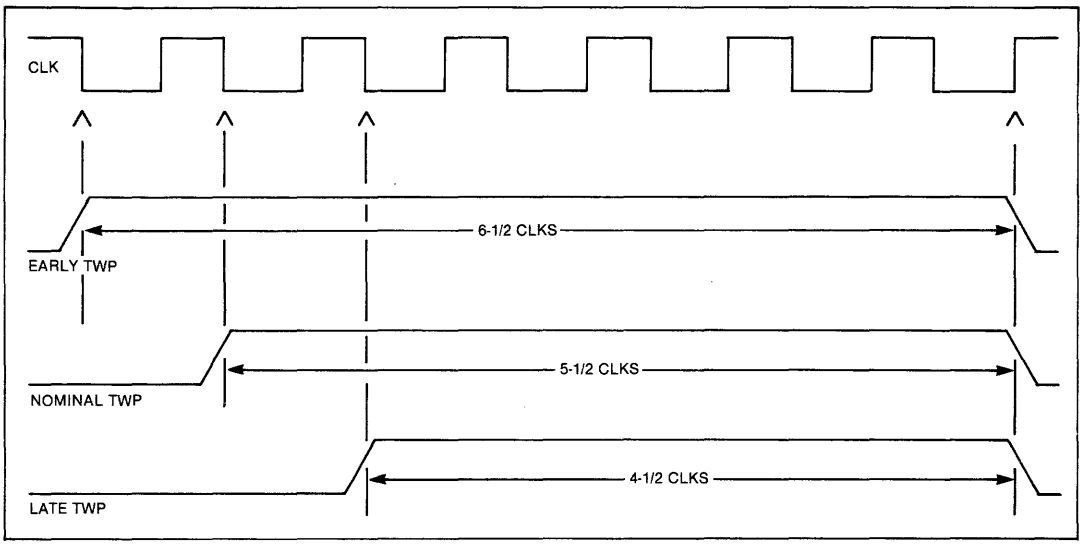
Note: DRQ and INTRQ reset are from rising edge (lagging) of $\overline{RE}$, whereas resets are from falling edge (leading) of $\overline{WE}$.

WRITE ENABLE TIMING — $\overline{WE}$ such that: R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TAS	Setup ADDR to $\overline{CS}$	50			nsec	
TSET	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
TAH	Hold ADDR from $\overline{CS}$	20			nsec	
THLD	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
TWE	$\overline{WE}$ Pulse Width	150			nsec	
TDRW	DRQ Reset from $\overline{WE}$		100	200	nsec	
TIRW	INTRQ Reset from $\overline{WE}$			8000	nsec	
TDS	Data Setup to $\overline{WE}$	150			nsec	
TDH	Data Hold from $\overline{WE}$	0			nsec	



REGISTER TIMINGS



WRITE DATA TIMING

WRITE DATA TIMING:

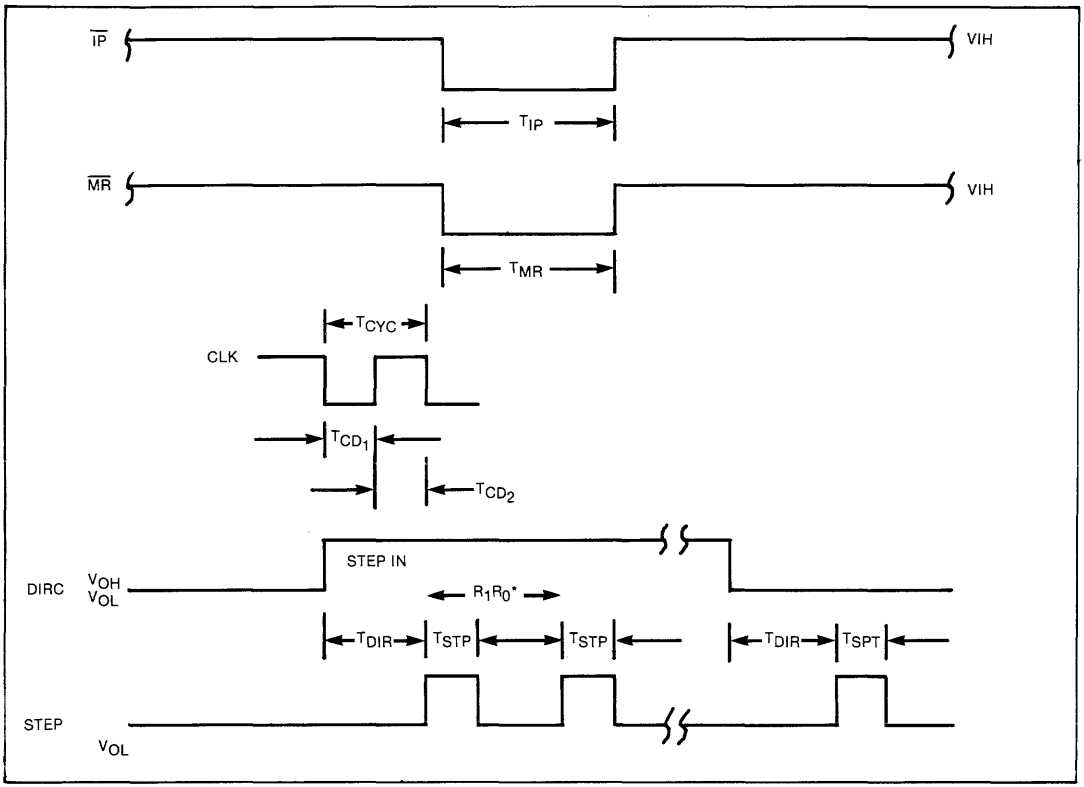
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twg	Write Gate to Write Data		4 2		µsec µsec	FM MFM
Tbc	Write Data Cycle Time		4,6,8		µsec	
Twf	Write Gate off from WD		4 2		µsec µsec	FM MFM
Twp	Write Data Pulse Width		820 690 570 1380		nsec nsec nsec nsec	Early MFM Nominal MFM Late MFM FM

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TPW	$\overline{\text{Raw Read}}$ Pulse Width	200			nsec	
TBC	$\overline{\text{Raw Read}}$ Cycle Time	3000			nsec	

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	50	67		nsec	
TCD_2	Clock Duty (high)	50	67		nsec	
TSTP	Step Pulse Output		4 8		µsec	MFM FM
TDIR	Dir Setup to Step		24 48		µsec	MFM FM
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	20			µsec	



MISCELLANEOUS TIMING

See page 481 for ordering information.

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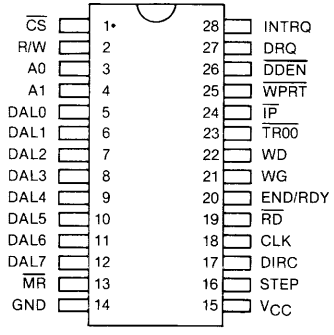
ADVANCED INFORMATION

WD1773 5¼" Floppy Disk Controller/Formatter

FEATURES

- 100% SOFTWARE COMPATIBILITY WITH WD1793
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- SINGLE (FM) AND DOUBLE (MFM) DENSITY
- 28 PIN DIP, SINGLE +5V SUPPLY
- TTL COMPATIBLE INPUTS/OUTPUTS
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- 8-BIT BI-DIRECTIONAL HOST INTERFACE



PIN DESIGNATION

DESCRIPTION

The WD1773 is an MOS/LSI device which performs the functions of a 5¼" Floppy Disk Controller/Formatter. It is fully software compatible with the Western Digital WD1793-02, allowing the designer to reduce parts count and board size on an existing WD1793 based design without software modifications.

With the exception of the enable Precomp/Ready line, the WD1773 is identical to the WD1770 controller. This line serves as both a READY input from the drive during READ/STEP operations, and as a Write Precompensation enable during Write operations. A built-in digital data separator virtually eliminates all external components associated with data recovery in previous designs.

The WD1773 is implemented in NMOS silicon gate technology and is available in a 28 pin, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enable Host communication with the device.
2	READ/WRITE	R/$\overline{W}$	A logic high on this input controls the placement of data on the $\overline{D0}$-$\overline{D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	ADDRESS 0,1	A0, A1	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DATA ACCESS LINES 0 THROUGH 7	DAL0-DAL7	Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line will drive one TTL load.
13	MASTER RESET	$\overline{MR}$	A logic low pulse on this line resets the device and initializes the status register.
14	GROUND	GND	Ground.
15	POWER SUPPLY	V_{CC}	+5V ±5% power supply input.
16	STEP	STEP	The Step output contains a pulse for each step of the drive's R/$\overline{W}$ head. The WD1770 and WD1772 offer different step rates.
17	DIRECTION	DIRC	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLOCK	CLK	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHZ ± 1%.
19	READ DATA	$\overline{RD}$	This active low input is the raw data line containing both clock and data pulses from the drive.
20	ENABLE PRECOMP/ READY LINE	ENP/RDY	Serves as a READY input from the drive during READ/STEP operations and as a Write Precomp enable during write operations.
21	WRITE GATE	WG	This output is made valid prior to writing on the diskette.
22	WRITE DATA	WD	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	TRACK 00	$\overline{TR00}$	This active low input informs the WD1770 that the drive's R/$\overline{W}$ heads are positioned over Track zero.
24	INDEX PULSE	$\overline{IP}$	This active low input informs the WD1770 when the physical index hole has been encountered on the diskette.
25	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing.
26	DOUBLE DENSITY ENABLE	$\overline{DDEN}$	This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN}$ = 0, double density is selected.

PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	DATA REQUEST	DRQ	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTERRUPT REQUEST	INTRQ	This active high output is set at the completion of any command or reset a read of the Status Register.

See page 481 for ordering information.

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WD1770/72/73 5¼" Floppy Disk Controller/Formatter Family Application Notes

INTRODUCTION

To meet the demand for a low cost compact LSI Floppy Disk Controller device, Western Digital has developed the WD1770. The WD1770 is a NMOS floppy disk controller device for 5¼" drives that incorporates the FD179X, a digital data separator and write precompensation circuitry all in a single chip. The device offers soft sector formatting, selectable stepping rates, automatic track seek with verify, and variable sector lengths. The FD1770 comes in a 28-pin dual-in-line package and operates from a single 5 volt only power supply.

APPLICATIONS

The mini-floppy controller is targeted for the low cost sector of the disk drive market, where digital data separation is preferred over analog phase lock loop. Included in this market are Personal Computers, Portable Computers and Small Business Computers.

FOLLOW ON DEVICES

WD1772

The device will be the same as the WD1770 except for increased stepping rates of 2, 3, 5 and 6ms.

WD1773

The device will be the same as the WD1770 except that it will be totally software compatible with the FD179X (No motor on feature).

HOST INTERFACING

Interfacing to a host processor is accomplished through the eight bit bidirectional Data Access Lines (DAL) and associated control lines. The DAL is used to transfer data, status and control words out of or into WD1770. The DAL having three states enabled as an output when Chip Select ($\overline{CS}$) is active low and Read/$\overline{Write}$ (R/$\overline{W}$) is high or as input receiver when $\overline{CS}$ and R/$\overline{W}$ is low. When transfer of data with the device is required by the host $\overline{CS}$ is made low. The address bits A0 and A1 combined with the R/$\overline{W}$ line select the register and direction of data.

During Direct Memory Access (DMA) data transfers between the WD1770 and Host Memory, the Data Request (DRQ) line is used in Data Transfer Control. This signal also appears as status bit 1 during Read/Write operations. On Disk Read operations the DRQ is active when an assembled byte is present in the Data Register, then reset when read by the Host. If the Host fails to read the Data register before the following byte is assembled in the data register the lost data bit is set in Status Register.

At the completion of every command INTRQ is generated. INTRQ is reset by either reading the status or by loading the command register. (After any register is written to the same register cannot be read from until 16μsec in MFM or 32μsec in FM have elasped.)

DISKETTE DRIVE INTERFACING

The WD1770 has two modes of operation depending on the state of DDEN, regardless of the state DDEN the CLK input remains at 8 MHz. Disk Reads with sector lengths of 128, 256, 512 and 1024 byte sector in both FM or MFM from 5¼" diskettes is accomplished via the internal digital data separator. Disk Write operation in MFM on inner tracks may require write precompensation. Write precompensation is enabled when bit 1 = 0, in the write command and a precompensation value of 125 ns will be produced.

The diskettes spindle motor is controlled by bit 3 of any Type I, II or III command, upon receiving a command with bit 3 = 0, the spin up sequence is enabled.

GENERAL INFORMATION

A +5 volt supply ±5% should be used as V_{CC}, and the clock input requires a free running 50% duty cycle at 8 MHz ± 1%.

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WESTERN DIGITAL
CORPORATION

FD179X-02
Floppy Disk Formatter/Controller Family

FEATURES

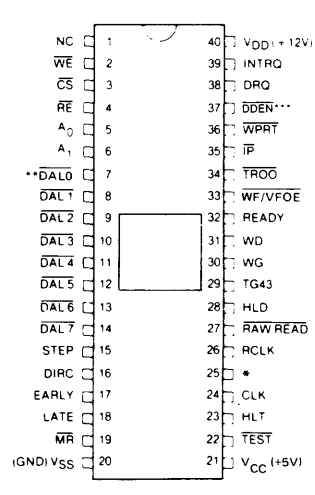
- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- INTERFACES TO WD1691 DATA SEPARATOR
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus			X	X		X
Inverted Data Bus	X	X			X	
Write Precomp	X	X	X	X	X	X
Side Selection Output					X	X

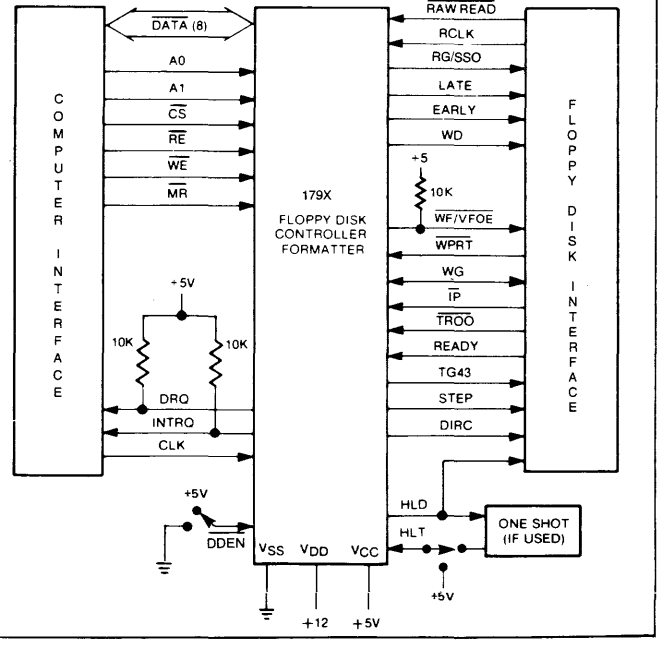
APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS
***1792/4 OPEN

PIN DESIGNATION



FD179X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ±1% for mini-floppies.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1791, 1792, 1793, 1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	$\overline{IP}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected. This line must be left open on the 1792/4.

GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

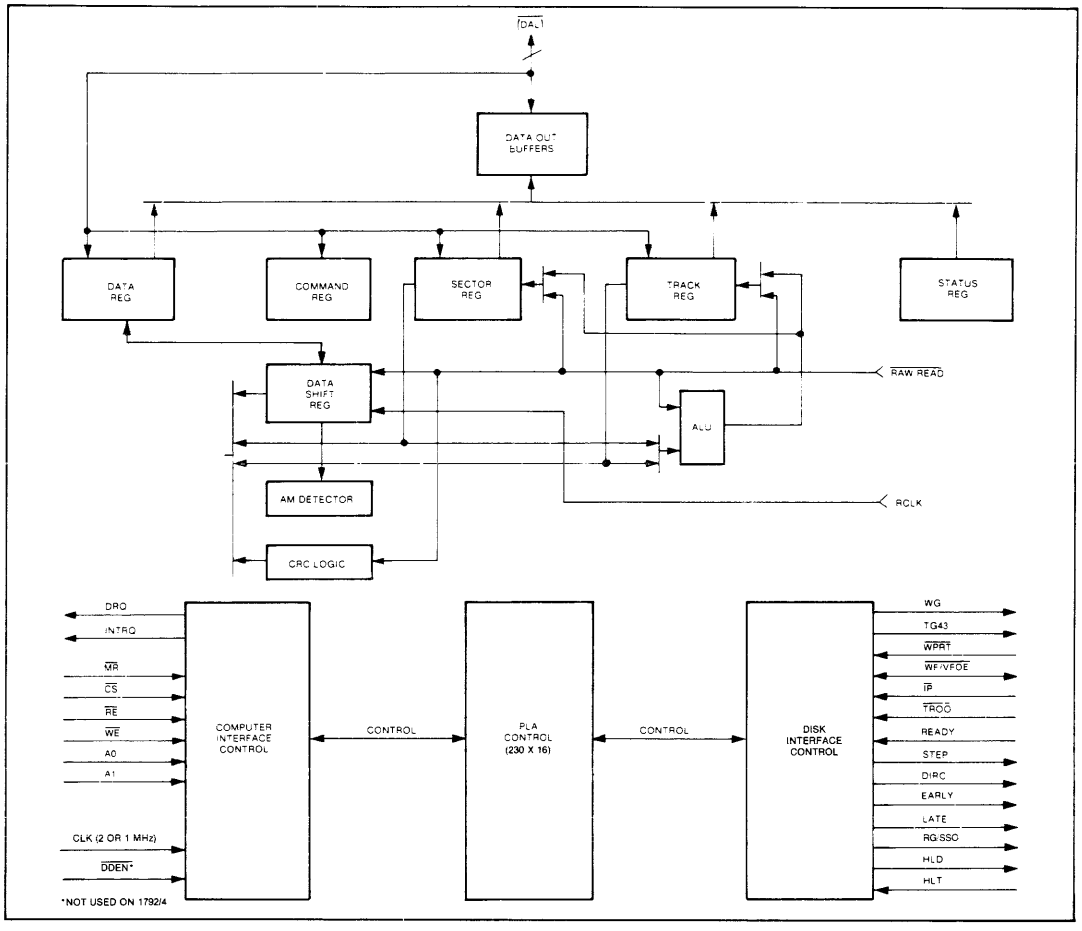
CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single



FD179X BLOCK DIAGRAM

density (FM) is assumed. 1792 & 1794 are single density only.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1 - A0		READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data

Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations in 8" double density the FD179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 200 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1791, 1792, 1793, 1794

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 1795, 1797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 1, Load head at beginning h = 0, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r0 r1), which determines the stepping motor rate as defined in Table 3.

A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK		2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$		0	1	0	1	X	X
R1	R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0	0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0	1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1	0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1	1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

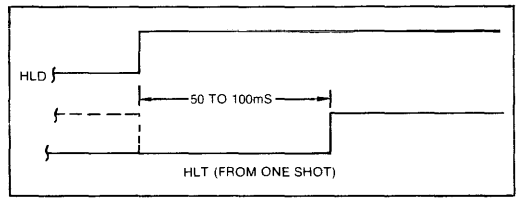
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

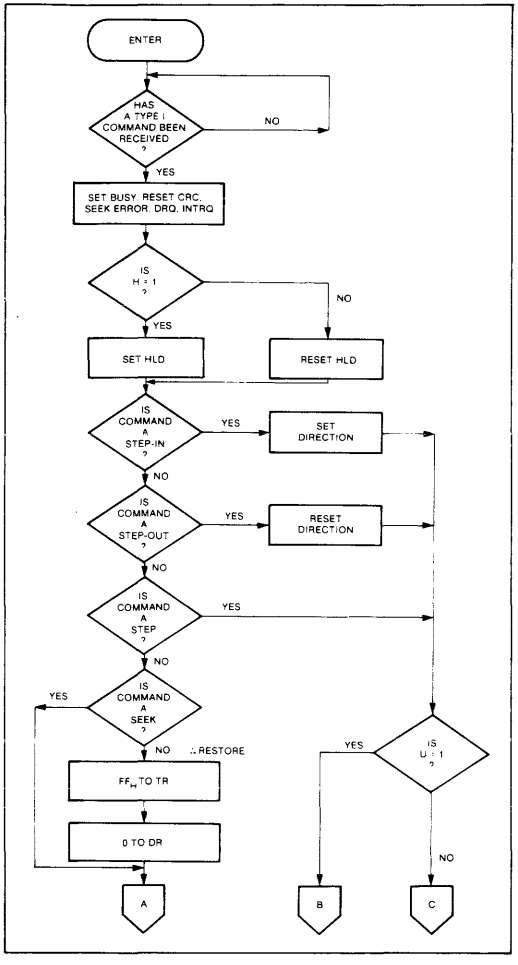
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

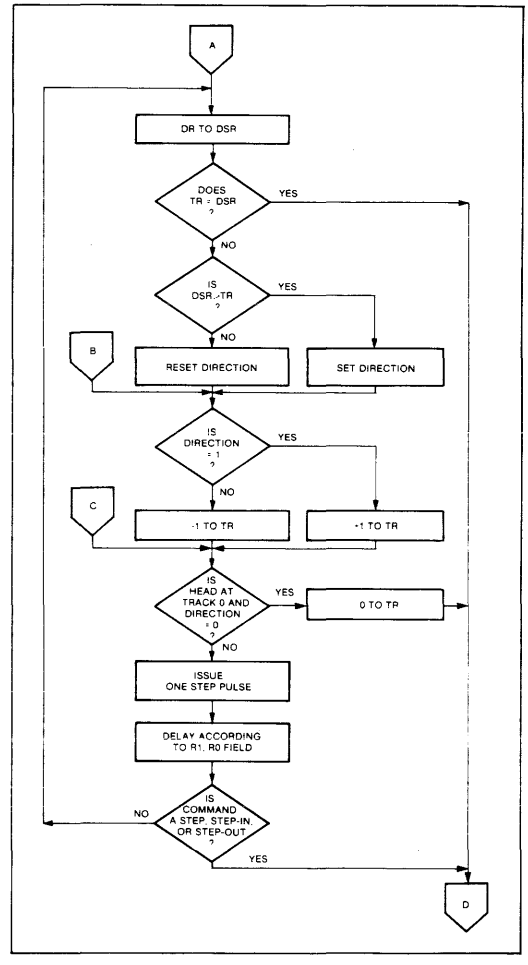
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1 r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

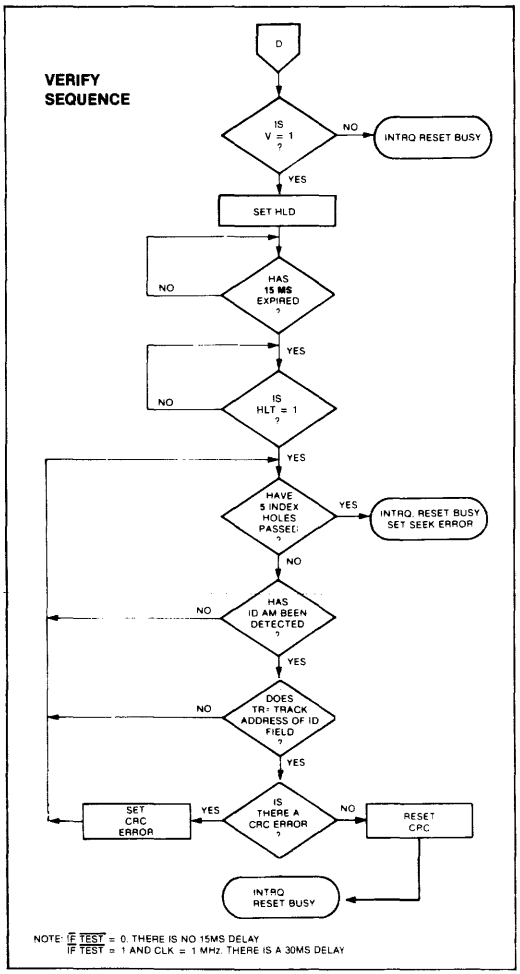
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

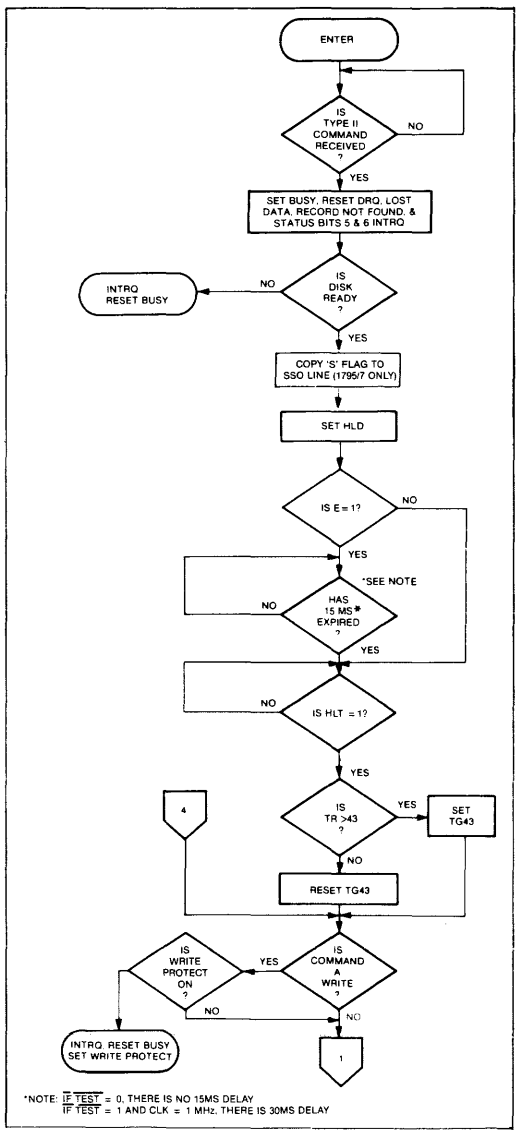


TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next

record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

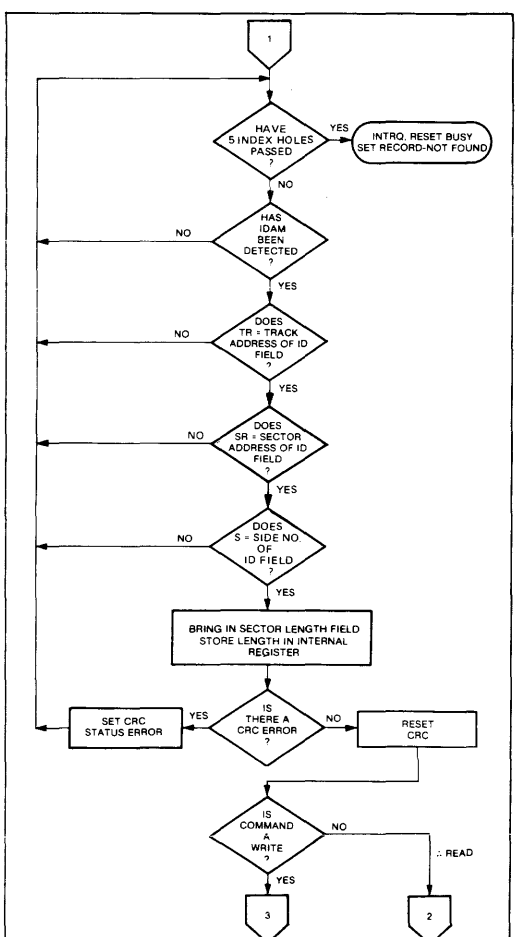
The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

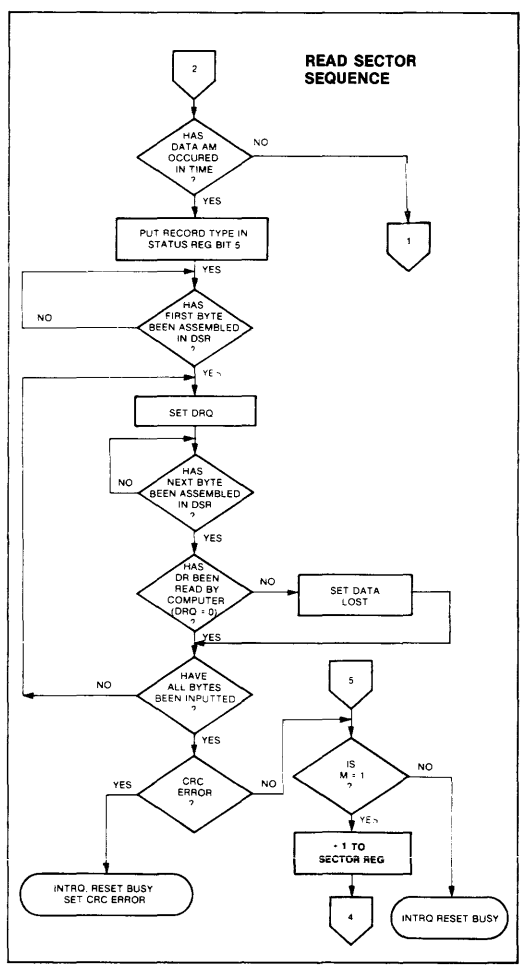
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'L' flag should be set to a one.

READ SECTOR

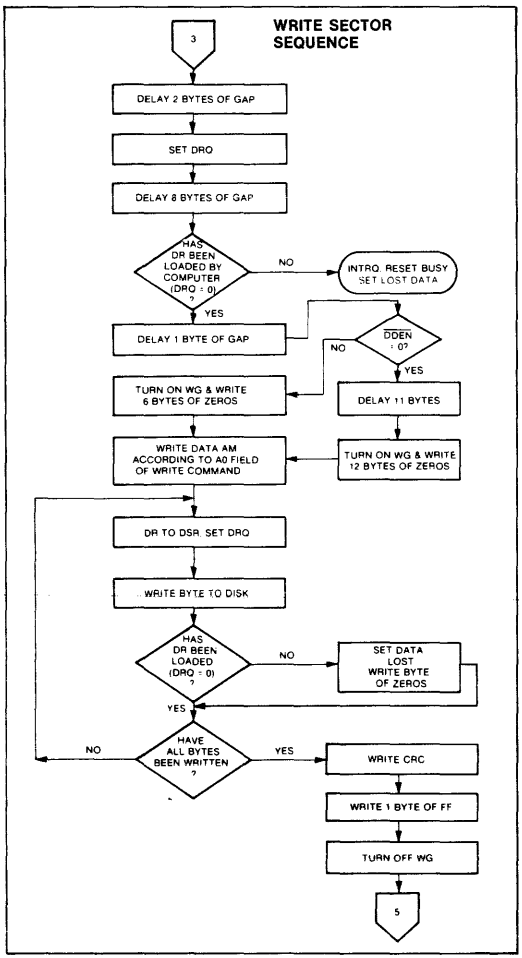
Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address



TYPE II COMMAND



TYPE II COMMAND



TYPE II COMMAND

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

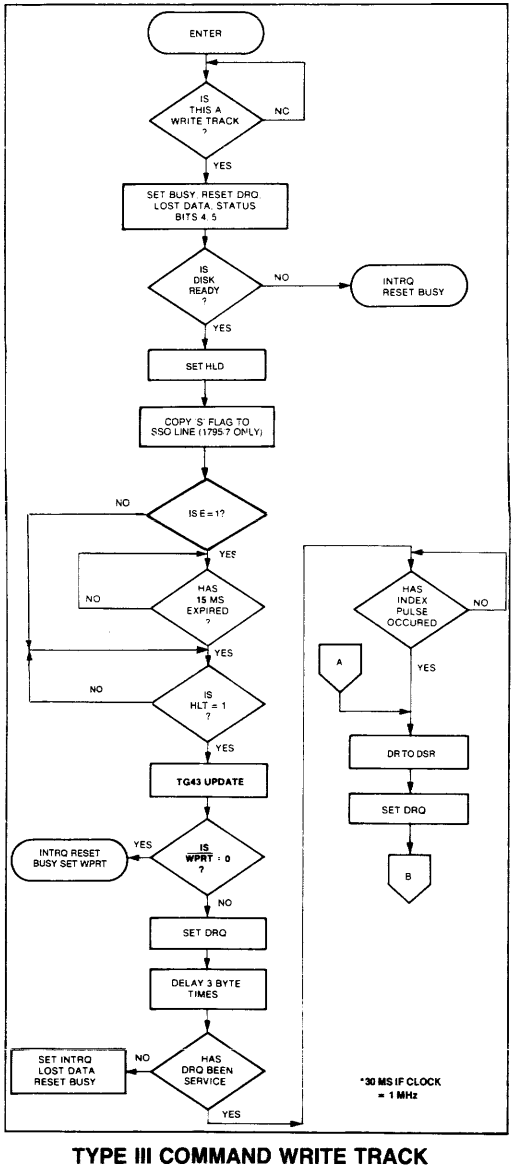
Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

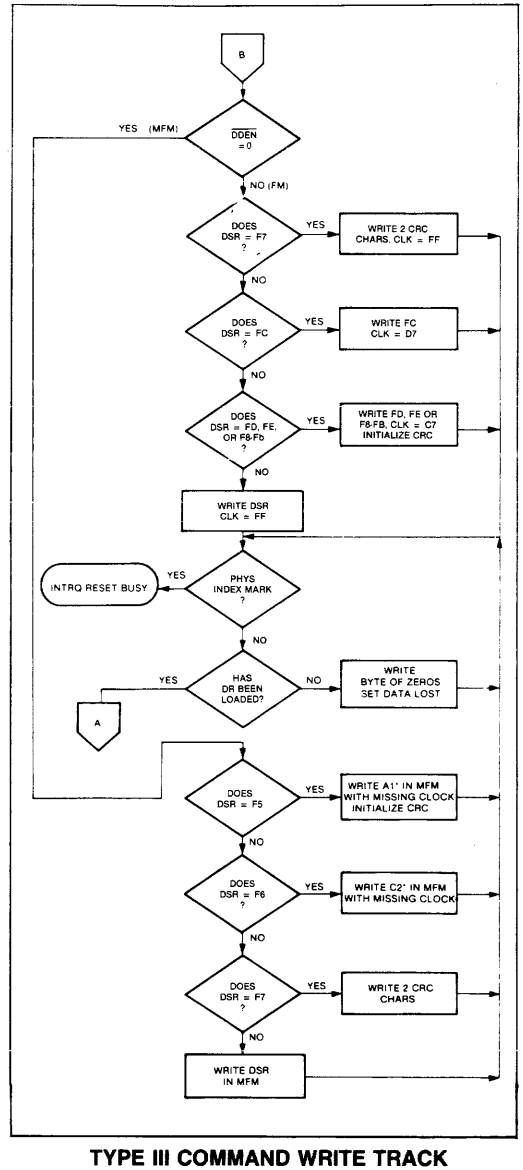
Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

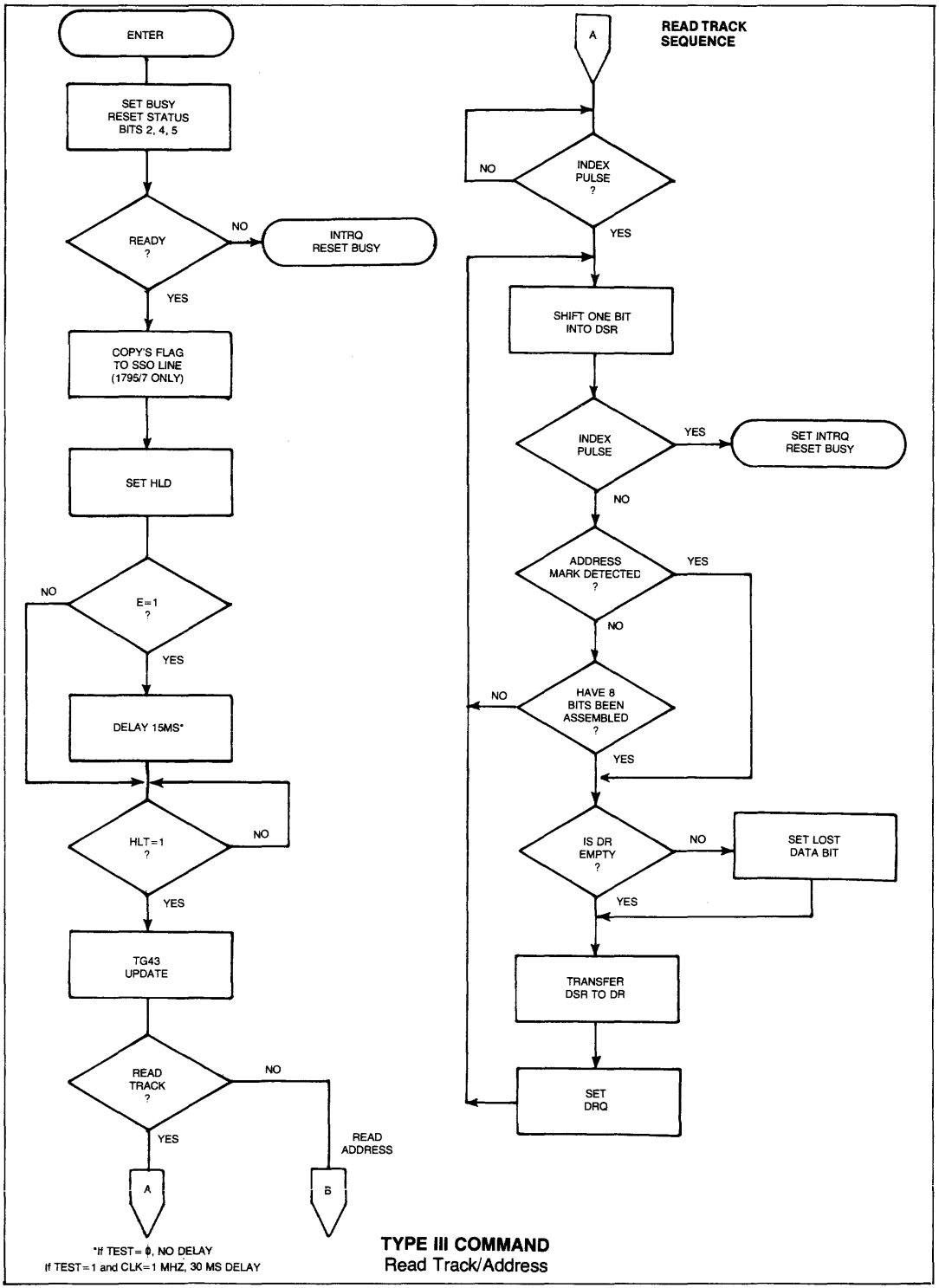
I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

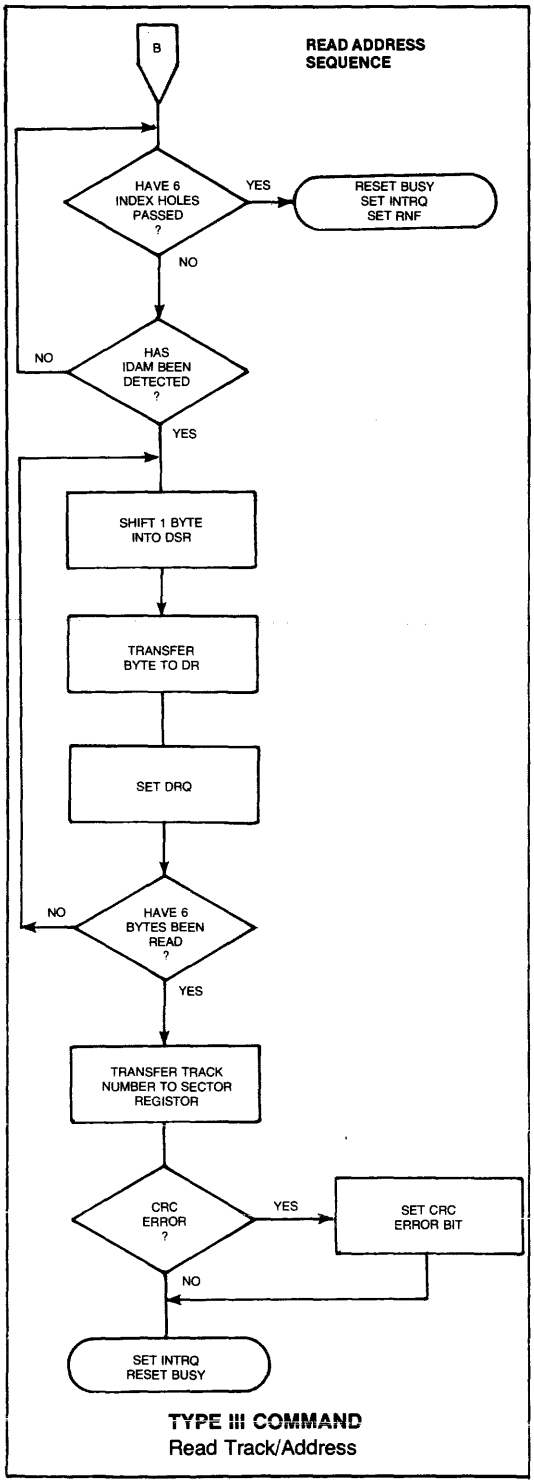
Wait 8 micro sec (double density) or 16 micro sec (single density before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT- READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	Delay Req'd. MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs
Write to Command Reg.	Read Status Bits 1-7	28 μs	14 μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF (or 00)[1]
	6	00
	1	FC (Index Mark)
*	26	FF (or 00)[1]
	6	00
	1	FE (ID Address Mark)
	1	Track Number
	1	Side Number (00 or 01)
	1	Sector Number (1 thru 1A)
	1	00 (Sector Length)
	1	F7 (2 CRC's written)
	11	FF (or 00)[1]
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	FF (or 00)[1]
	247**	FF (or 00)[1]

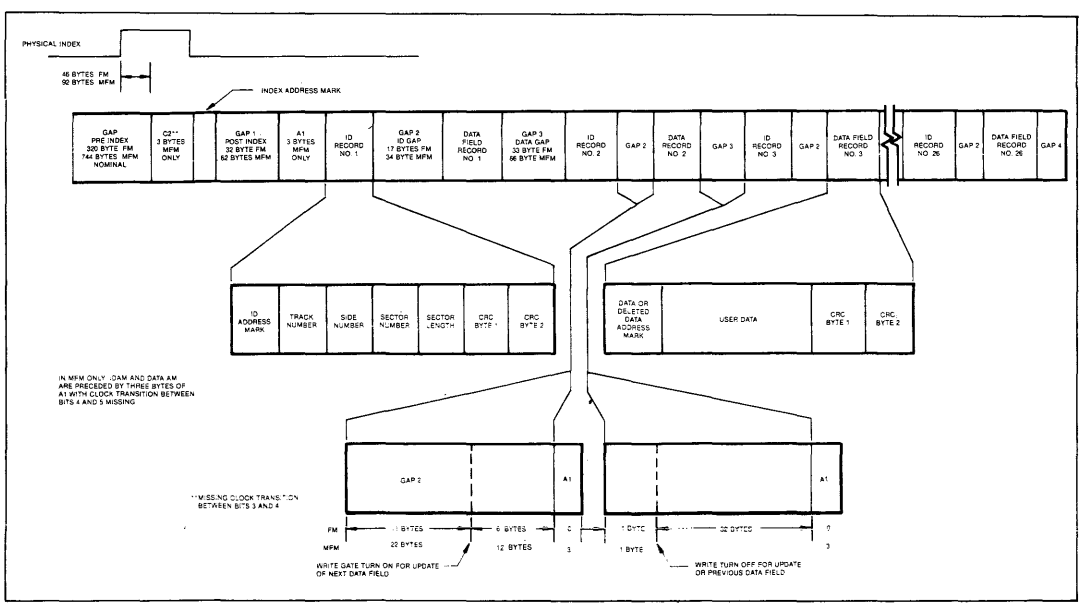
*Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 247 bytes.
1-Optional '00' on 1795/7 only.

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	80	4E
	12	00
	3	F6 (Writes C2)
	1	FC (Index Mark)
*	50	4E
	12	00
	3	F5 (Writes A1)
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (1 thru 1A)
	1	01 (Sector Length)
	1	F7 (2 CRCs written)
	22	4E
	12	00
	3	F5 (Writes A1)
	1	FB (Data Address Mark)
	256	DATA
	1	F7 (2 CRCs written)
	54	4E
	598**	4E

*Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 or 1024 bytes.

2) Gap 2 cannot be varied from the IBM format.

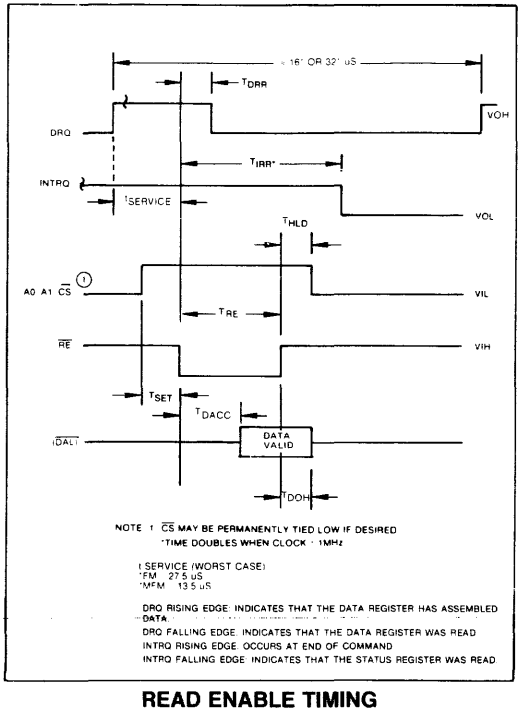
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



READ ENABLE TIMING

TIMING CHARACTERISTICS

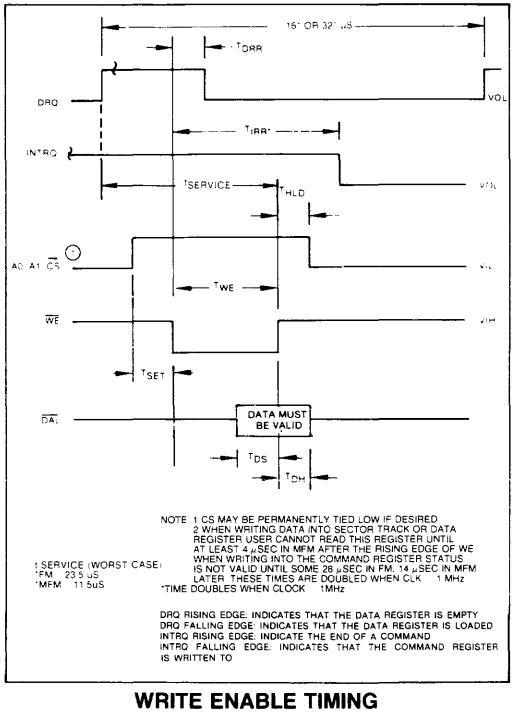
T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING (See Note 6, Page 21)

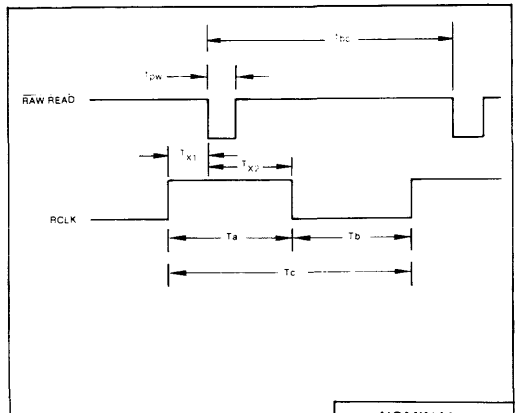
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	



WRITE ENABLE TIMING



				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_a	T_b	T_c
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2μs	4 μs
5"	MFM	0	1 MHz	2 μs	2μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

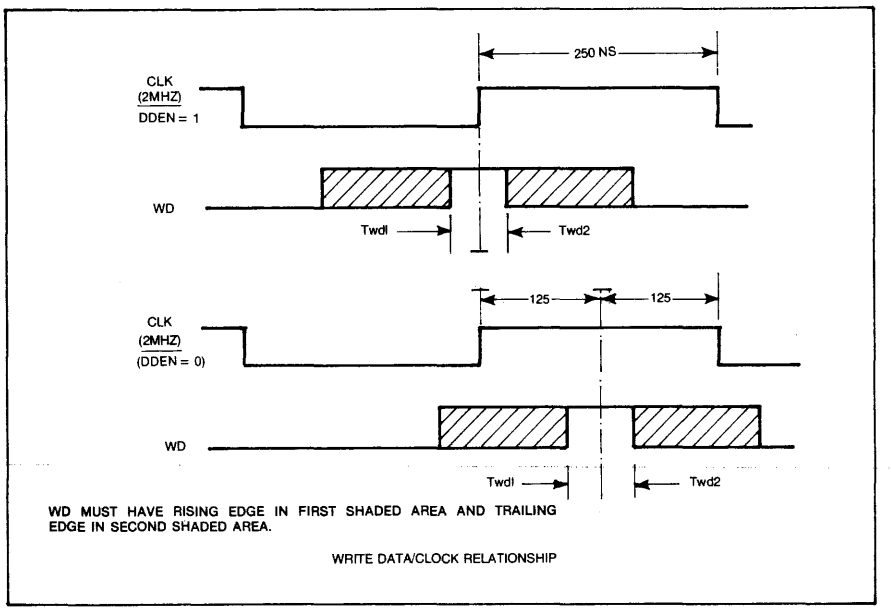
INPUT DATA TIMING

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
T_{X1}	RCLK hold to $\overline{\text{Raw Read}}$	40			nsec	See Note 1
T_{X2}	$\overline{\text{Raw Read}}$ hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (See Note 6, Page 21)

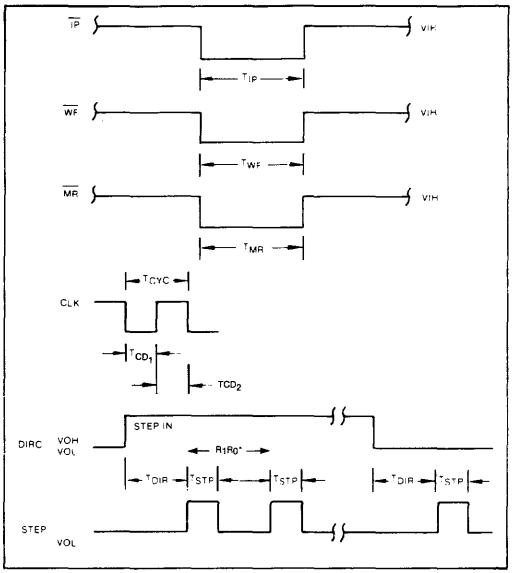
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width		500	**650**	nsec	FM
			200	**350**	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twdl	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ



WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	See Note 5
TDIR	Dir Setup to Step		12		μsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	See Note 5
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{DD} with repect to V_{SS} (ground): + 15 to − 0.3V

Voltage to any input with respect to V_{SS} = + 15 to − 0.3V

I_{CC} = 60 MA (35 MA nominal)

I_{DD} = 15 MA (10 MA nominal)

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.

Operating temperature = 0°C to 70°C

Storage temperature = − 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{DD}**
I_{OL}	Output Leakage		10	μA	V_{OUT} = V_{DD}
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = − 100 μA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.6 mA*
P_D	Power Dissipation		0.6	W	

*1792 and 1794 I_O = 1.0 mA

**Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pull-up resistors. See Tech Memo #115 for testing procedures.

See page 481 for ordering information.

FD179X Application Notes

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be *the* solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte sychronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5¼" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexidecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A_1	PIN 5 A_0	PIN 4 $\overline{RE}=\emptyset$	PIN 2 $\overline{WE}=\emptyset$
0	0	0	STATUS REG	COMMAND
0	0	1	TRACK REG	REG
0	1	0	SECTOR REG	TRACK REG
0	1	1	DATA REG	SECTOR REG
1	X	X	H1-Z	DATA REG
				H1-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A_0, A_1, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14μs* FM = 28μs*
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive)

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2MHz (8" drive) or 1MHz (5¼" drive) with a 50% duty cycle. Accuracy should be ±1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TROO}$ line to go active low. This line should be connected to the drive's $\overline{TROO}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed −0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. *sensor* and makes an active transition for each revolution of the diskette. The $\overline{TROO}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5¼"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5¼" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When $\overline{DDEN}$ is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

There are two methods of performing Write Precompensation:

1) External Delay elements
2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the Ø1, Ø2 and Ø3 signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, Ø1 will be used for EARLY, Ø2 for nominal (EARLY = LATE = 0), and Ø3 for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The Ø4 output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2MHz and 4MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4MHz clock is shifting "ones" through the shift register and maintaining Q_D at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4MHz clock until it reaches the Q_D output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zeros or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of '5'. When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the Q_D output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK ÷ 2. If VFO CLK ÷ 2 is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO.

If, correspondingly, CLK ÷ 2 is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

Free Running Frequency	2MHz
Capture Range	± 15%
Lock Up Time	50 microsec. "1111" or "0000" Pattern 100 Microsec "1010" Pattern

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK ÷ 2 OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TROO line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TROO. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

TRACK	SIDE	SECTOR	CRS LENGTH	CRC 1	CRC 2

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

I_0 = NOT-READY TO READY TRANSITION
I_1 = READY TO NOT-READY TRANSITION
I_2 = EVERY INDEX PULSE
I_3 = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command ($I_3 - I_0$) are set to a 1. If $I_3 - I_0$ are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX D0).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition (I_3 = 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with $I_3 - I_0 = 0$ must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5¼″	SINGLE	1	3125	109,375*	64μs	2304**	80,640
5¼″	DOUBLE	1	6250	218,750	32μs	4608***	161,280
5¼″	SINGLE	2	3125	218,750	64μs	2304	161,280
5¼″	DOUBLE	2	6250	437,500	32μs	4608	322,560
8″	SINGLE	1	5208	401,016	32μs	3328	256,256
8″	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8″	SINGLE	2	5208	802,032	32μs	3328	512,512
8″	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

*Based on 35 Tracks/Side
**Based on 18 Sectors/Track (128 byte/sec)
***Based on 18 Sectors/Track (256 bytes/sec)

FIGURE 3. NOMINAL VS. WORSE CASE SERVICE TIME

SIZE	DENSITY	NOMINAL TRANSFER TIME	WORST-CASE 179X SERVICE TIME	
			READ	WRITE
5¼"	SINGLE	64μs	55.0μs	47.0μs
5¼"	DOUBLE	32μs	27.5μs	23.5μs
8"	SINGLE	32μs	27.5μs	23.5μs
8"	DOUBLE	16μs	13.5μs	11.5μs

FIGURE 4A. FM RECORDING

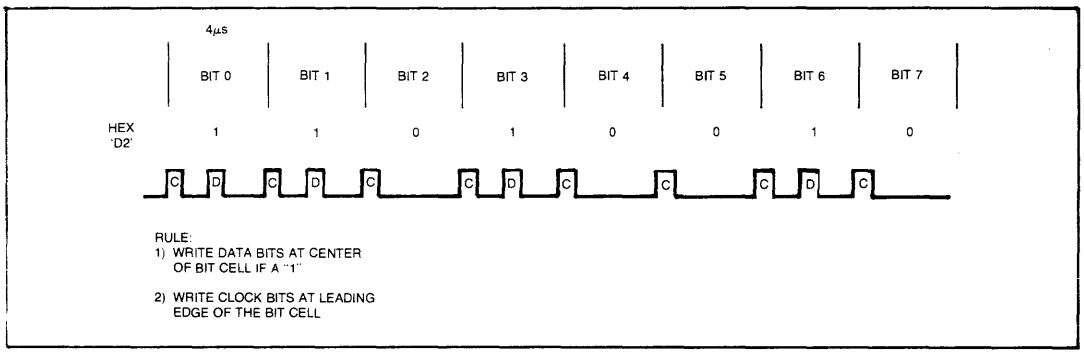


FIGURE 4B. MFM RECORDING

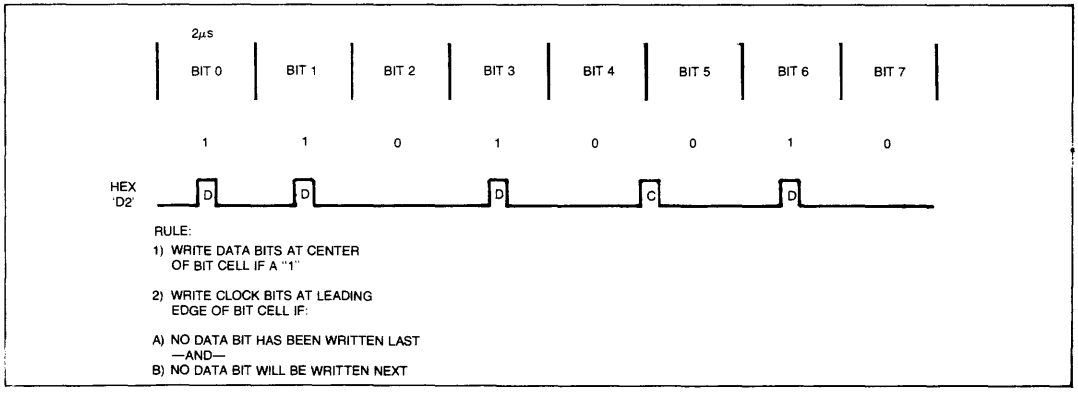
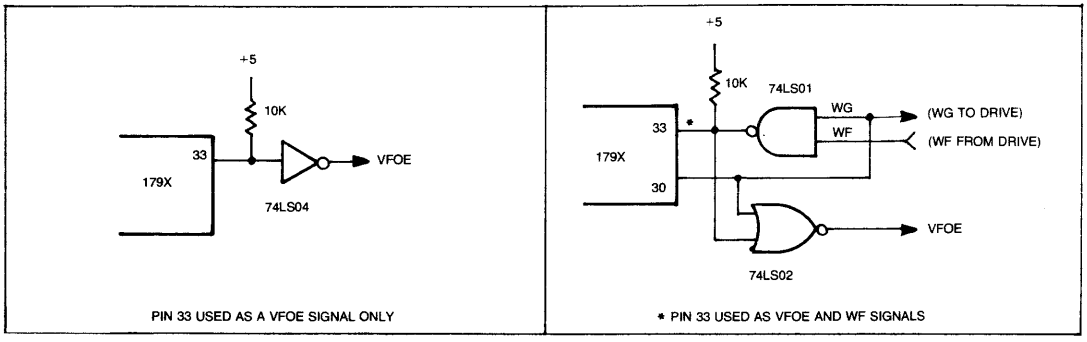


FIGURE 5. WF/VFOE DEMULTIPLEXING CIRCUITRY



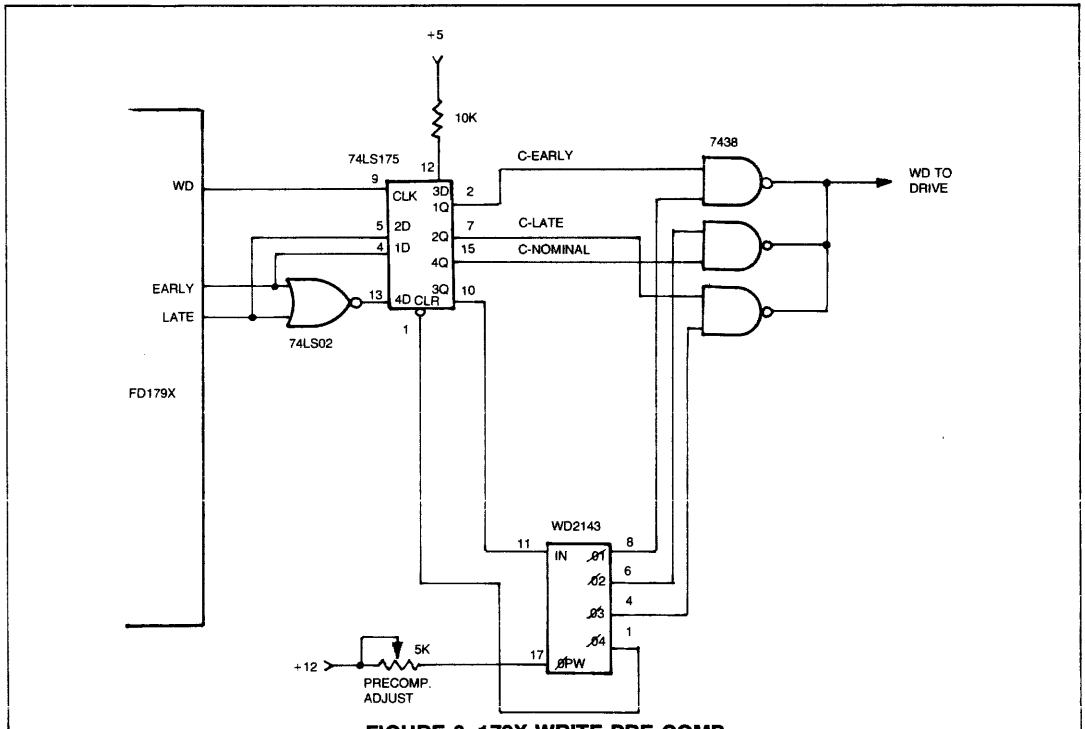


FIGURE 6. 179X WRITE PRE-COMP

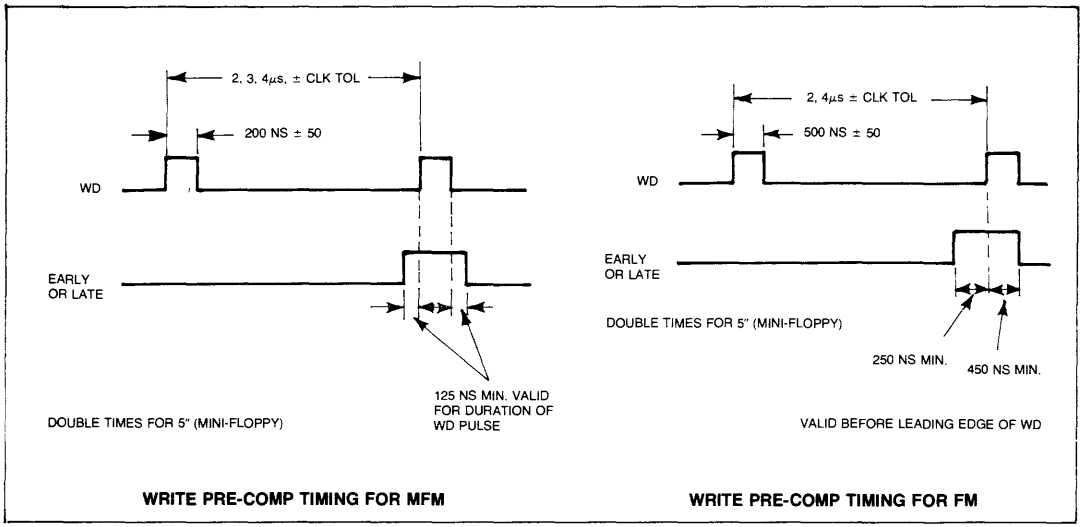


FIGURE 7. WRITE PRE-COMP TIMING

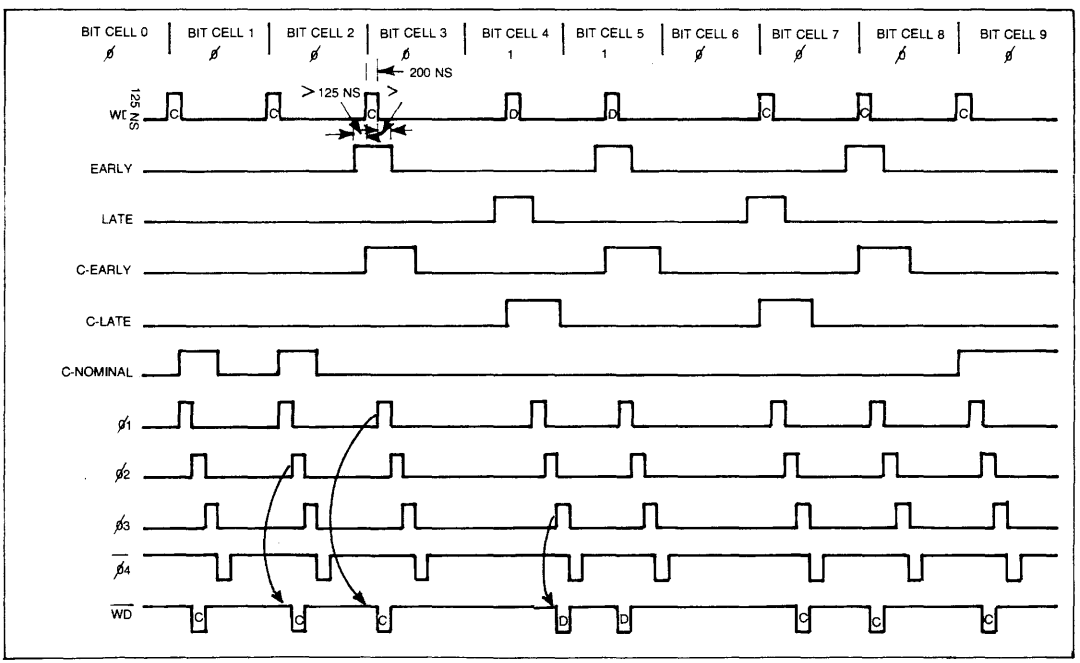


FIGURE 8. PRECOMP TIMING FOR CIRCUIT IN FIGURE 6

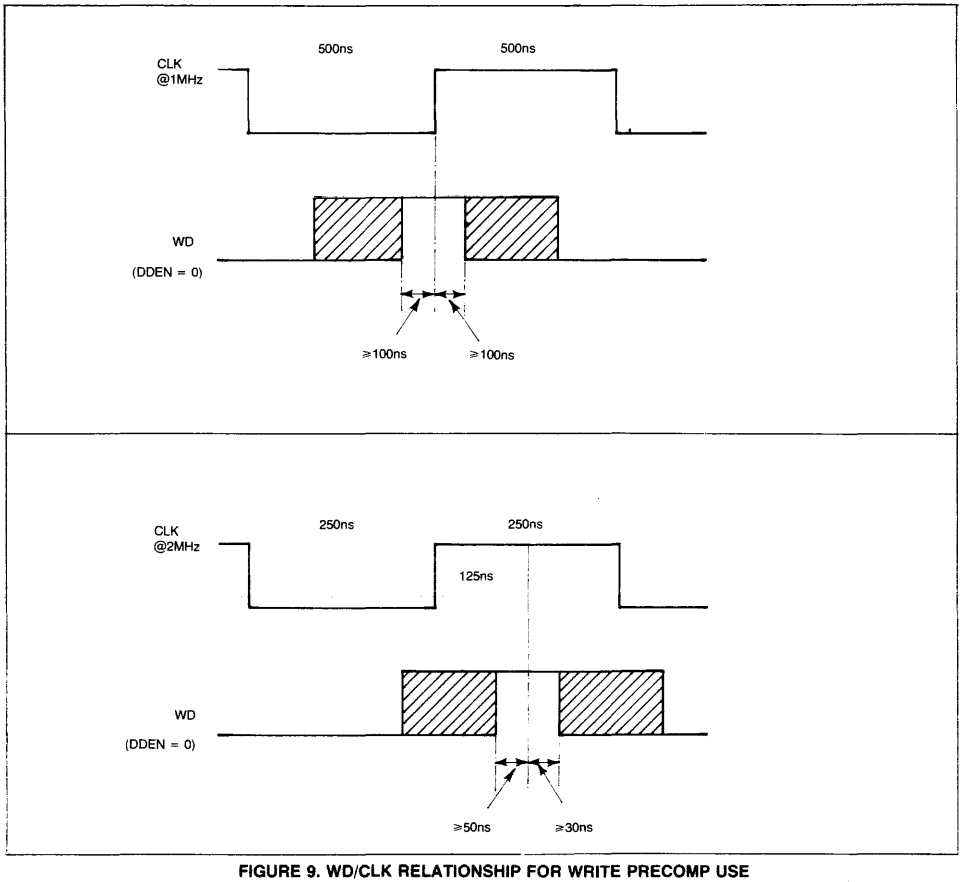


FIGURE 9. WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE

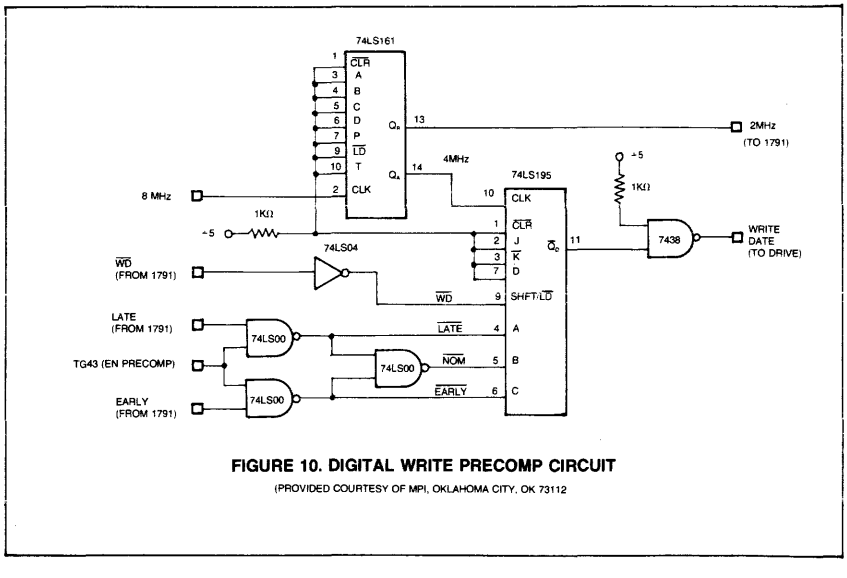
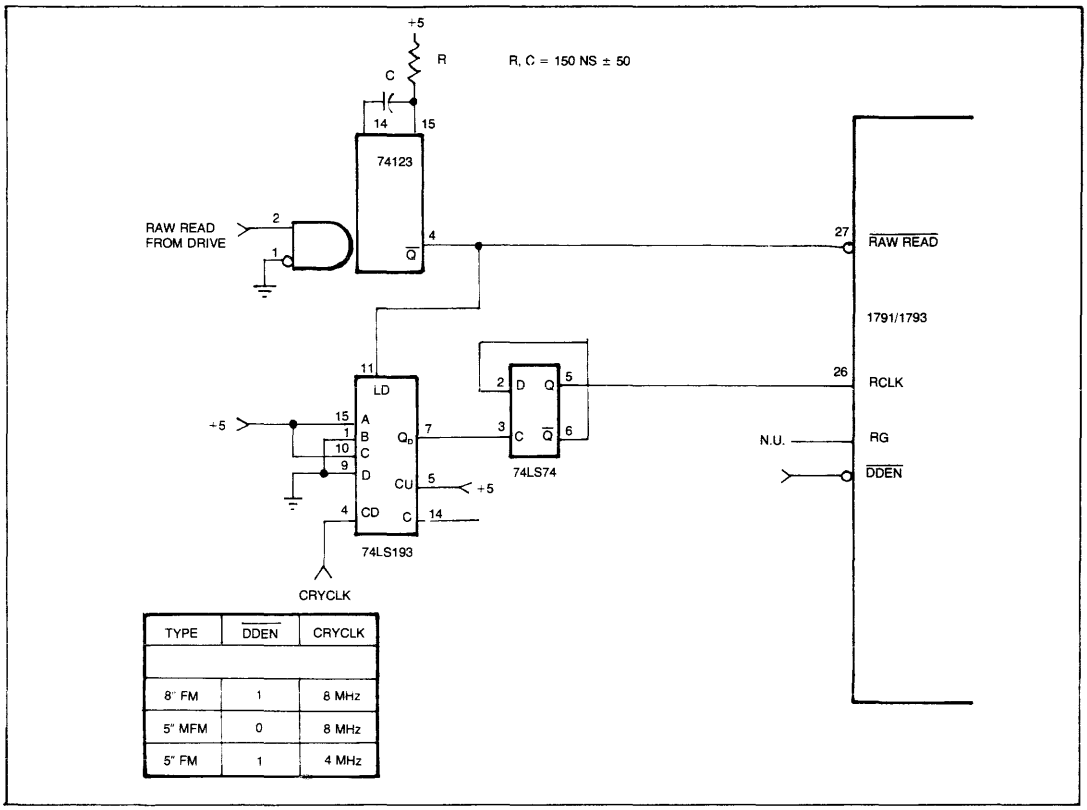


FIGURE 10. DIGITAL WRITE PRECOMP CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112



TYPE	$\overline{\text{DDEN}}$	CRYCLK
8" FM	1	8 MHz
5" MFM	0	8 MHz
5" FM	1	4 MHz

FIGURE 11. COUNTER/SEPARATOR

745288 PROGRAMMING TABLE

ADDRESS	DATA	ACTION TAKEN
00	01	NONE
01	01	RETARD BY 1 COUNT
02	02	
03	03	
04	03	RETARD BY 2 COUNTS
05	04	
06	05	
07	06	
08	0B	ADVANCE BY 2 COUNTS
09	0D	
0A	0C	
0B	0E	
0C	0F	
0D	0F	ADVANCE BY 1 COUNT
0E	00	
0F	01	
10	01	FREE RUN
11	02	
12	03	
13	04	
14	05	
15	06	
16	07	
17	08	
18	09	
19	0A	
1A	0B	
1B	0C	
1C	0D	
1D	0E	
1E	0F	
1F	00	

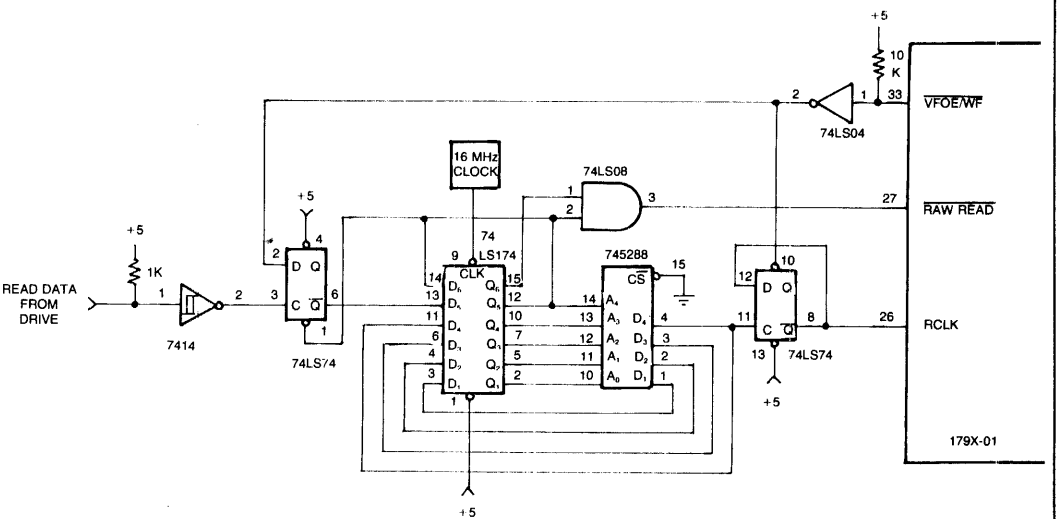


FIGURE 12. 179X DATA SEPARATOR

(PROVIDED COURTESY OF ANDROMEDA SYSTEMS, PANORAMA CITY, CA 91402)

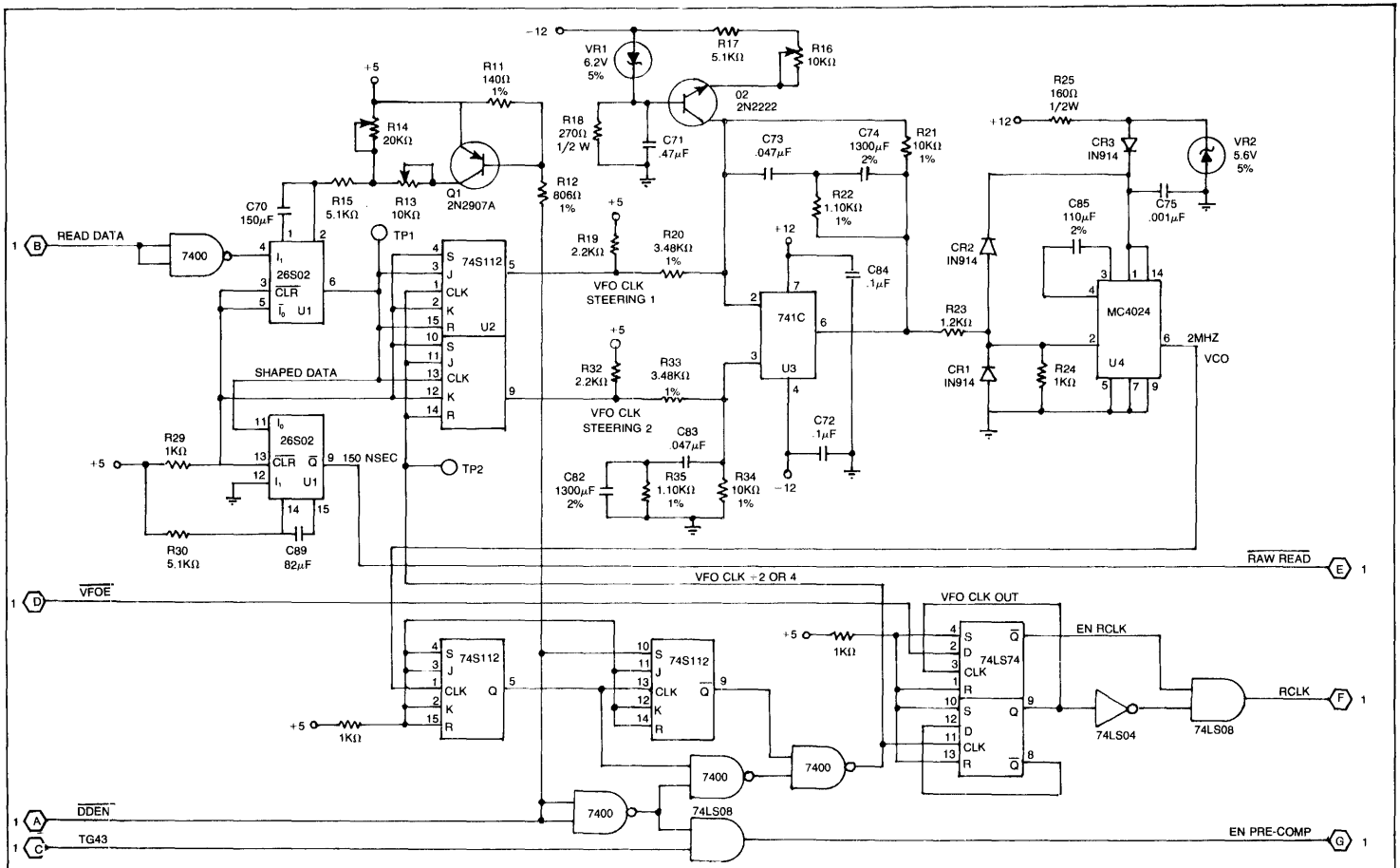


FIGURE 13. PLL DATA RECOVERY CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112)

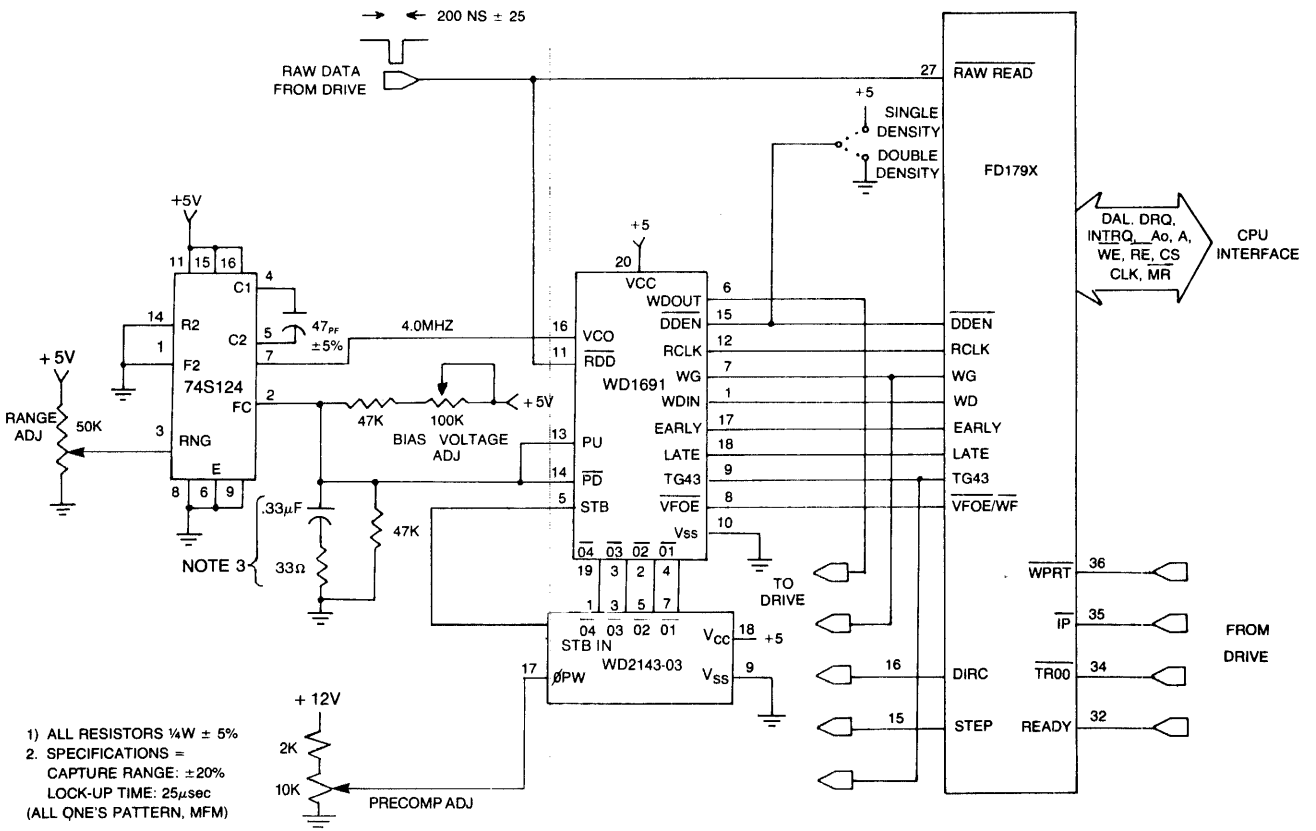


FIGURE 14. 8" SINGLE/DOUBLE DENSITY SYSTEM

Refer to 179X-02 Floppy Disk Formatter/Controller Family Data Sheet for Command, Timing and Status Information.

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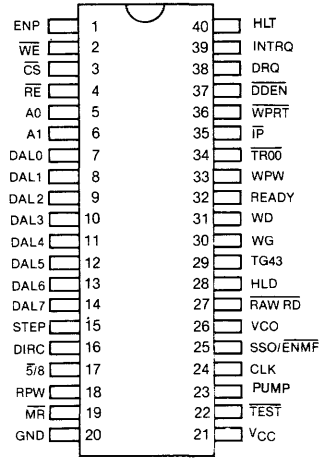
WD279X-02 Floppy Disk Formatter/Controller Family

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY



PIN DESIGNATION

DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2795/7 has a side select output for controlling double sided drives.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on double density Write Data output only.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for minifloppies.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the Command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5¼," 8" SELECT	$\overline{5/8}$	This input selects the internal VCO frequency for use with 5¼" drives or 8" drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.
22	TEST	$\overline{TEST}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2791, 2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal ÷2 of the Master Clock. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2795, 2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the WD279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the WD279X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This input pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

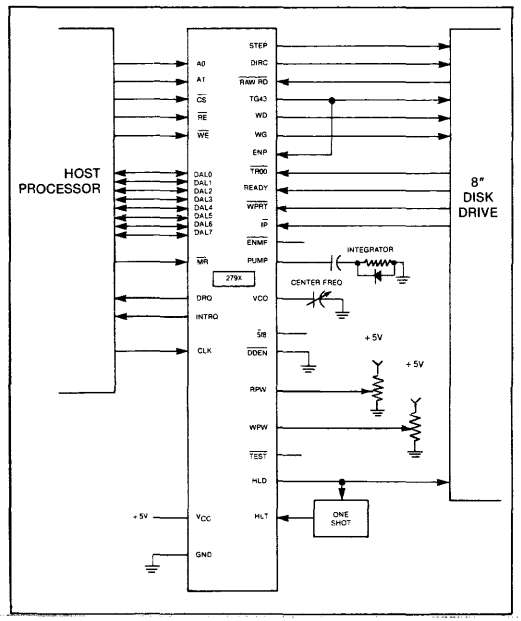


Figure 1.

APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation may be enabled, its value predetermined by an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line package.

FEATURES	2791	2793	2795	2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Out			X	X
Internal CLK Divide	X	X		

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations in Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

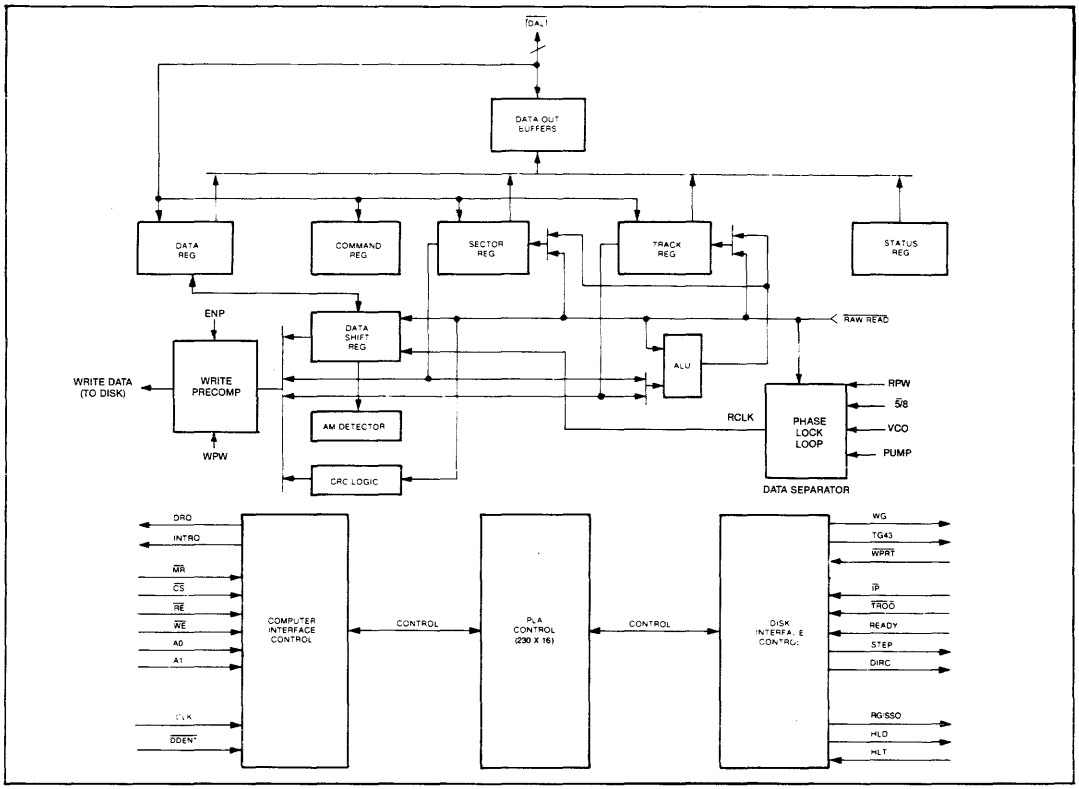
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.



WD279X BLOCK DIAGRAM

Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷ 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8}$ = 0, 5¼" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5/8}$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, TEST, and $\overline{MR}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*2795/97 may vary — see command summary.

The WD279X recognizes tracks and sectors numbered 00-FFX. However, due to programming restrictions, only tracks and sectors 00 thru F4 can be formatted.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{DDEN}$ = 0), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

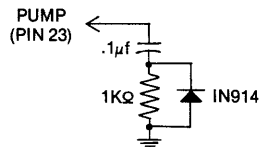
After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22μf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK R1	CLK R0	2 MHz $\overline{TEST}$ = 1	1 MHz $\overline{TEST}$ = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

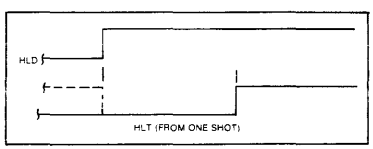
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID

Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When HLT = 1, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.



HEAD LOAD TIMING

When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

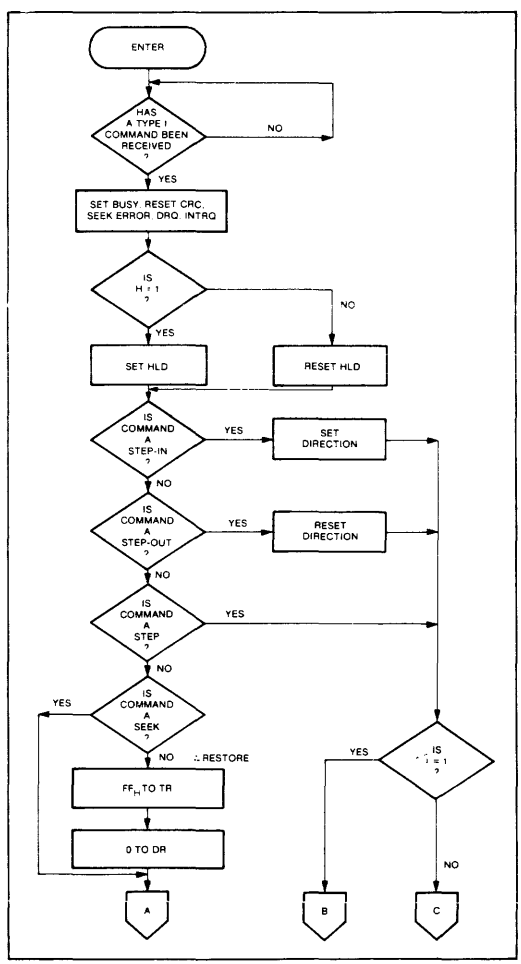
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

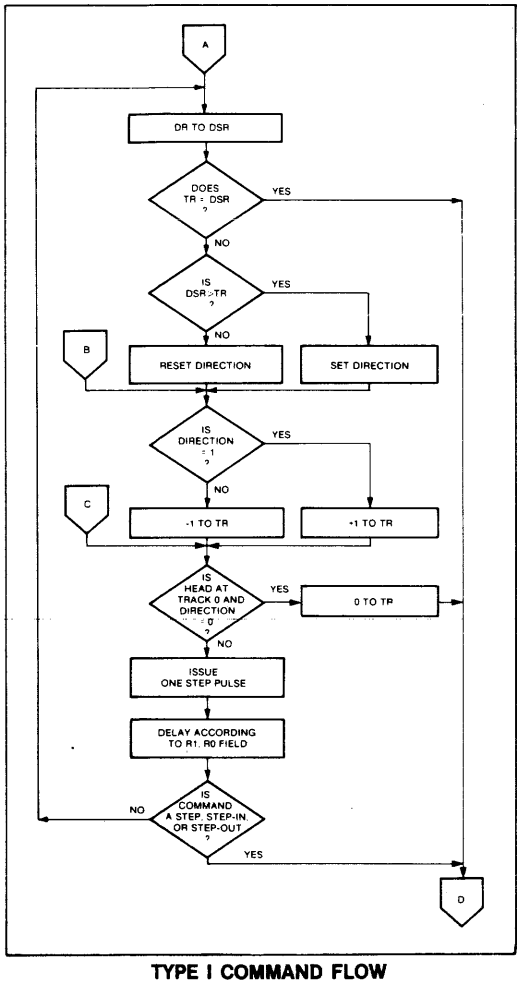
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

SEEK

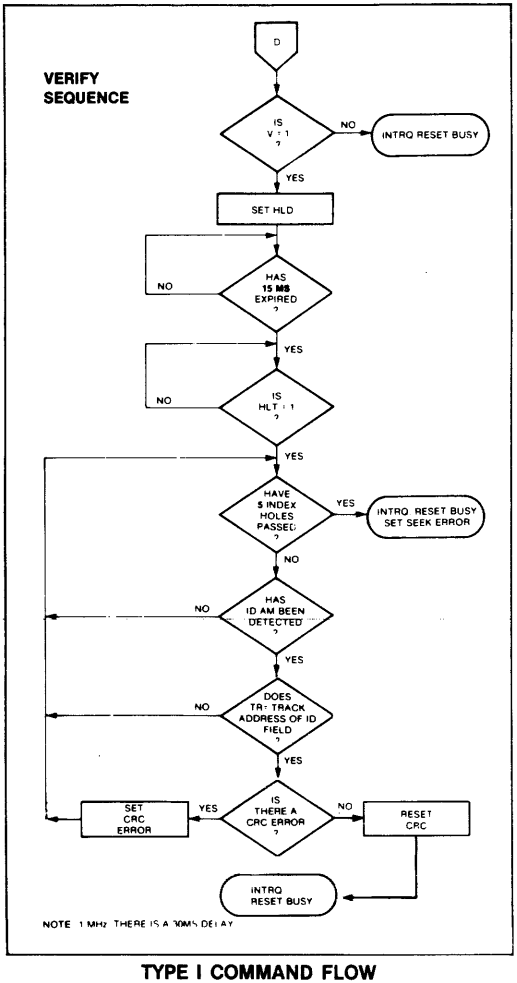
This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

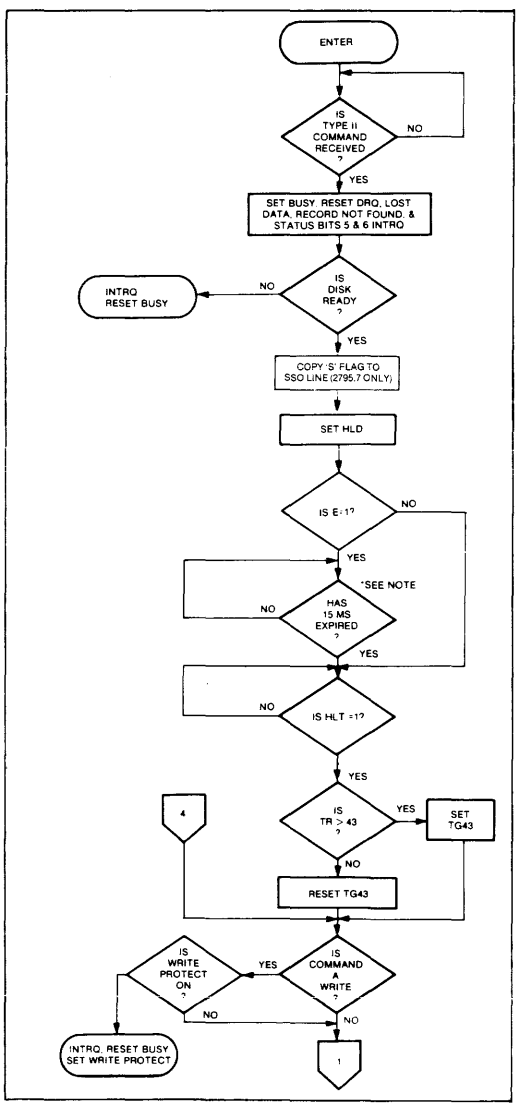
On the 2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

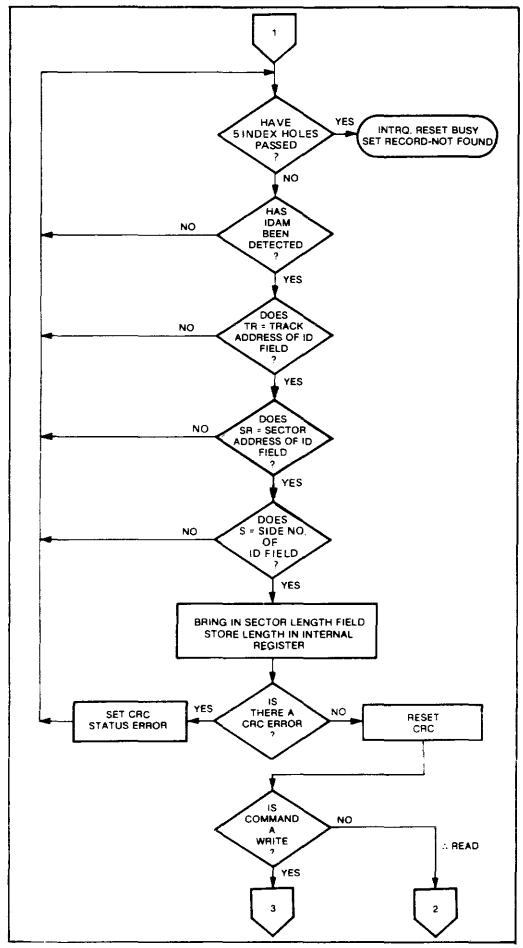
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the 279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from



TYPE II COMMAND

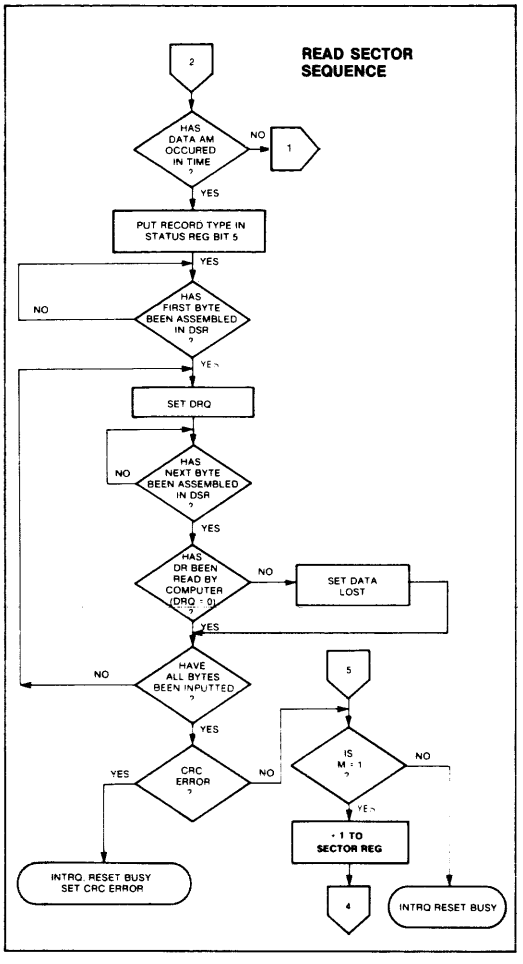


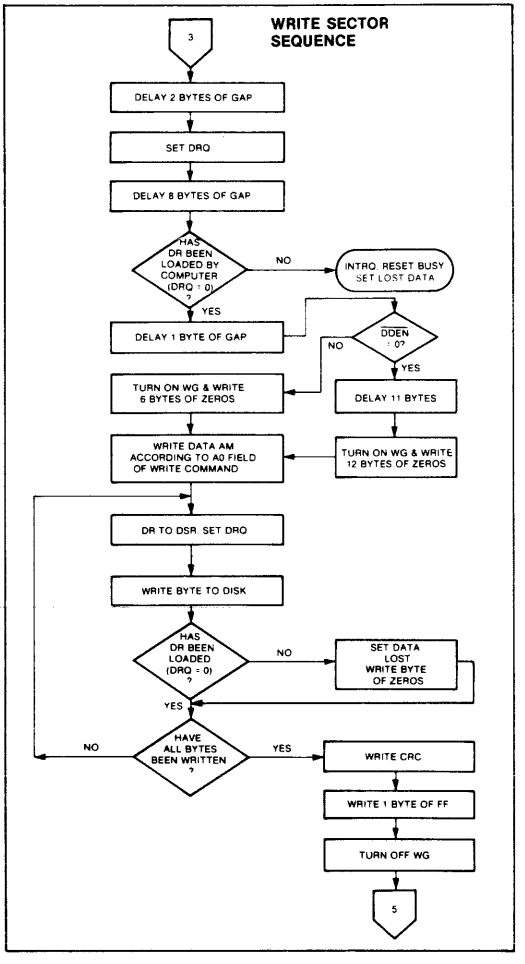
TYPE II COMMAND

depending upon the command. The 279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds





TYPE II COMMAND

the number available. The 279X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 2791-93 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the 279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 2795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2795/7 READ SECTOR and WRITE SECTOR com-

TYPE II COMMAND

mands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one bye of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

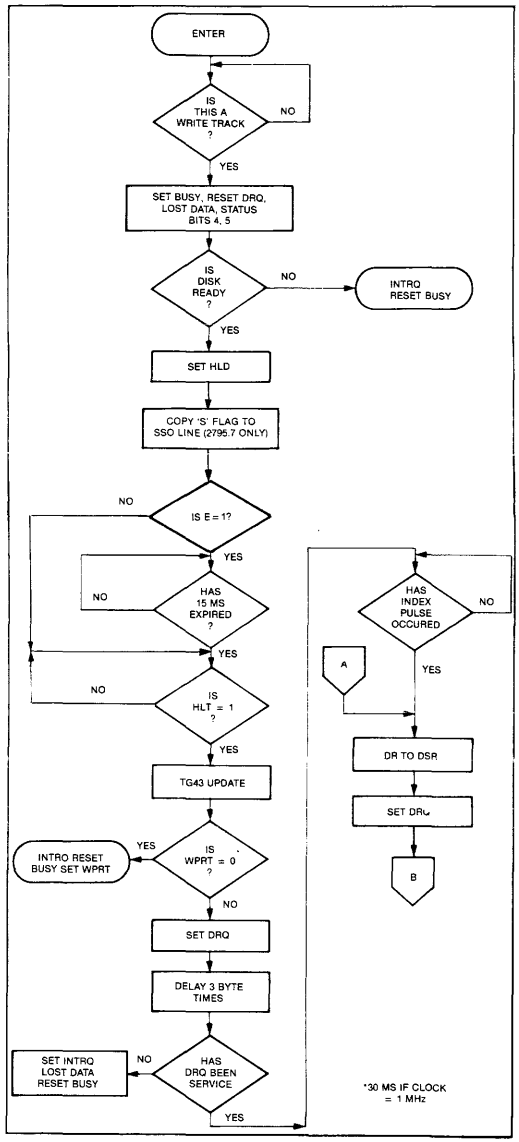
TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

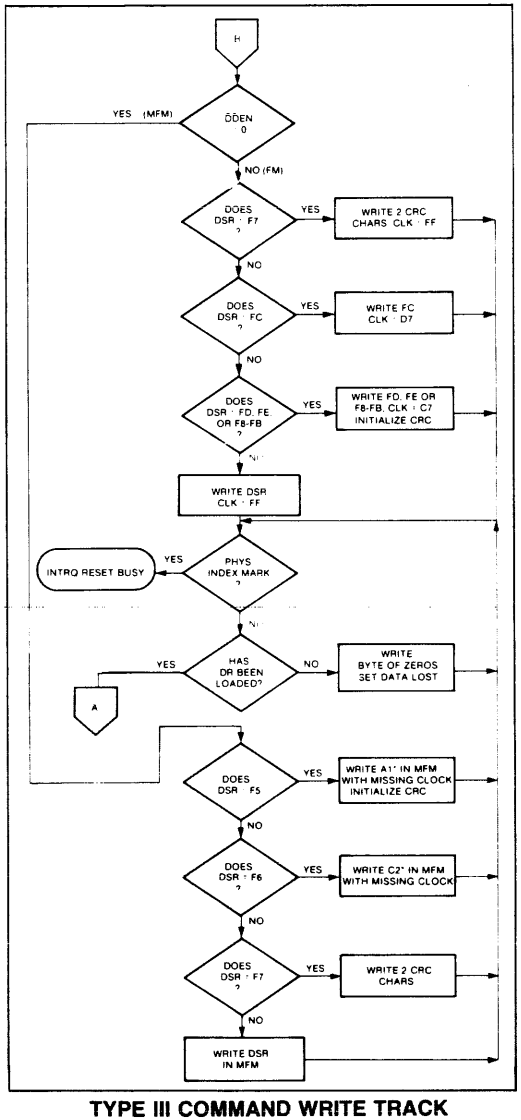
Although the CRC characters are transferred to the computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.



TYPE III COMMAND WRITE TRACK

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The ac-



TYPE III COMMAND WRITE TRACK

cumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	WD279X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	WD279X INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

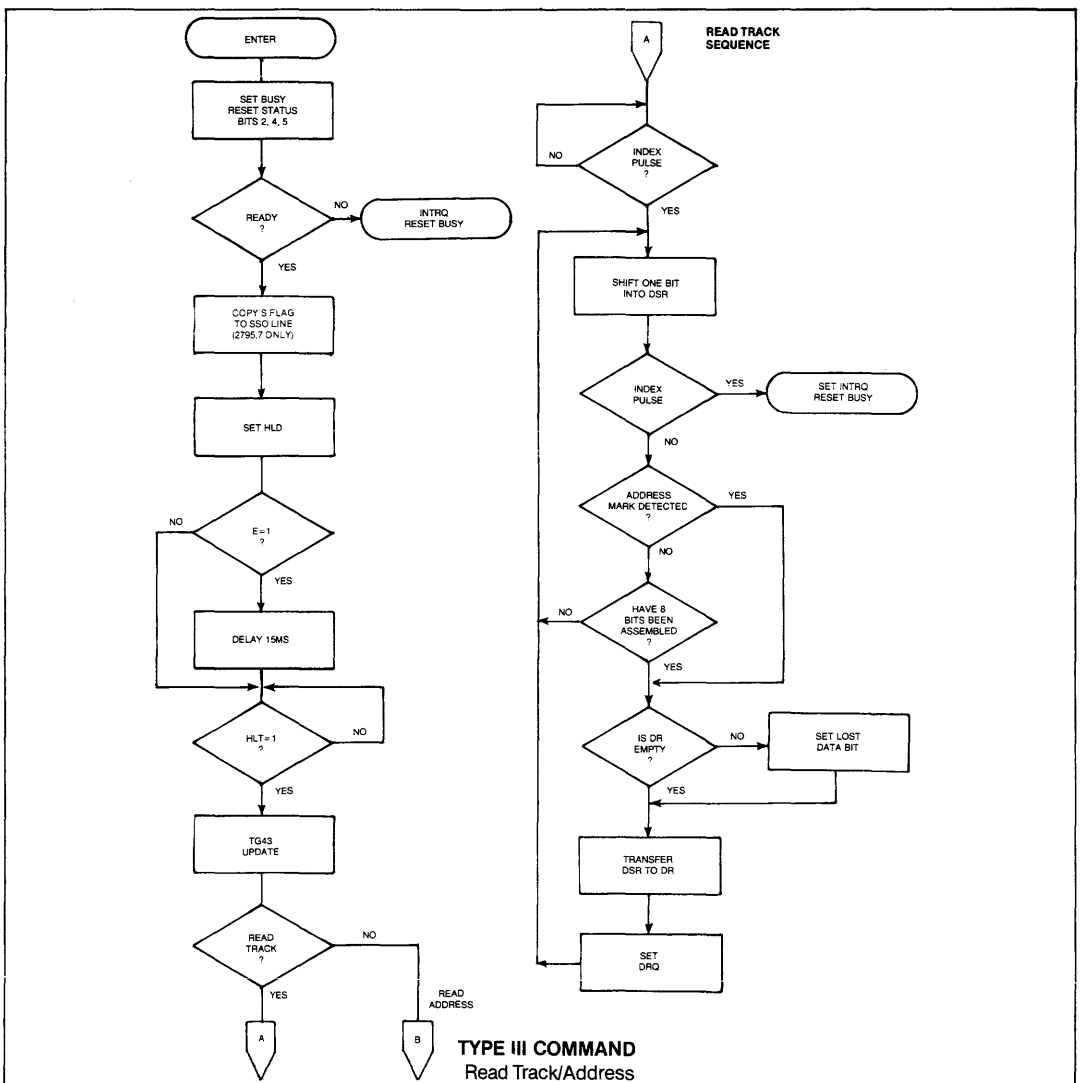
TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate



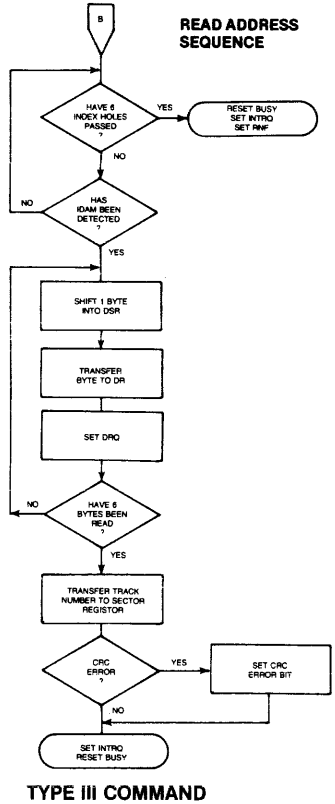
TYPE III COMMAND
Read Track/Address

interrupt condition I_3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
1 26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247[2]	FF (or 00)

1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed.

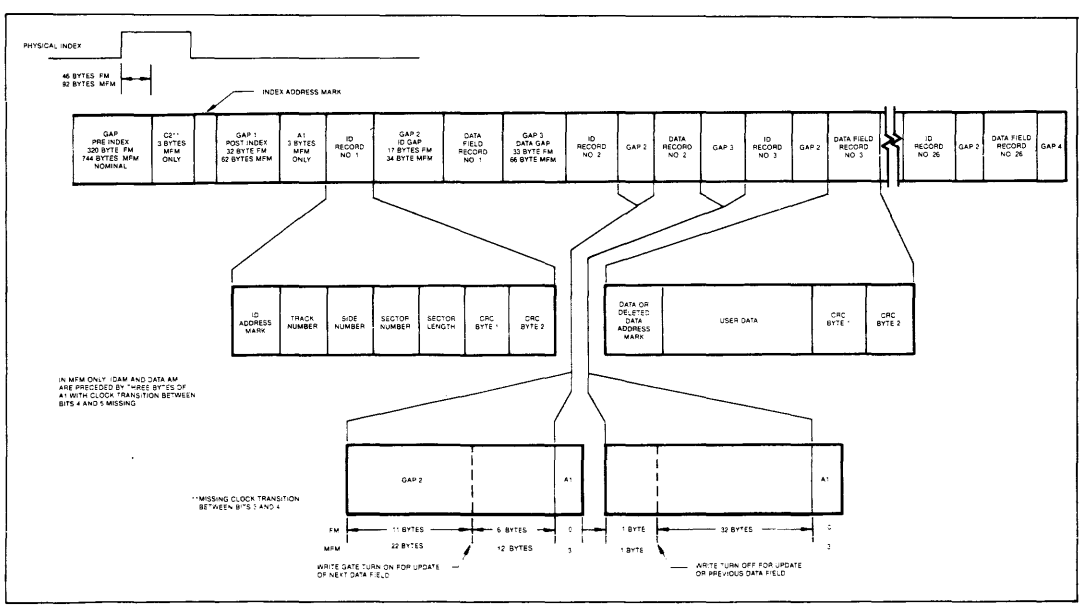
IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order for format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times

** Continue writing until 279X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.
** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with
respect to V_{SS} = +7 to −0.5V
Operating temperature = 0°C to 70°C
Storage temperature = −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			0.45	V	$I_O = 1.6$ mA
V_{OHP}	Output High PUMP	2.2			V	$I_{OP} = -1.0$ mA
V_{OLP}	Output Low PUMP			0.2	V	$I_{OP} = +1.0$ mA
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	μA	V_{IN} = 0V
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on 2791 and 3.

TIMING CHARACTERISTICS

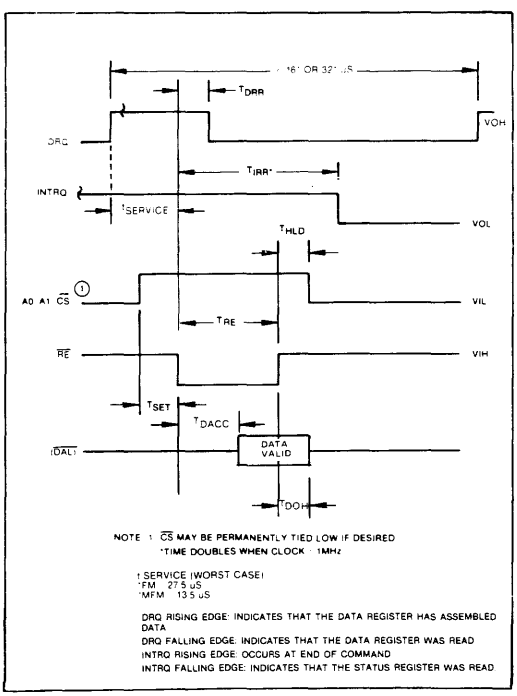
T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	C_L = 50 pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{WE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	

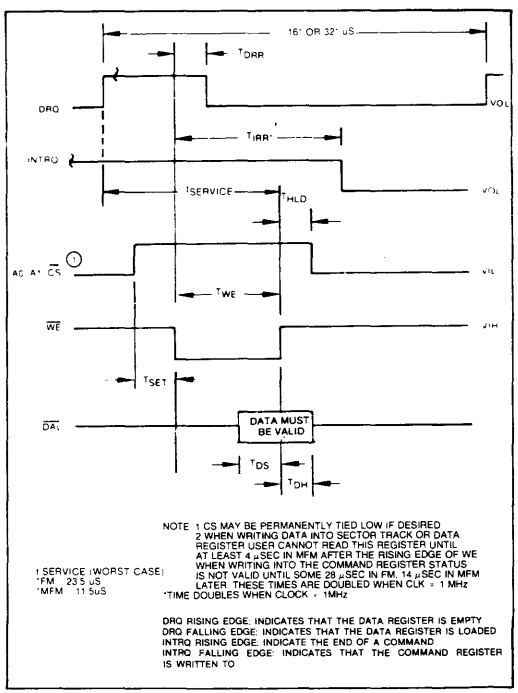


NOTE 1: $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
*TIME DOUBLES WHEN CLOCK = 1MHz

† SERVICE (WORST CASE)
*FM 27.5 uS
*MFM 13.5 uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER HAS ASSEMBLED DATA
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER WAS READ
INTRQ RISING EDGE: OCCURS AT END OF COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE STATUS REGISTER WAS READ

READ ENABLE TIMING



NOTE 1 CS MAY BE PERMANENTLY TIED LOW IF DESIRED
2 WHEN WRITING DATA INTO SECTOR TRACK OR DATA REGISTER USER CANNOT READ THIS REGISTER UNTIL AT LEAST 4 µSEC IN MFM AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 28 µSEC IN FM, 14 µSEC IN MFM LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz
*TIME DOUBLES WHEN CLOCK = 1MHz

† SERVICE (WORST CASE)
*FM 23.5 uS
*MFM 11.5uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER IS EMPTY
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER IS LOADED
INTRQ RISING EDGE: INDICATE THE END OF A COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE COMMAND REGISTER IS WRITTEN TO

WRITE ENABLE TIMING

INPUT DATA TIMING

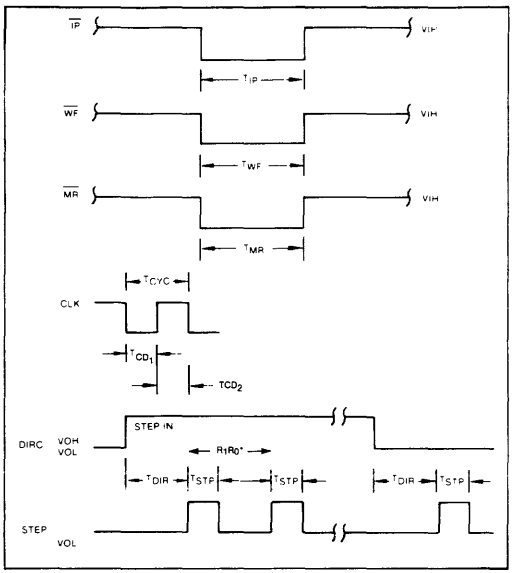
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (NO WRITE PRECOMPENSATION)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		200	250	300	nsec	MFM
T_{WG}	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
T_{WF}	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{CD_1}	Clock Duty (low)	230	250	20000	nsec	
T_{CD_2}	Clock Duty (high)	230	250	20000	nsec	
T_{STP}	Step Pulse Output	2 or 4			µsec	See Note
T_{DIR}	Dir Setup to Step		12		µsec	± CLK ERROR
T_{MR}	Master Reset Pulse Width	50			µsec	
T_{IP}	Index Pulse Width	10			µsec	See Note
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
	Precomp Adjust.	100		300	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 100 nsec
		200	300	400	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 300 nsec
		600	900	1200	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Cext = 0
	Oscillator. Adjustable by ext. capacitor on Pin 26		4.0		MHz	Cext = 35 pf
	Pump Up + 25%	5.0			MHz	PU = 2.2V Cext = 35 pf
VCO	Pump Down − 25%			3.0	MHz	$\overline{PD}$ = 0.2V Cext = 35 pf
VCO	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35 pf
	T_A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Adjustable external capacitor	20	45	100	pf	VCO = 4.0MHz nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	$\overline{DDEN}$ = 0 $\overline{5/8}$ = 1
			250		KHz	$\overline{DDEN}$ = 0 $\overline{5/8}$ = 0
			250		KHz	$\overline{DDEN}$ = 1 $\overline{5/8}$ = 1
			125		KHz	$\overline{DDEN}$ = 1 $\overline{5/8}$ = 0
PU/DON	PU/$\overline{PD}$ time on (pulse width)			250	ns	MFM
				500	ns	FM

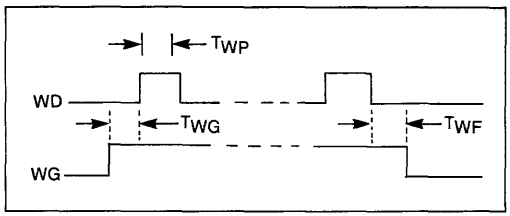


MISCELLANEOUS TIMING

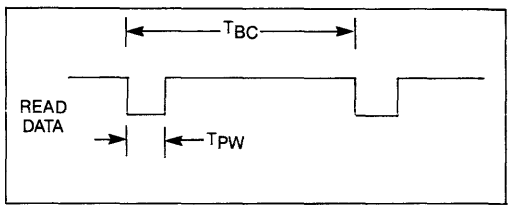
*FROM STEP RATE TABLE

NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.



WRITE DATA TIMING



READ DATA TIMING

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19). Insure that $\overline{5/8}$, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4 Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8" DD, 500ns for 5¼" DD, etc.).
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5¼" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

WD279X-02 Floppy Disk Formatter/Controller Family Application Notes

INTRODUCTION

In an effort to simplify Floppy Diskette interfacing, Western Digital has been constantly improving the LSI Controller/Formatter, the most recent of which is the WD279X Family of LSI controller devices, incorporating advanced technology to include controller, Write Precompensation and Analog Phase Lock Loop in a single 40 pin dual-in-line package. With this package we can now offer the designer the simplest ever interfacing option.

The family consists of four members, WD2791, WD2793, WD2795 and WD2797. WD2791 and WD2793 offer internal clock divide in true and inverted data bus. The WD2795 and WD2797 offer internal side select. The family supports both 5¼" and 8" Diskette Drives and both single and double density.

HOST INTERFACING

The LSI Diskette Controller has been developed to ease the interfacing of Processor to Disk Device. The Host interfacing with WD279X Family is accomplished with minimum external devices via an 8 bit Bidirectional bus, read/write controls, register select lines and optional control line for chip select, 5¼" or 8" select, enable mini floppy, double density enable. The basic operation at the controller is accomplished by selecting the device via (CS) chip select line, enabling selection of one of the five internal registers (Figure 1).

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

Figure 1.

Each time a command is issued to the WD279X, the busy bit is set and INTRQ (Interrupt Request) line is reset. The user has the option of testing for the busy bit or polling INTRQ to determine if command has been completed.

The busy bit will be reset whenever the WD279X is idle and awaiting a new command. The INTRQ line once set, can only be reset by reading of the status register or issuing a new command.

The A_0, A_1 Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6250, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the WD279X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2 MHz (8" drive) or 1 MHz (5¼" drive) with 50% duty cycle. Accuracy should be +1% (crystal source) since all internal timing, including stepping rates, are based upon this clock, or a single 2 MHz CLK on WD2791 and WD2793 since $\overline{ENMF}$ line will internally divide CLK.

The MR or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initalizes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The WD179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TR00}$ line to go active low. This line should be connected to the drive's $\overline{TR00}$ sensor.

The DDEN line causes selection of either single density (DDEN = 1) or double density operation. DDEN should not be switched during a read or write operation.

The 5/8 Line selects interal VCO frequency to be used with 5¼" or 8" drives.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the

drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the WD279X. Inputs to the WD279X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed −0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. sensor that informs the WD279X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open," Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The WD279X will look at the ready signal prior to executing READ/WRITE commands. READY is not inspected during any Type 1 commands. All type 1 commands will execute regardless of the Logic Level on this Line.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the WD279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the WD279X terminated operations, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the WD2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

For write operations, the WD279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the WD279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, and interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Command types are summarized in Table 1 and Table 2.

Table 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

		Bits							
Type	Command	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	I_1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

		Bits							
Type	Command	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Table 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Load head at beginning h = 2, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II & III	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

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WD1691 Floppy Support Logic (F.S.L.)

FEATURES

- DIRECT INTERFACE TO THE FD179X
- ELIMINATES EXTERNAL FDC LOGIC
- DATA SEPARATION/RCLK GENERATION
- WRITE PRECOMPENSATION SIGNALS
- VFOE/WF DEMULTIPLEXING
- PROGRAMMABLE DENSITY
- 8" OR 5.25" DRIVE COMPATIBLE
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- SINGLE +5V SUPPLY

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.

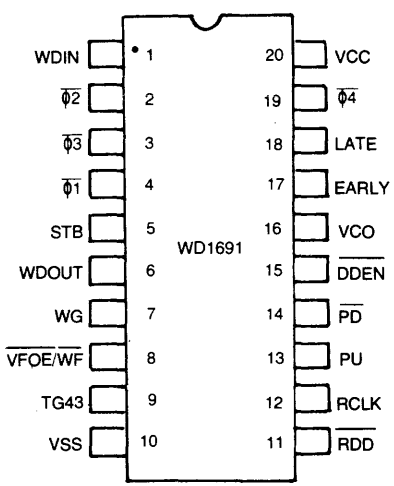


Figure 1 WD1691 PIN DESIGNATION

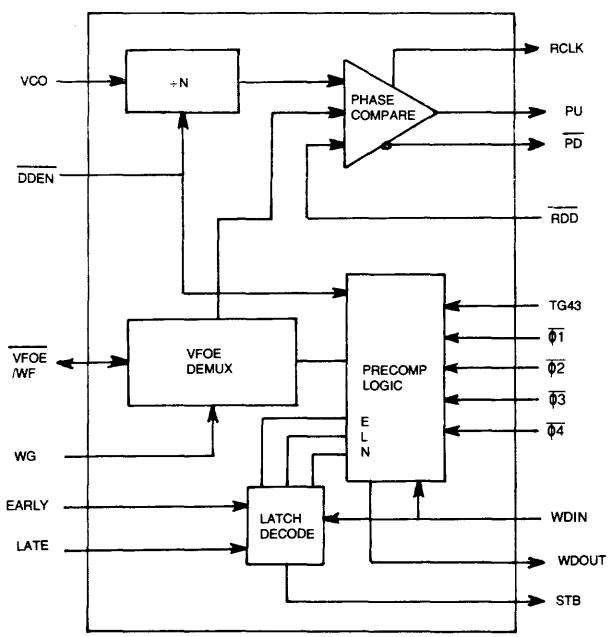


Figure 2 WD1691 BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4, 19	PHASE 2, 3, 1, 4	$\overline{\phi 2}$ $\overline{\phi 3}$ $\overline{\phi 1}$ $\overline{\phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	$\overline{\text{VFOE}}/\overline{\text{WF}}$	Ties directly to the FD179X $\overline{\text{VFOE}}/\overline{\text{WF}}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
10	V_{SS}	V_{SS}	Ground
11	READ DATA	$\overline{\text{RDD}}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{\text{PD}}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{\text{DDEN}}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{CC}	V_{CC}	+ 5V ± 10% power supply

Table 1 PIN DEFINITIONS

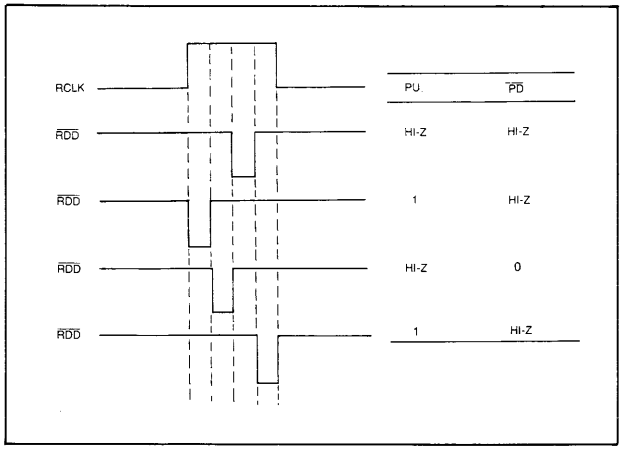


Figure 3 PUMP SIGNAL TIMING DIAGRAM

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

Figure 4 DATA RECOVERY LOGIC

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: $\overline{DDEN}$, VCO, $\overline{RDD}$, and $\overline{VFOE/WF}$; and three outputs: PU, $\overline{PD}$ and RCLK. The $\overline{VFOE/WF}$ input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

The Write Precompensation circuit has been designed to be used with the WD2143-03 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-03 is not needed. In this case, $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, $\overline{\phi 4}$, and STB should be tied together, $\overline{DDEN}$ left open, and TG43, WDIN, Early, and Late tied to ground.

In the double-density mode ($\overline{DDEN}$=0), the signals Early and Late are used to select a phase input ($\overline{\phi 1}$ – $\overline{\phi 4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-03 to start its pulse generation. $\overline{\phi 2}$ is used as the write data pulse on nominal (Early=Late=ϕ), $\overline{\phi 1}$ is used for early, and $\overline{\phi 3}$ is used for late. The leading edge of $\overline{\phi 4}$ resets the STB line in anticipation of the next write data pulse. When TG43=0 or $\overline{DDEN}$=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while $\overline{DDEN}$=0.

The signals, $\overline{DDEN}$, TG43, and $\overline{RDD}$ have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

When $\overline{VFOE/WF}$ and WRITE GATE are low, the data recovery circuit is enabled. When the $\overline{RDD}$ line goes Active Low, the PU or $\overline{PD}$ signals will become active. See Figure 4. If the $\overline{RDD}$ line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an *increase* in VCO frequency. If the $\overline{RDD}$ line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while $\overline{PD}$ will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of $\overline{RDD}$ occurs in the center of the RCLK window, both PU and $\overline{PD}$ will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. See Figure 3. The RCLK signal is a divide-by-16 ($\overline{DDEN}$=1) or a divide-by-8 ($\overline{DDEN}$=0) of the VCO frequency.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will go from a tri-state to .4V minimum. By tying PU and $\overline{PD}$ together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tristate level to approximately 1.4V. This yields a worst case swing of ± 1V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and $\overline{PD}$ signals are affected by the width of the RAW READ ($\overline{RDD}$) pulse. The wider the RAW READ pulse, the longer the PU or $\overline{PD}$ signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns, (VCO = 4MHz, $\overline{DDEN}$ = 0) or 500ns. (VCO = 2MHz, $\overline{DDEN}$ = 1), then both a PU and $\overline{PD}$ will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, an ideal condition for the FD179X internal recovery circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... −25° to 70°C
Voltage on any pin with respect to Ground (vss) ..... −0.2 to +7V
Power Dissipation 1W
Storage Temp.—Ceramic—65°C to +150°C
Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0 to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = OV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.2		+0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			+0.45	V	I_{OL}=3.2MA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH}=−200μa
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

NOTE: For AC and functional testing purposes, a Logic '0' is measured at 0.8V, and a Logic '1' at 2.0V.

AC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5V ± 10%; V_{SS} = OV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	$\overline{DDEN}$=0
		.5	2	6	MHz	$\overline{DDEN}$=1
R_{pw}	$\overline{RDD}$ Pulse Width	100	200		ns.	
W_{el}	EARLY (LATE) to WDIN	100			ns.	
P_{on}	PUMP UP/DN Time	0		250	ns.	
W_{pi}	WDIN to WDOUT			80	ns.	$\overline{DDEN}$=1
I_{nr}	Internal Pull-up Resistor	4.0	6.5	10	KΩ	

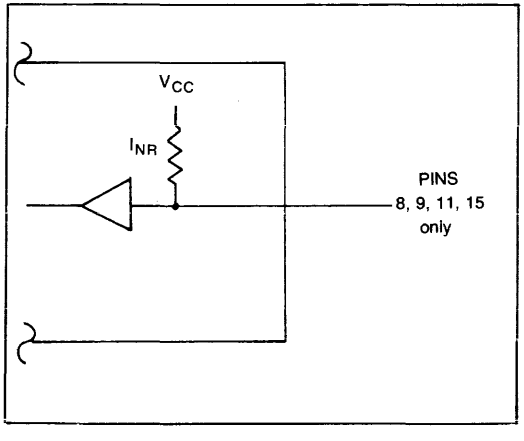


Figure 5 INTERNAL PULL-UP RESISTOR

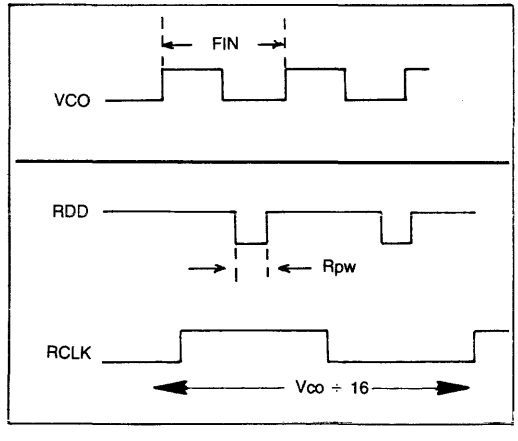


Figure 6 RDD AND RCLK PULSE DIAGRAMS

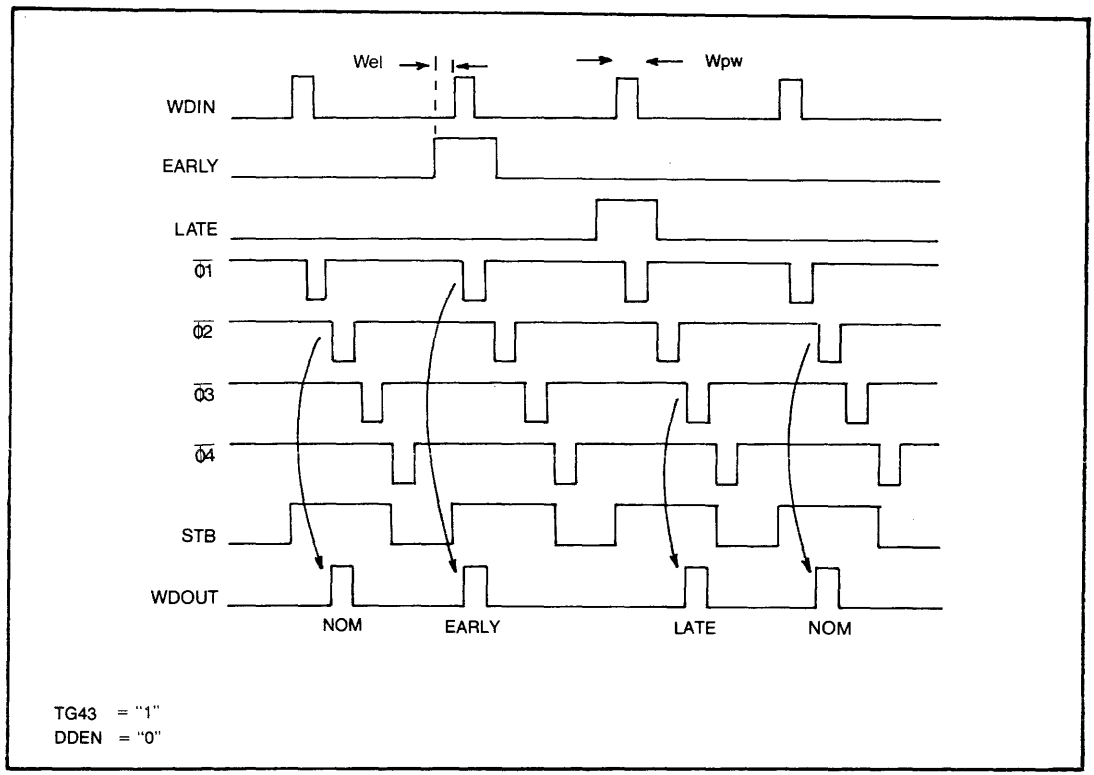


Figure 7 WRITE DATA TIMING (MFM)

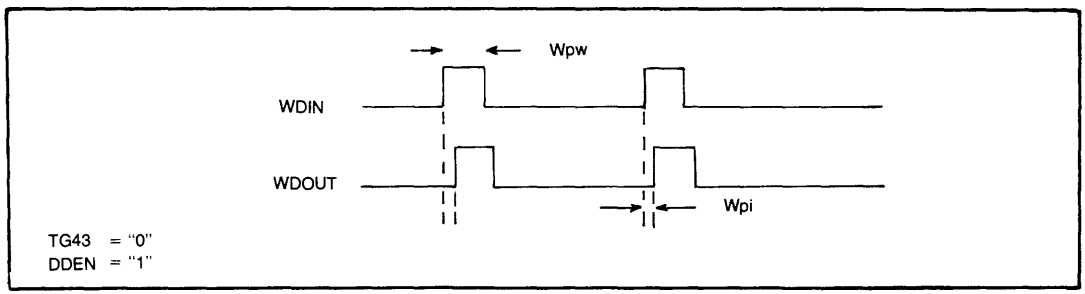


Figure 8 WRITE DATA TIMING (FM)

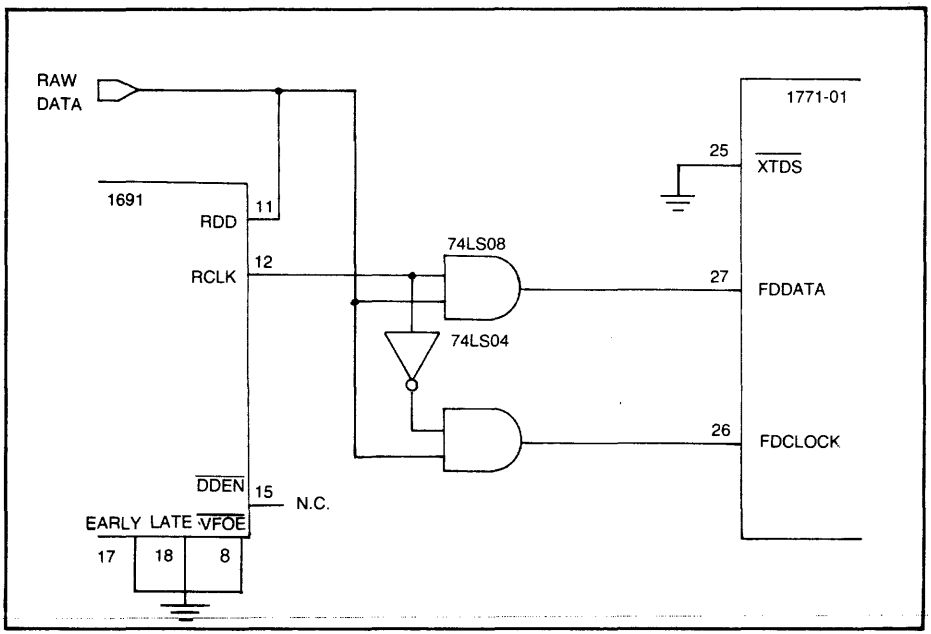


Figure 9 WD1691 to FD1771-01 INTERFACE

TYPICAL APPLICATIONS

Figure 9 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 10 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or $\overline{PD}$ signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-03 is also used, providing write precompensation when in double-density, from tracks 44-77. The $\overline{DDEN}$ line can either be controlled by a toggle switch or a logic level from the host system.

ALIGNMENT

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the $\overline{IP}$ line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically.

The pulse width set on pin 4 ($\overline{\emptyset 1}$) will be the desired precomp delay from nominal.

The data separator must be adjusted with the $\overline{RDD}$ or $\overline{VFOE}$/$\overline{WF}$ line at a Logic I. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.

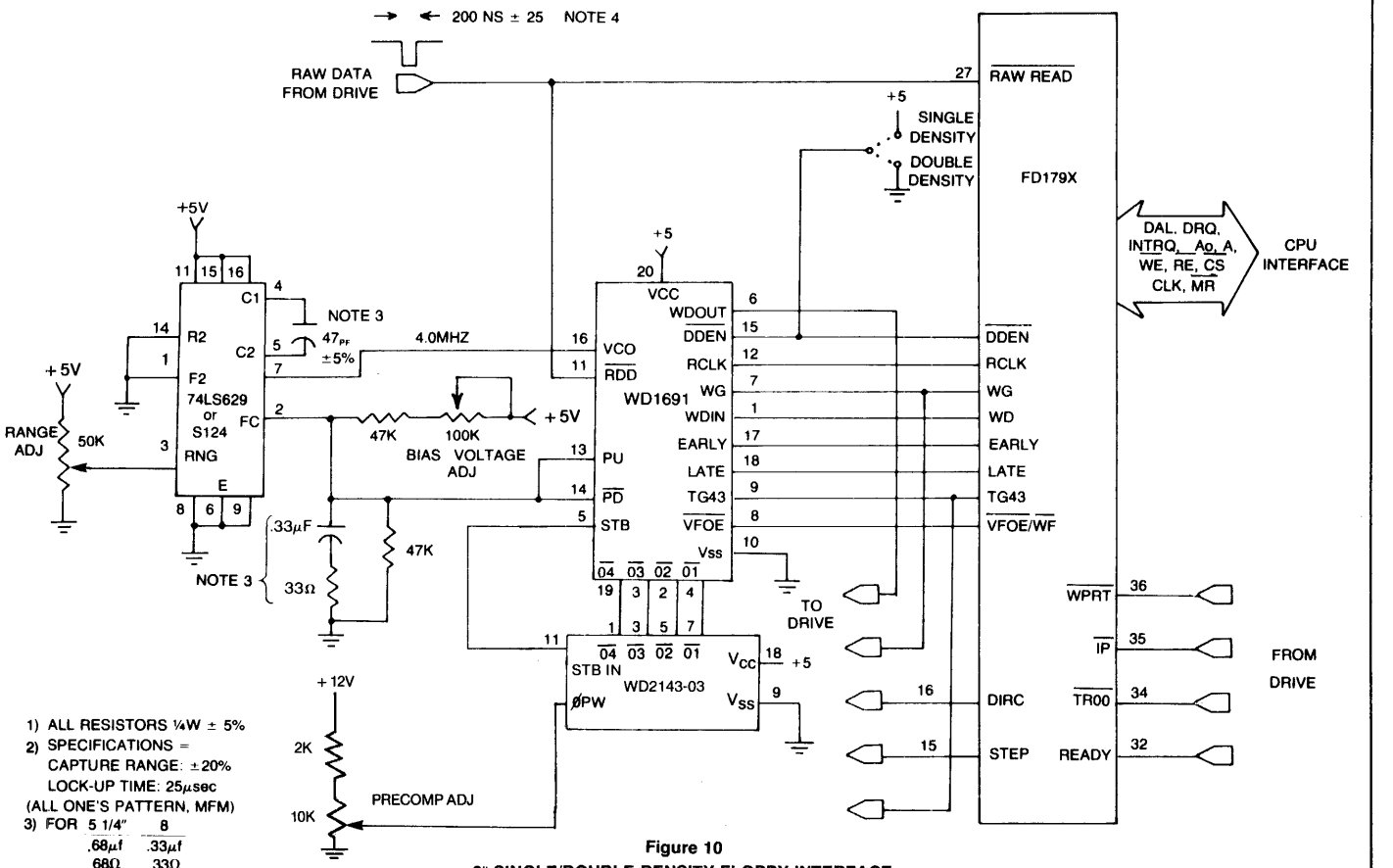
SUBSTITUTING VCO's

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a ± 15% capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about ± 25%, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.

2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is −200ua. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of −200ua.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.



1) ALL RESISTORS ¼W ± 5%
2) SPECIFICATIONS =
   CAPTURE RANGE: ±20%
   LOCK-UP TIME: 25μsec
   (ALL ONE'S PATTERN, MFM)
3) FOR 5 1/4" 8
   .68μf .33μf
   68Ω 33Ω
   82Pf 47Pf
4) $\overline{RDD}$ = ONE EIGHTH RCLK WIDTH MAXIMUM
   250ns for 4MHz
   500ns for 2MHz

Figure 10
8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE

See page 481 for ordering information.

Printed in U.S.A.

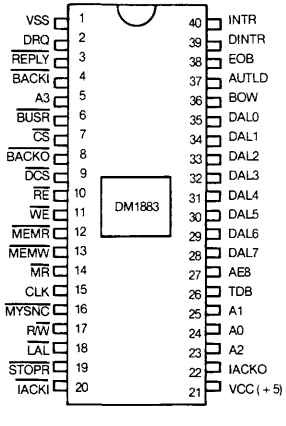
DM1883A/B Direct Memory Access Controller

FEATURES

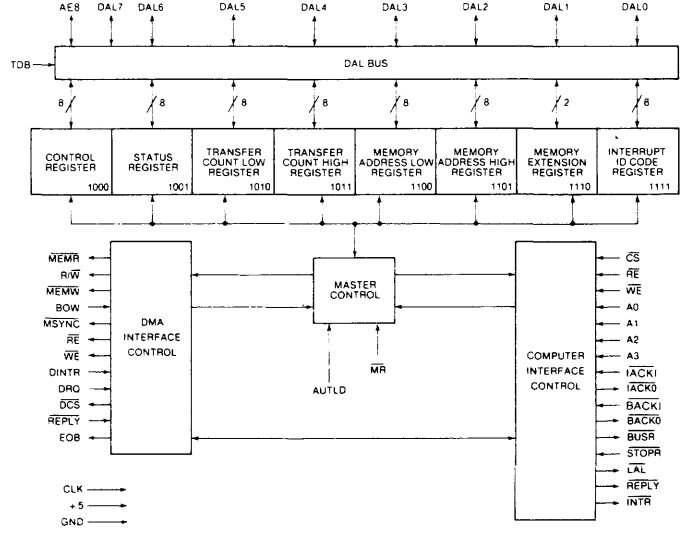
- AUTOMATIC DAISY CHAINING OF BUS AND INTERRUPT ACKNOWLEDGE SIGNALS
- AUTO LOAD OPTION
- SINGLE +5 VDC POWER SUPPLY
- 8 BIT BI-DIRECTIONAL DATA BUS
- TRUE OR COMPLEMENT DATA BUS
- 8 CPU ADDRESSABLE DMAC REGISTERS
- 8 CPU ADDRESSABLE DEVICE REGISTERS
- AUTOMATIC GENERATION OF DEVICE CS DURING DMA AND CPU DEVICE ACCESSES
- 256K MEMORY ADDRESSING
- 64K PROGRAMMABLE PAGE PROTECTION
- BYTE OR WORD DMA TRANSFERS
- INTERRUPT AND BUS REQUEST CAPABILITIES
- END-OF-BLOCK SHUT OFF BY DMAC
- TIME-OUT INTERRUPT CAPABILITY
- SINGLE CLOCK INPUT
- CS, RE, WE, A0-A3 ADDRESSING
- STOP REQUEST INPUT TO DELAY INTERRUPT OR BUS REQUESTS
- COMPATIBLE WITH OUR FLOPPY DISC CONTROLLERS
- 8 BIT PROGRAMMABLE INTERRUPT ID CODE

GENERAL DESCRIPTION

The DM1883 Direct Memory Access Controller (DMAC) is packaged in a 40 pin standard dual in-line package. The chip requires a single +5 power supply input and a single clock input. The device contains 8 CPU addressable registers, and allows for up to 8 CPU addressable device registers if the automatic device chip select feature is used. Byte or word transfers can be programmed, and all memory DMA operations are handshaked for compatibility with a variety of bus structures. Up to 256K bytes of memory can be accessed directly with 64K page protection and nonexistent memory interrupt as options. Bus and Interrupt Acknowledge signals are internally daisy chained, and a STOP REQUEST input prevents new requests while a current request is active. Device accesses are not handshaked, and a BUS HOLD feature is present for high speed devices. Device interrupt input, end-of-block output, and I/O read/write output pins simplify hardware interfacing to the device and the CPU bus. The AUTO LOAD feature allows automatic boot-loading of up to 64K bytes or words into memory starting at location zero. An 8 bit interrupt ID code is also provided.



PIN CONNECTIONS



DM1883 BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
1	GROUND	VSS	Ground
2	DATA REQUEST	DRQ	Data service request input from the peripheral device. A DMA transfer is initiated when this signal goes high.
3	$\overline{\text{REPLY}}$	$\overline{\text{REPLY}}$	Active low bi-directional handshake signal for both CPU and DMA transfers.
4	$\overline{\text{BACK IN}}$	$\overline{\text{BACKI}}$	Bus acknowledge in. An active low input signal from the CPU or a previous device in the $\overline{\text{BACK}}$ daisy chain. When low this signal will initiate a DMA transfer if the DMAC was requesting a DMA cycle.
5, 23, 24, 25	REGISTER SELECTS	A0-A3	These inputs select one of eight DMAC registers or one of eight device registers. When A3 is high the DMAC is selected. When A3 is low the DMAC is deselected and $\overline{\text{DCS}}$ is made low by the DMAC to activate device transfers. $\overline{\text{CS}}$ input to the DMAC must be made low before either the DMAC or the device may be selected by the CPU.
6	$\overline{\text{BUS REQUEST}}$	$\overline{\text{BUSR}}$	Active low output signal to initiate a CPU bus request and to latch A8-A15, A17 of the 18 bit DMA transfer address from DAL0-DAL7, AE8 into an external register.
7	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	Active low chip select input signal for CPU controlled operations.
8	$\overline{\text{BACK OUT}}$	$\overline{\text{BACKO}}$	Bus acknowledge out. An active low output signal used to pass $\overline{\text{BACKI}}$ along the daisy chain when the DMAC is not requesting a DMA cycle. This output is not affected by $\overline{\text{STOPR}}$.
9	$\overline{\text{DEVICE SELECT}}$	$\overline{\text{DCS}}$	Active low device chip select output signal for CPU and DMAC controlled operations.
10	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	Active low bi-directional read enable for the DMAC and the device.
11	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	Active low bi-directional write enable for the DMAC and the device. $\overline{\text{RE}}$ and $\overline{\text{WE}}$ are inputs during CPU controlled operations, and outputs to the device during DMAC controlled operations.
12	$\overline{\text{MEMORY READ}}$	$\overline{\text{MEMR}}$	Active low output to initiate a memory read during DMA transfers to the peripheral device.
13	$\overline{\text{MEMORY WRITE}}$	$\overline{\text{MEMW}}$	Active low output to initiate a memory write during DMA transfers from the peripheral device.
14	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	Active low master reset signal to initialize the DMAC.
15	CLOCK	CLK	Clock input
16	$\overline{\text{MEMORY SYNC}}$	$\overline{\text{MSYNC}}$	Active low memory sync output to initiate a memory access during DMA transfers.
17	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	This output indicates the direction of transfer for the peripheral device. High for device-to-memory transfers (READ), and low for memory to device transfers (WRITE). Tied directly to Control Register bit 4.
18	$\overline{\text{LOAD ADDRESS LOW}}$	$\overline{\text{LAL}}$	Active low output signal to latch A0-A7, A16 of the 18-bit DMA transfer address from DAL0-DAL7, AE8 into an external register. $\overline{\text{BUSR}}$ and $\overline{\text{LAL}}$ are compatible with INTEL 8212 devices.

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
19	$\overline{\text{STOP REQUEST}}$	$\overline{\text{STOPR}}$	Active low input that prevents $\overline{\text{INTR}}$ and $\overline{\text{BUSR}}$ from going low even if a request becomes active. An active $\overline{\text{INTR}}$ or $\overline{\text{BUSR}}$ request will not be affected by this input going low. This signal is used to speed up daisy chaining of bus and interrupt acknowledge inputs, and to prevent new requests while some other request is in the process of being serviced.
20	$\overline{\text{IACK IN}}$	$\overline{\text{IACKI}}$	Interrupt acknowledge in. An active low input signal from the CPU or a previous device in the $\overline{\text{IACK}}$ daisy chain. The DMAC is selected when $\overline{\text{INTR}}$ is low and this signal goes low. If $\overline{\text{RE}}$ also goes low while the DMAC is selected via this signal then the interrupt ID code is gated onto DAL0-DAL7.
21	POWER SUPPLY	V_{CC}	+5 VDC power supply input
22	$\overline{\text{IACK OUT}}$	$\overline{\text{IACKO}}$	Interrupt acknowledge out. An active low output signal used to pass $\overline{\text{IACKI}}$ along the daisy chain when the DMAC is not requesting an interrupt. This output is not affected by $\overline{\text{STOPR}}$.
26	TRUE DATA BUS	TDB	This input selects a true data bus on the DAL lines when high or open, and a complemented data bus on the DAL lines when low.
27	ADDRESS EXTENSION	AE8	Address extension bit output. Used during DMA operations to extend the address to 18 bits. This bit is true if TDB is high and complemented if TDB is low.
28-35	DATA ACCESS LINES	DAL0-DAL7	An 8-bit bi-directional three-state bus for CPU and DMAC controlled transfers to and from the DMAC. These signals remain in a three-state mode if the peripheral device is selected via A3 instead of the DMAC.
36	BYTE OR WORD	BOW	Byte or word DMA transfer mode input. When high memory addresses are incremented by one after every DMA transfer. When low memory addresses are incremented by two after every DMA transfer and the LSB of the memory address is forced to zero.
37	AUTO LOAD	AUTLD	Active high input to initiate a non-programmed 64K device to memory data transfer.
38	END OF BLOCK	EOB	Active high output to shut off the peripheral device when the transfer count goes to zero.
39	DEVICE INTERRUPT	DINTR	Interrupt service request input from the peripheral device. An interrupt request is generated by the DMAC if this input is high and the device interrupt enable bit in the command register is also set.
40	$\overline{\text{INTERRUPT REQUEST}}$	$\overline{\text{INTR}}$	Active low interrupt service request output. This output goes low if: 1) Any one of the three interrupt conditions is active, and 2) The $\overline{\text{STOPR}}$ input is high, and 3) The corresponding interrupt enable bit for the interrupting condition is set.

NOTE: The following pins float when not active low and require an external pull-up resistor of 10 KΩ (or greater) to +5 VDC:

$\overline{\text{INTR}}$, $\overline{\text{REPLY}}$, $\overline{\text{RE}}$, $\overline{\text{WE}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MSYNC}}$

The following pins have internal 10 KΩ pull-up resistors to +5 VDC:

TBD, DRQ, DINTR

WIRE-ORABLE SIGNALS

The following output signals can be wired together with a single common pull-up resistor if multiple DMAC chips exist on the same board:

$\overline{MSYNC}$, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{INTR}$

REGISTER SELECTION

A 4-bit address input (A0, A1, A2, A3) is used to select one of 8 internal DMAC registers or to generate a device chip select ($\overline{DCS}$) output signal for selection of up to 8 peripheral device registers. The following table details the selection process.

INPUTS					OUTPUT	SELECTED REGISTER
$\overline{CS}$	A3	A2	A1	A0	$\overline{DCS}$	
L	L	X	X	X	L	One of 8 peripheral device registers
L	H	L	L	L	H	DMAC control register (0)
L	H	L	L	H	H	DMAC status register (1)
L	H	L	H	L	H	DMAC TC low register (2)
L	H	L	H	H	H	DMAC TC high register (3)
L	H	H	L	L	H	DMAC MA low register (4)
L	H	H	L	H	H	DMAC MA high register (5)
L	H	H	H	L	H	DMAC MA ext. register (6)
L	H	H	H	H	H	DMAC ID code register (7)

NOTE: L = Low voltage level, H = High voltage level, X = don't care.

TRANSFER COUNT REGISTER (TCR)

A 16-bit counter register that holds the two's complement of the transfer count (words or bytes) for DMA transfer operations. The low order 8 bits are in TC low, and the high order 8 bits are in TC high. The count is incremented by one after every DMA transfer. When the count reaches zero bit 3 of the Status Register is set to a one. If bit 3 in the Command Register is also a one then $\overline{INTR}$ will go low (providing $\overline{STOPR}$ is also high). TCR is set to a one on a MASTER RESET to allow a 64K transfer count during auto load.

MEMORY ADDRESS REGISTER (MAR)

An 18-bit counter register that occupies 3 DMA registers. Bits 0-7 are in MA low, bits 8-15 are in MA high, and bits 16-17 are in MA ext. The carry from bit 15 to 16 is enabled if and only if bit 6 of the Command Register is set to a one. If the BOW input pin is high then the MAR is incremented by one after every DMA transfer. If the BOW input pin is low then the MAR is incremented by two after every transfer and bit 0 is forced to a zero. This register is cleared to all zeros on a MASTER RESET.

During a DMA operation the DMA address is gated onto the DAL lines in two 9-bit bytes. The first byte out contains MAR 8-15 on DAL 0-7 and MAR 17 or AE8. The second byte out contains MAR 0-7 on DAL 0-7 and MAR 16 on AE8. The first byte is valid on the trailing edge of $\overline{BUSR}$, and the second byte is valid on the trailing edge of $\overline{LAL}$. Note that the address can easily be extended to 24 bits by decoding the address of the 2-bit extension register externally and gating the 6 unused bits into an external latch. This would give the system 16 Mbytes of addressing with either 65K or 256K bytes of paging.

REGISTER DEFINITIONS

DMAC CONTROL REGISTER (CR)

7	6	5	4	3	2	1	0
N/A	AECE	HBUS	IOM	TCIE	TOIE	DIE	RUN

BIT	SYMBOL	FUNCTION
0	RUN	Run/stop bit. A 1 places the DMAC in the run mode. A 0 terminates DMAC operation.
1	DIE	Device interrupt enable. A 1 allows a high input on DINTR to set the $\overline{INTR}$ output low.
2	TOIE	Time-out interrupt enable. A 1 allows the time-out one-shot to set the $\overline{INTR}$ output low. The time-out interrupt is set during a DMA transfer if $\overline{REPLY}$ does not go low within 5 usec of $\overline{MSYNC}$ going low.
3	TCIE	Transfer count zero interrupt enable. A 1 allows a zero in the transfer count register to set the $\overline{INTR}$ output low.
4	IOM	Input or output mode. A 1 sets READ mode (from the peripheral device to memory), and a 0 sets WRITE mode (from memory to the peripheral device). This bit also appears as an ungated output on the R/$\overline{W}$ pin.
5	HBUS	Hold bus. A 1 informs the DMAC to hold onto the bus for the entire block instead of releasing the bus after each byte or word transfer.

BIT	SYMBOL	FUNCTION
6	AECE	Address extension carry enable. A 1 allows a carry from DMA address bit 15 to propogate into bit 16.
7	N/A	Not used.

NOTE: Bits 1, 2, 3 set $\overline{\text{INTR}}$ low on an active condition if and only if the $\overline{\text{STOPR}}$ input is high.

DMAC STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
BUSY	AECE	HBUS	IOM	TCZI	TOI	DINT	BOW

BIT	SYMBOL	FUNCTION
0	BOW	Byte or word data channel. A read only bit that indicates the status of the BOW input pin. A 1 bit indicates byte mode, and the DMA memory address is incremented by one after each DMA transfer. A 0 bit indicates word mode, and the DMA memory address is incremented by two (bit 0 is forced to a 0) after every DMA transfer.
1	DINT	If set a device interrupt has occurred. This is a read/write bit. Resetting this bit to a zero will reset $\overline{\text{INTR}}$.
2	TOI	If set a time-out interrupt has occurred. This is a read/write bit. Resetting this bit to a zero will reset $\overline{\text{INTR}}$.
3	TCZI	If set a transfer count equals zero interrupt has occurred. A read only bit. Sets EOB output when set.
4	IOM	Input-output mode. This bit reflects the status of bit 4 in the Command Register. A read only bit.
5	HBUS	Hold bus. This bit reflects the status of bit 5 in the Command Register. A read only bit.
6	AECE	Address extension carry enable. This bit reflects the status of bit 6 in the Command Register. A read only bit.
7	BUSY	Busy (data transfer not completed). A read only bit that reflects the status of bit 0 (RUN) in the Command Register.

NOTE: Bits 1, 2, 3 are set if the corresponding condition occurs. The enable bits in the CR affect only the $\overline{\text{INTR}}$ output, and not the Status Register.

ID CODE REGISTER (IDR)

An 8-bit programmable interrupt ID code register that gives the system an efficient way to establish a jump or vector address during a DMAC interrupt. The register is cleared to all zeros during a MASTER RESET, and must be loaded by the program during system initialization. If $\overline{\text{INTR}}$ is low, and $\overline{\text{IACKI}}$ and $\overline{\text{RE}}$ go low then the contents of this register are gated onto DAL 0-7. IACKI and $\overline{\text{CS}}$ must not be allowed to be low at the same time.

MASTER RESET

All register bits are reset to a zero during a MASTER RESET except the following which are set to ones: TCR bit 0, CR4, CR5, CR6, SR4, SR5, and SR6. This sets up the DMAC for a 64K transfer from the peripheral device to memory starting at address 0. The hold bus mode is also enabled. Execution of an Auto Load will begin DMA transfers under the above conditions.

AUTO LOAD

If the AUTLD input is made active after a MASTER RESET then bits CR3, CR1, and CR0 are also set. This places the DMAC in run mode, and enables two of the interrupt conditions. The DMAC will initiate data transfers, and will continue until either the transfer count reaches zero or a device interrupt occurs. Either event will terminate transfers and generate an interrupt.

WRITE PROTECT FEATURE

During CPU controlled transfers to the DMAC, if the RUN bit is set then any attempt to write into any of the Memory Address or Transfer Count registers will result in a NOP. $\overline{\text{REPLY}}$ will be made low in any case.

CPU CONTROLLED DATA TRANSFERS

During a CPU controlled transfer the CPU must have control of the system bus. When a CPU cycle is

initiated the system decodes the address on the bus. If the DMAC or its associated peripheral device is selected then $\overline{CS}$ to the DMAC is made low. The DMAC looks at the A3 input. If A3 is low the peripheral device is selected, and $\overline{DCS}$ is made low. The DMAC will not respond to an active $\overline{RE}$ or $\overline{WE}$ if A3 is low, and the DAL bus will stay in a high impedance state. This allows the DMAC DAL bus and the device DAL bus to be tied together if the device DAL bus is also in a high impedence state when the device is not selected.

If A3 is high when $\overline{CS}$ is low then the DMAC is selected and will respond to an active low $\overline{RE}$ or $\overline{WE}$. A0-A2 selects the DMAC as described under the REGISTER SELECTION section. If $\overline{RE}$ goes low the DMAC places the contents of the selected register on the DAL bus and activates $\overline{REPLY}$ to inform the CPU that valid data is on the bus. If $\overline{WE}$ goes low the DMAC gates the contents of the DAL bus into the selected register and activates $\overline{REPLY}$ to inform the CPU that data has been accepted.

If the peripheral device has more than 8 registers, or the device has fewer than 8 registers and there are one or more auxiliary registers external to the device, then it may be easier for the user to separate DMAC and device chip selects. In this mode $\overline{CS}$ to the DMAC is activated if and only if the DMAC is selected and A3 is tied to +5 VDC. The chip select to the device from a CPU controlled data transfer is ORed with $\overline{DCS}$ out of the DMAC. In this mode $\overline{DCS}$ will go low if and only if a DMA transfer is in effect and can be used by the controller as a "DMA ACTIVE" signal. Note that in any case actual data transfers to and from the CPU and the peripheral device are done by way of the device's DAL bus, not the DMAC's DAL bus.

DMAC CONTROLLED DATA TRANSFERS

When the DMAC is in RUN mode (CR0=1) it waits for a Data Request (DRQ) input from the peripheral device. When DRQ becomes active the DMAC requests the bus from the CPU by activating $\overline{BUSR}$. If $\overline{STOPR}$ was active when DRQ went active then the DMAC would wait until $\overline{STOPR}$ went high before activating $\overline{BUSR}$. When $\overline{BACKI}$ goes low in response to an active $\overline{BUSR}$ the request has been granted and the DMAC controls data transfers between the peripheral device and memory. The direction of the transfer is determined by the status of the READ/$\overline{WRITE}$ (R/$\overline{W}$) output pin. Note that R/$\overline{W}$ is tied directly to CR4.

1.) DEVICE-TO-MEMORY DMA TRANSFERS (CR4=1)

Once the DMAC has been granted the bus the following occurs:

A.) The DMAC places the high byte of the memory address on the DAL lines, activates $\overline{DCS}$, and then raises $\overline{BUSR}$. The trailing edge of $\overline{BUSR}$ can be used to latch the address into an external buffer.

B.) The DMAC places the low byte of the memory address on the DAL lines while activating $\overline{LAL}$, and then activates $\overline{MSYNC}$. The trailing edge of $\overline{LAL}$ can be used to latch the address into an external buffer

C.) The DAL lines are placed into a high impedence state in anticipation of a data transfer across the bus.

D.) The DMAC activates $\overline{RE}$ and then activates $\overline{MEMW}$.

E.) The DMAC waits for $\overline{REPLY}$ to go low. When $\overline{REPLY}$ is active the DMAC deactivates $\overline{MEMW}$ and then deactivates $\overline{RE}$.

F.) If the DMAC is *not* in hold bus mode (CR5=1) then the DMAC deactivates $\overline{DCS}$ and gives up control of the bus. If the DMAC is in hold bus mode then $\overline{DCS}$ remains low until after the completion of the final data transfer. Note that $\overline{BUSR}$ still cycles for every transfer.

G.) After the completion of every data transfer the memory address register is incremented by one in byte mode or two in word mode.

H.) After the completion of every data transfer the transfer count is incremented by one. Transfers are considered to be completed when the transfer count equals zero.

2.) MEMORY-TO-DEVICE DMA TRANSFERS (CR4=0)

Once the DMAC has been granted the bus it goes through the same steps as in the DEVICE-TO-MEMORY mode with the exception of steps "D" and "E" which are as follows:

D.) The DMAC activates $\overline{MEMR}$ and then activates $\overline{WE}$.

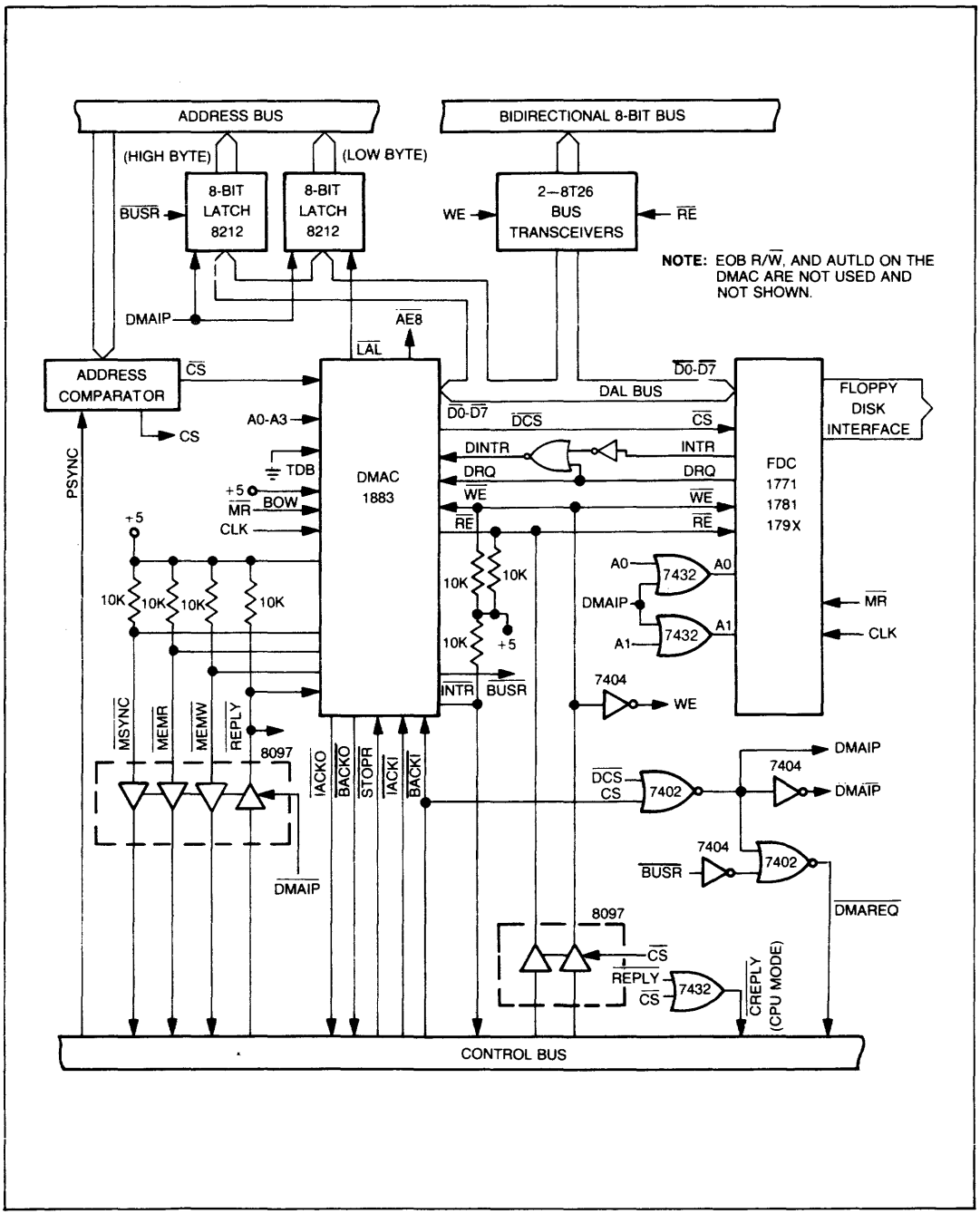
E.) The DMAC waits for $\overline{REPLY}$ to go low. When REPLY is active the DMAC deactivates $\overline{WE}$ and then deactivates $\overline{MEMR}$.

In either mode $\overline{BACKI}$ will be gated out to $\overline{BACKO}$ as soon as the DMAC deactivates $\overline{DCS}$. This allows other devices in the chain to gain access to the bus immediately.

INTERRUPTS

There are three individually enabled interrupt conditions. If any of the conditions occurs it will set its corresponding bit in the Status Register. If the

appropriate enable bit in the Command Register is set then INTR is also activated. Note that these are independent functions. When INTR is active then the DMAC can be selected by an active IACKI instead of an active CS. CS and IACKI must not both be active at the same time.



TYPICAL DMAC TO FDC APPLICATION

Once an interrupt condition sets its corresponding bit in the status register the bit stays set until a CPU write to the status register occurs with a zero in the bit position.* If any one (or more) of the three interrupt condition bits in the Status Register is set then IACKI will not be gated out to IACKO even if the interrupt is *not* enabled.

NOTE: For a transfer-count-equals-zero interrupt condition to be cleared the Transfer Count Register must be loaded with a non-zero count.

The three interrupt conditions are as follows:

1.) DEVICE INTERRUPT (DINT)

A device interrupt condition occurs when the DINTR input is made high. This sets SR1 and, if CR1 is set, it activates INTR. The RUN bit is also reset thus terminating all subsequent DMA transfers. A device interrupt could be generated by a number of causes, and the program will have to test the device's Status Register to determine the cause of the interrupt. The DINT status bit in the DMAC Status Register must be cleared by the program as a part of the interrupt service routine.

2.) TRANSFER COUNT EQUALS ZERO INTERRUPT (TCZI)

When the TCR is incremented to zero after a DMA transfer the TCZI status bit (SR3) is set and the RUN bit (CR0) is reset. This terminates all DMA operations and, if CR3 is set, activates INTR. SR3 can be cleared only by loading a non-zero value into the TCR. The EOB output pin is high whenever SR3 is set.

3.) TIME-OUT INTERRUPT (TOI)

During any DMA transfer the leading edge of MSYNC triggers an internal time delay of approximately 5 microseconds. If the DMAC does not receive an active low REPLY input within that time delay then the DMA operation is terminated, the RUN bit is reset, and the TOI status bit (SR2) is set. If CR2 is set then INTR is activated. SR2 can only be cleared by writing a zero into that position of the Status Register.

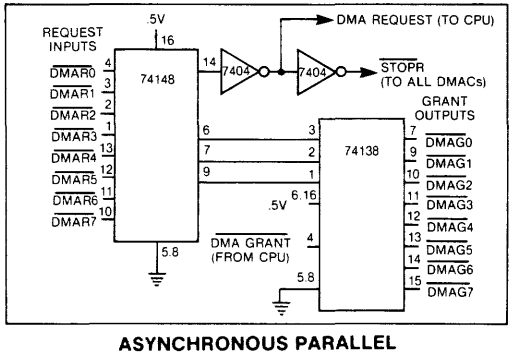
INTERRUPT OPERATION

When the DMAC activates INTR the CPU responds by activating IACKI. This signal can be daisy chained through all devices. The first device in the chain that has any bit in SR1-SR3 set will block the gating of IACKI out to IACKO. In addition, if INTR is active an IACKI will select the DMAC. An active RE after an IACKI select will gate the contents of the interrupt ID code register onto the DAL lines. The ID code stays active on the DAL lines as long as IACKI and RE are active. This code, which is cleared to zero by a MASTER RESET and loaded by the program during system initialization, can be used by the system to create a JUMP or VECTOR address for the device interrupt routine. Note that an active CS during a DMAC select via an active IACKI will cause unspecified results. Note also that no condition can activate INTR unless its corresponding enable bit is set and STOPR is high. If STOPR is active when the interrupt condition occurs then the DMAC will hold INTR inactive until STOPR goes inactive. At that time the DMAC will activate INTR automatically.

DMA PRIORITY SYSTEMS

Fixed Priority

A fixed priority can be established in two ways: through a parallel request-grant system or through a CPU controlled daisy chain system. A typical asynchronous parallel DMA priority system is shown. In this system any request generates an active STOPR, which is gated to all devices, and an active DMA request to the CPU. The CPU DMA grant generates a grant to the requesting device with the highest priority. If more than one request is received at the same time then the grants are honored from the highest to the lowest priority. In most cases, however, grants are not received simultaneously. The highest priority devices, therefore, will receive most of the immediate grants with the others being delayed by an active STOPR.



ASYNCHRONOUS PARALLEL DMA PRIORITY SYSTEM

Establishing a fixed priority system through a daisy chain approach requires the CPU monitor a "DMA IN PROGRESS" signal on the bus. This signal can be generated from DCS during a DMA transfer (i.e., DCS·CS). In this mode the CPU activates BACKI and STOPR in response to some bus request. STOPR is tied to all DMA controllers to prevent new bus requests while BACKI is propagating through all non-requesting DMAC devices. When the requesting DMAC gains control over the bus and activates DCS the CPU drops BACKI*. When DCS is deactivated the CPU deactivates STOPR to allow new requests. In this manner the device physically

closest to the CPU on the daisy chain has highest priority for all request cycles.

NOTE: $\overline{BACKI}$ and $\overline{STOPR}$ can be dropped at the same time with no effect on the priority scheme, but the CPU may have to capture new requests until $\overline{DCS}$ goes high.

Rotating Priority

This is a daisy chain approach that prevents one device from getting most of the bus grants if multiple devices are active at the same time. In this mode any device requesting the bus causes the CPU to activate $\overline{BACKI}$. This signal is tied to the $\overline{BACKI}$ and $\overline{STOPR}$ inputs of the first DMAC. The $\overline{BACKO}$ output of the first DMAC goes to the $\overline{BACKI}$ and $\overline{STOPR}$ inputs of the second DMAC, and so on. The $\overline{BACKO}$ output of the last DMAC in the chain goes back to the CPU to reset its $\overline{BACKI}$ output. In this mode the first device cannot request again until all other requesting devices in the chain have also been serviced.

In any case, if the CPU has to have the DMA request held active throughout the DMA cycle then the user will have to create this signal on the controller thusly: DMAREQ = BUSR + (DCS·$\overline{CS}$). If the device and DMAC chip selects are generated on the controller separately then the $\overline{CS}$ can be eliminated from the equation. It is needed only to distinguish a CPU chip select from a DMA cycle chip select. Note that in either case the second term in the equation is equivalent to "DMA CYCLE IN PROGRESS" (DMAIP).

SPECIFICATIONS

Absolute Maximum Ratings

Ambient Temperature Under Bias...0°C to +70°C
Voltage on Any Pin with Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 0.6 Watt

NOTE: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND =0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100 µA
I_{DL}	Data Bus Leakage			-50	µA	V_{IN} = 0.45V
				10	µA	V_{IN} = V_{CC}
I_{IL}	Input Leakage			10	µA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	90	mA	

NOTE: VOL ≤0.4V when interfacing with low power Schottky parts (I_{OL} <1 mA).

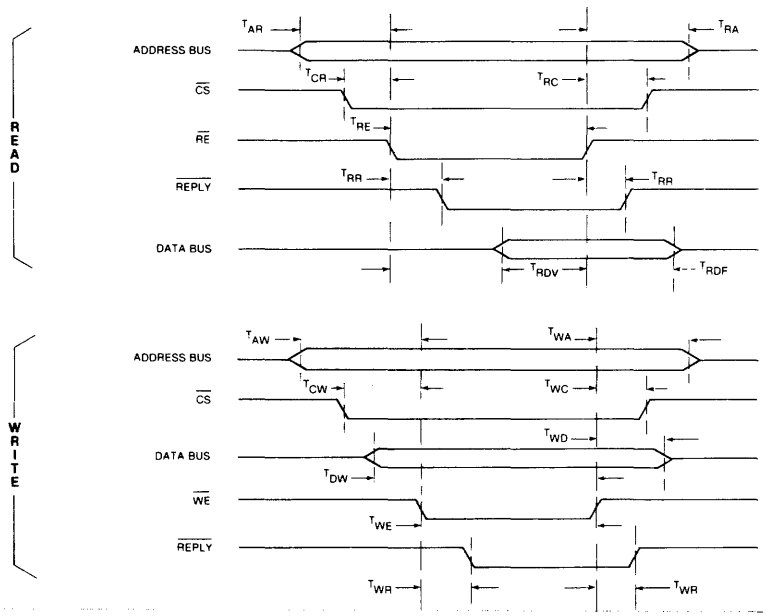
Capacitance

T_A = 25°C; V_{CC} = GND = 0V

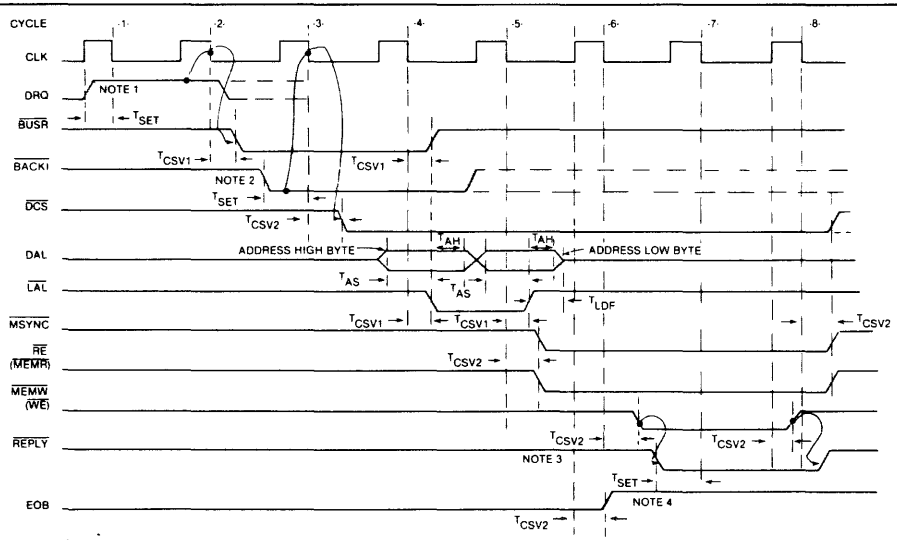
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

System Clock (CLK) Characteristics

Maximum Frequency = 2.0 MHz
Minimum Pulse Width = 250 ns
Maximum Pulse Width = 50% of duty cycle



CPU CONTROLLED TRANSFER



NOTES:
1. BUSR ↓ FOLLOWS SECOND CLK ↓ AFTER DRZ ↑.
2. a. CYCLE 2 IS SKIPPED FOR ALL SUBSEQUENT TRANSFERS WHEN IN THE HOLD MODE, I.E., DCS REMAINS LOW FOR ENTIRE BLOCK OF TRANSFERS.
   b. FOLLOWING BUSR ↓ WITH DCS HIGH (I.E., REQUESTING BUS CONTROL), THE DMA WILL ADD WAIT CYCLES BETWEEN CYCLES 2 AND 3 UNTIL BACK1 ↓ IS RECEIVED.
3. CYCLE 7 WILL BE REPEATED FOR EACH ADDITIONAL PERIOD THAT REPLY ↓ IS DELAYED TO THE DMA. CYCLE 7 WILL BE SKIPPED (I.E., MEMW (WE) PULSE WIDTH = 1/2 CLK PERIOD) IF REPLY IS MADE LOW PRIOR TO CLK ↓ OF CYCLE 6 (E.G., REPLY TIED TO GND DURING DMA TRANSFER).
4. EOB IS ACTIVATED ONLY FOR THE TRANSFER WHERE TCR INCREMENTS FROM 11 . . . 1 TO 00 . . . 0 (I.E., END OF BLOCK).
5. TO INSURE PROPER LOADING OF DAL BUS CONTENTS INTO THE CONTROLLER REGISTERS, THE WE PULSE WIDTH MUST BE GREATER THAN OR EQUAL TO ONE CLK PERIOD. THIS REQUIREMENT CAN ALSO BE SOLVED OFF CHIP BY TRIGGERING WE ↑ (TRAILING EDGE) WITH CLK ↓.

DMA CONTROLLED TRANSFER TIMING

AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	DESCRIPTION	MIN	MAX.	UNIT	COND
CPU CONTROLLED TRANSFER TIMING - READ					
T_{AR}	Address Valid to $\overline{RE}$ ↓	80		ns	
T_{CR}	$\overline{CS}$ ↓ to $\overline{RE}$ ↓	0		ns	
T_{RE}	$\overline{RE}$ Pulse Width	300		ns	
T_{RDV}	$\overline{RE}$ ↓ to Data Valid		375	ns	CL = 50 pF
T_{RR}	$\overline{RE}$ ↓ (↓) to $\overline{REPLY}$ ↓ (↓)	50	350	ns	CL = 50 pF
T_{RA}	Address Hold from $\overline{RE}$ ↑	30		ns	
T_{RC}	$\overline{CS}$ Hold from $\overline{RE}$ ↑	0		ns	
T_{RDF}	Data Float from $\overline{RE}$ ↑		200	ns	
CPU CONTROLLED TRANSFER TIMING - WRITE					
T_{AW}	Address Valid to $\overline{WE}$ ↓	80		ns	
T_{CW}	$\overline{CS}$ ↓ to $\overline{WE}$ ↓	0		ns	
T_{DW}	Data Valid to $\overline{WE}$ ↑	300		ns	CL = 50 pF
T_{WE}	$\overline{WE}$ Pulse Width	300		ns	
T_{WR}	$\overline{WE}$ ↓ (↓) to $\overline{REPLY}$ ↓ (↓)	50	350	ns	CL = 50 pF
T_{WA}	Address Hold from $\overline{WE}$ ↑	30		ns	
T_{WC}	$\overline{CS}$ Hold from $\overline{WE}$ ↑	0		ns	
T_{WD}	Data Hold from $\overline{WE}$ ↑	30		ns	

SYMBOL	DESCRIPTION	MIN	TYP	MAX.	UNIT	COND
DMA CONTROLLED TRANSFER TIMING						
T_{CSV1}	Indicated CLK Edge to Indicate Signal Valid		150	250	ns	CL = 50 pF
T_{CSV2}	Indicated CLK Edge to Indicated Signal Valid		250	400	ns	CL = 50 pF
T_{AS}	DAL Set Up to $\overline{BUSR}$ ↑ or $\overline{LAL}$ ↓ (↓)	80			ns	CL = 50 pF
T_{AH}	DAL Hold from $\overline{BUSR}$ ↑ or $\overline{LAL}$ ↓ (↓)	50			ns	CL = 50 pF
T_{LDF}	$\overline{LAL}$ ↑ to DAL Float			250	ns	CL = 50 pF
T_{SET}	Indicated Signal Setup to Indicated CLK Edge	80			ns	
MISCELLANEOUS TIMING (τ = 1 CLOCK PERIOD)						
$\overline{CS}$ ↓ (↓) To $\overline{DCS}$ ↓ (↓) Propogation Delay (for A3 low)			150	250	ns	CL = 50 pF
$\overline{IACKI}$ ↓ (↓) to $\overline{IACKO}$ ↓ (↓) Propogation Delay when Not Requesting Interrupt			150	250	ns	CL = 50 pF
$\overline{BACKI}$ ↓ (↓) to $\overline{BACKO}$ ↓ (↓) Propogation Delay when Not Requesting Bus			150	250	ns	CL = 50 pF
$\overline{MR}$ Pulse Width	2τ					
DINTR, AUTLD, DRQ, $\overline{REPLY}$ Pulse Width	1τ					
BOW ↓ (↓) or TDB ↓ (↓) Set Up	500				ns	
Waiting $\overline{INTR}$ ↓ or $\overline{BUSR}$ ↓ from $\overline{STOPR}$ ↑				1τ - 400	ns	CL = 50 pF
$\overline{INTR}$ ↓ from DINTR ↑				1.5τ - 400	ns	CL = 50 pF

NOTE: A 1 TTL load is assumed on all output signals

See page 481 for ordering information.

Printed in U.S.A

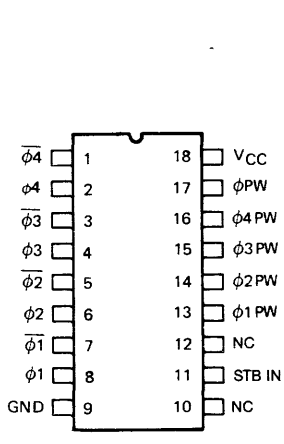
WD2143-03 Four Phase Clock Generator

FEATURES

- IMPROVED VERSION OF WD2143-01
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- TTL CLOCK INPUT
- TTL CLOCK OUTPUTS
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR

GENERAL DESCRIPTION

The WD2143-03 Four-Phase Clock Generator is a MOS/LSI device capable of generating four phase clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ϕPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate ϕ1PW—ϕ4PW control inputs.



PIN DESIGNATION

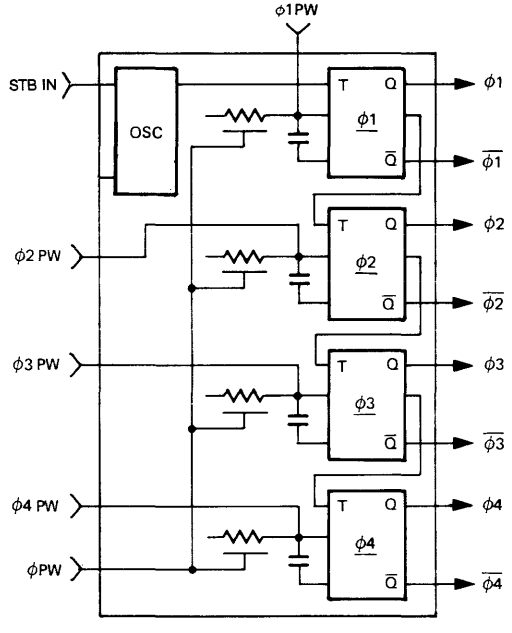


Figure 1 WD2143-03 BLOCK DIAGRAM

DEVICE OPERATION

Each of the phase outputs can be controlled individually by typing an external resistor from ϕ1PW-ϕ4PW to a +5V supply. When it is desired to have ϕ1 through ϕ4 outputs the same width, the ϕ1PW-ϕ4PW inputs should be left open and an external resistor tied from the ϕPW (Pin 17) input to +12V.

STROBE IN (pin 11) is driven by a TTL square wave. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

PIN NUMBER	SYMBOL	DESCRIPTION
1, 3, 5, 7	$\overline{\phi 1}$—$\overline{\phi 4}$	Four phase clock outputs. These outputs are inverted (active low).
2, 4, 6, 8	ϕ1-ϕ4	Four Phase clock outputs. These outputs are true (active high).
9	GND	Ground
10	NC	No connection
11	STB IN	Input signal to initiate four-phase clock outputs.
12	NC	No connection
13-16	ϕ1PW-ϕ4PW	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if ϕPW is used.
17	ϕPW	External resistor input to control all phase outputs to the same pulse widths.
18	V_{CC}	+5V ± 5% power supply input

Table 1 PIN DESCRIPTIONS

TYPICAL APPLICATIONS

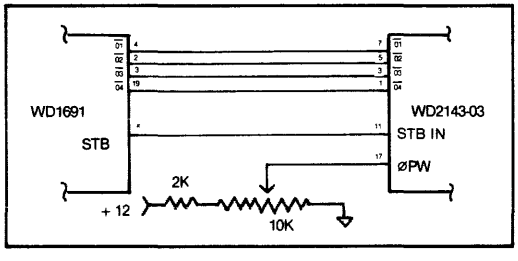


Figure 2 WRITE PRECOMP OPERATION WITH F.S.L. WD1691

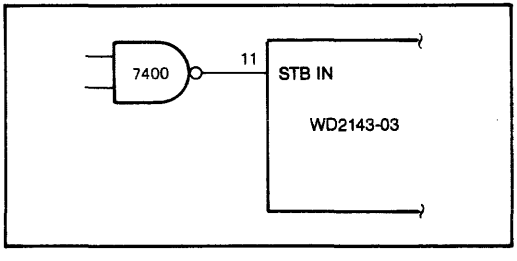


Figure 3 TTL SQUARE WAVE OPERATION

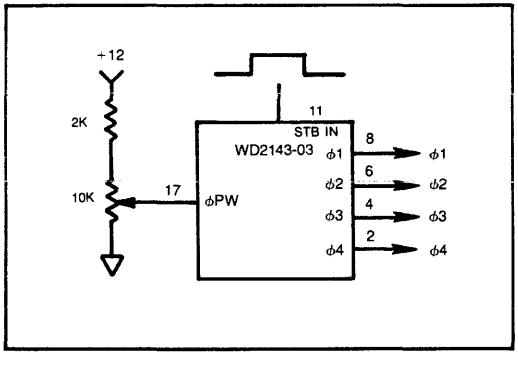


Figure 4 EQUAL PULSE WIDTH OUTPUTS

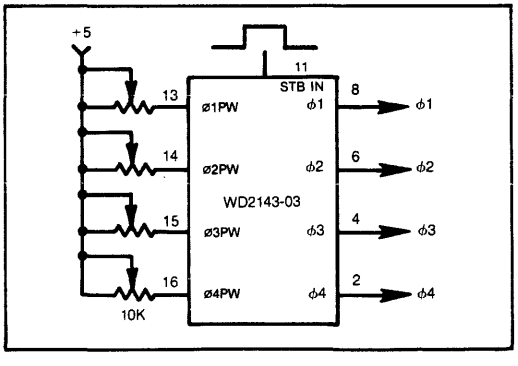


Figure 5 INDIVIDUAL PULSE WIDTH OUTPUTS

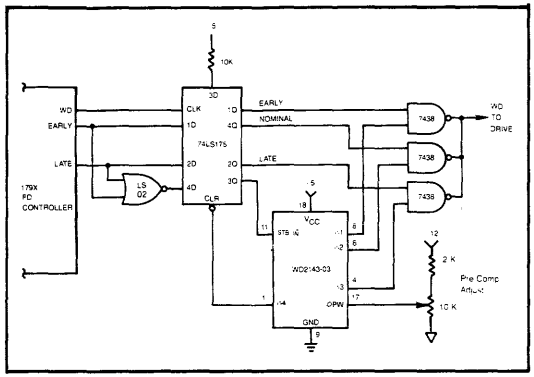


Figure 6 WRITE PRECOMP FOR FLOPPY DISK

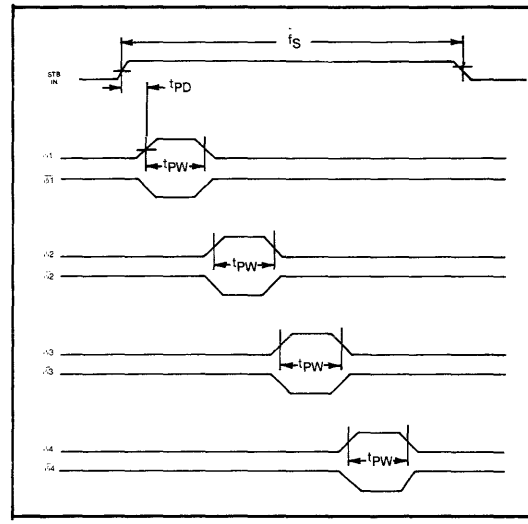


Figure 7 WD2143-03 TIMING DIAGRAM

SPECIFICATIONS

Absolute Maximum Ratings		
Operating Temperature		0° to +70° C
Voltage on any pin with respect to Ground*		−0.5 to +7V
Power Dissipation		1 Watt
Storage Temperature	plastic	−55° to +125° C
	ceramic	−65° to +150°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.

*Pin 17 = −0.5V to +12V. Increasing voltage on Pin 17 will decrease T_{pw}.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, GND = OV, T_A = 0° to 70°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{OL}	TTL low level output		0.4	V	i_{OL} = 1.6 mA
V_{OH}	TTL high level output	2.0		V	i_{OH} = −100 μA
V_{IL}	STB in low voltage		0.8	V	
V_{IH}	STB in high voltage	2.4		V	
i_{CC}	Supply Current		80	mA	All outputs open

Table 2 DC ELECTRICAL CHARACTERISTICS

SWITCHING CHARACTERISTICS

V_{CC} =5V ± 5%, GND = 0V T_A = 0° to 70° C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
t_{PD}	STB IN to ø1		140	ns	
t_{pw}	Pulse Width (any output)	100	300	ns	CL = 30pf
t_{PR}	Rise Time (any output)		30	ns	CL = 30pf
t_{PF}	Fall Time (any output)		25	ns	CL = 30pf
f_S	STROBE PULSE WIDTH		1.0	μs	combined t_{pw} = 400 ns
t_{DPW}	Pulse Width Differential		± 10	%	Referenced to ø1, 100-300 ns.

Table 3 SWITCHING CHARACTERISTICS

NOTE: T_{PW} measured at 50% V_{OH} Point; V_{OL} = 0.8V, V_{OH} = 2.0V.

See page 481 for ordering information.

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WESTERN DIGITAL
CORPORATION

WD9216-00/WD9216-01
Floppy Disk Data Separator — FDDS

FEATURES

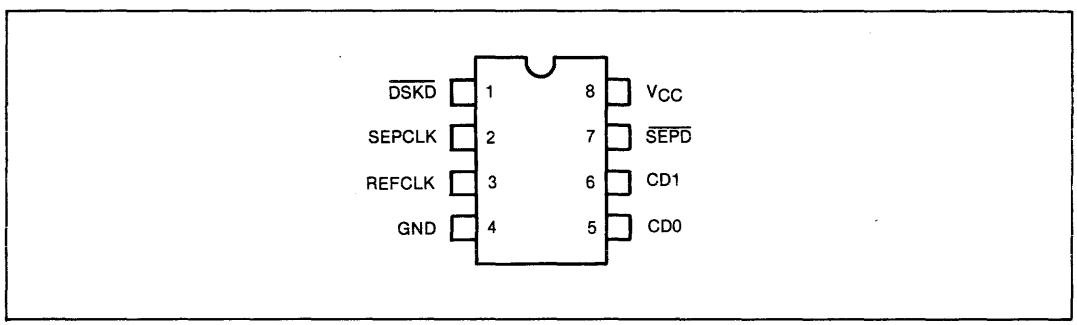
- PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- NO CRITICAL ADJUSTMENTS REQUIRED
- COMPATIBLE WITH WESTERN DIGITAL 179X, 176X AND OTHER FLOPPY DISK CONTROLLERS
- SMALL 8-PIN DUAL-IN-LINE PACKAGE
- +5 VOLT ONLY POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS

GENERAL DESCRIPTION

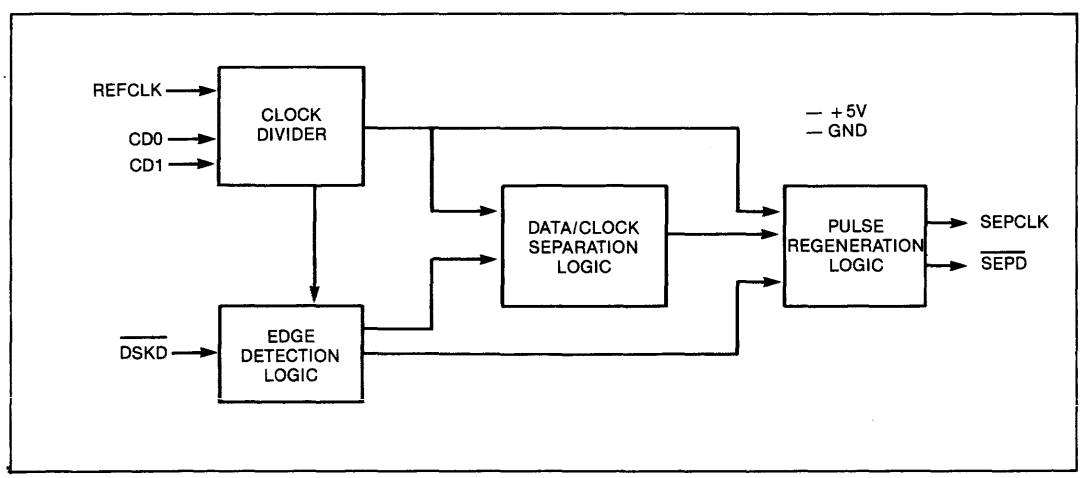
The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The WD9216 is available in two versions; the WD9216-00, which is intended for 5¼" disks and the WD9216-01 for 5¼" and 8" disks.



PIN CONFIGURATION



FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range..... −55°C to 125°C
Positive Voltage on any Pin,
with respect to ground..... +8.0V
Negative Voltage on any Pin,
with respect to ground..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

OPERATING CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER		MIN.	TYP.	MAX.	UNITS	COMMENTS
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL} = 1.6mA
High Level V_{OH}		2.4			V	I_{OH} = −100μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$0 \leq V_{IN} \leq V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				50	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	WD 9216-00
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	WD 9216-01
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	100			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

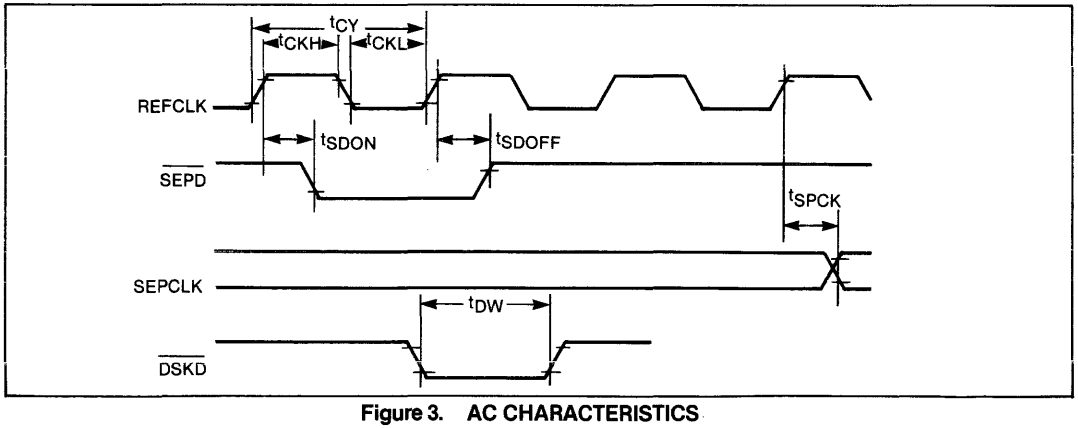


Figure 3. AC CHARACTERISTICS

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	Disk Data	$\overline{DSKD}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input.
4	Ground	GND	Ground.
5,6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	Separated Data	$\overline{SEPD}$	SEPD is the data output of the FDDS
8	Power Supply	V_{CC}	+5 volt power supply

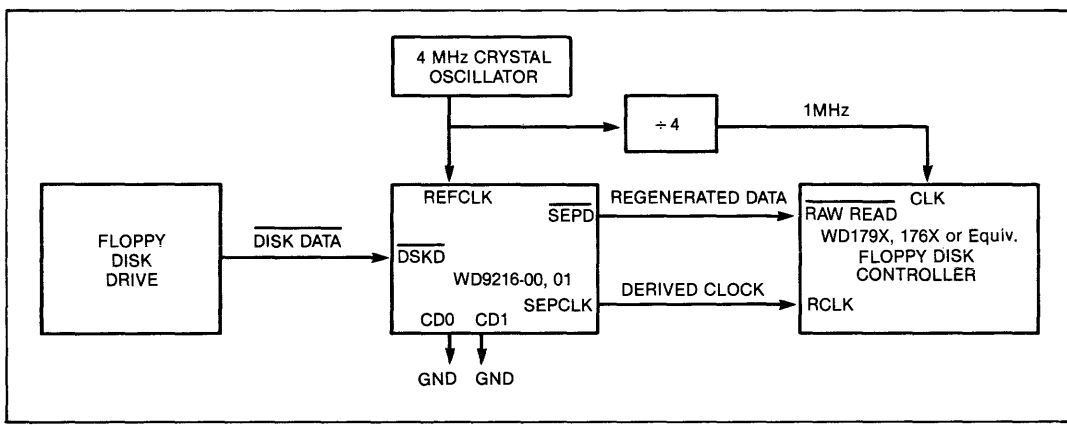


Figure 1.
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)

OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8″ or 5¼″)	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	Select either one
8	SD	8	0	1	
8	SD	4	0	0	
5¼	DD	8	0	1	Select either one
5¼	DD	4	0	0	
5¼	SD	8	1	0	Select any one
5¼	SD	4	0	1	
5¼	SD	2	0	0	

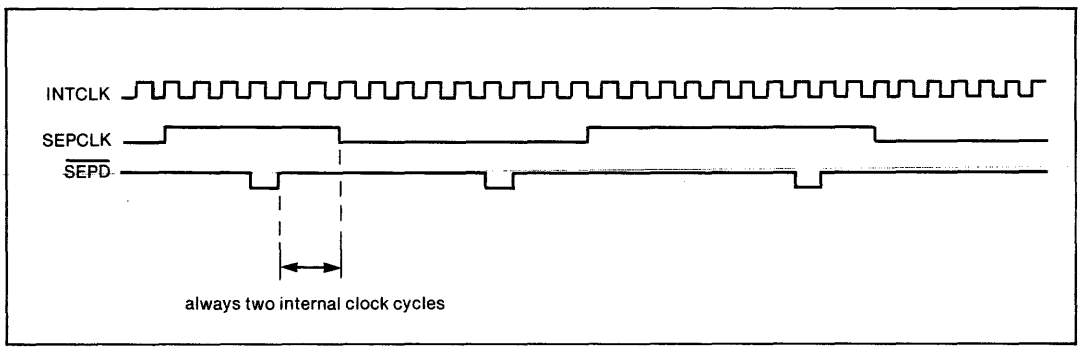


Figure 2.

See page 481 for ordering information.

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WD1100 Series Winchester Controller Chips

DESCRIPTION

The WD1100 Chip series provides a low cost alternative for developing a Winchester Controller. These devices have been designed to read and convert an MFM data stream into 8-bit parallel bytes. During a write operation, parallel data is converted back into MFM to be written on the disk. Address Marks are generated and detected while CRC bytes can be appended and checked on the data stream. The WD1100 is fabricated in N-channel silicon gate technology and is available in a 20-pin Dual-In-Line package.

- WD1100-01 SER/PARALLEL CONVERTER
- WD1100-02 MFM GENERATOR
- WD1100-12 IMPROVED MFM GENERATOR
- WD1100-03 AM DETECTOR
- WD1100-04 CRC GENERATOR/CHECKER
- WD1100-05 PAR/SERIAL CONVERTER
- WD1100-06 ECC/CRC LOGIC
- WD1100-07 HOST INTERFACE LOGIC
- WD1100-09 DATA SEPARATION SUPPORT LOGIC

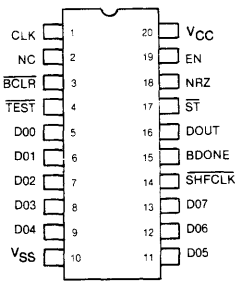
FEATURES

- SA1000/ST506 COMPATIBLE
- SINGLE 5V SUPPLY
- TRI-STATE DATA LINES
- 5 MBITS/SEC TRANSFER RATE
- SIMPLIFIED INTERCONNECT

APPLICATIONS

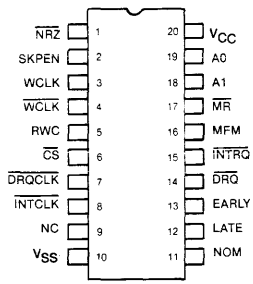
Winchester Controllers For:

- SHUGART ASSOCIATES
- SEAGATE TECHNOLOGY
- QUANTUM CORP.
- TANDON MAGNETICS
- MINISCRIBE
- RMS
- CMI . . . AND OTHERS



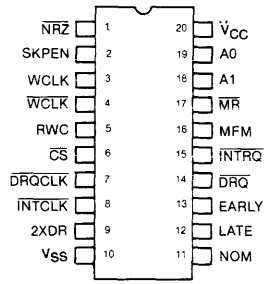
WD1100-01

SERIAL/PARALLEL CONVERTER



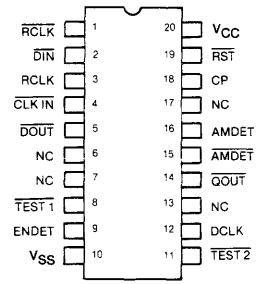
WD1100-02

MFM GENERATOR



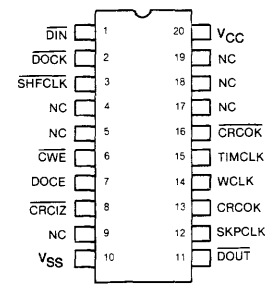
WD1100-12

IMPROVED MFM GENERATOR



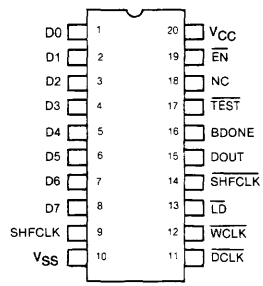
WD1100-03

AM DETECTOR



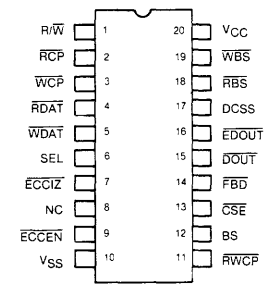
WD1100-04

CRC GENERATOR/CHECKER



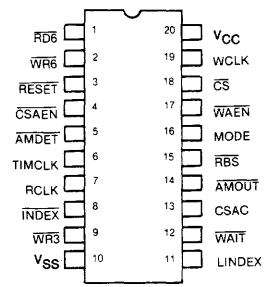
WD1100-05

PARALLEL/SERIAL CONVERTER



WD1100-06

ECC/CRC LOGIC



WD1100-07

HOST INTERFACE LOGIC

See page 481 for ordering information.

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Western Digital
WD1100-01 Serial/Parallel Converter

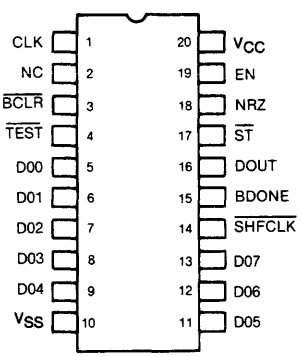
DESCRIPTION

The WD1100-01 Serial/Parallel Converter allows the user to convert NRZ (non-return to zero) data from a Winchester disk drive into 8 bit parallel form. Additional inputs are provided to signal the start of the parallel process, as well as Byte Strobes to signify the end of the conversion. The device contains two sets of 8-bit registers; one register may be read (in parallel), while data is being shifted into the other register. This double-buffering allows the Host to read data from the disk drive at one-eighth the actual data rate.

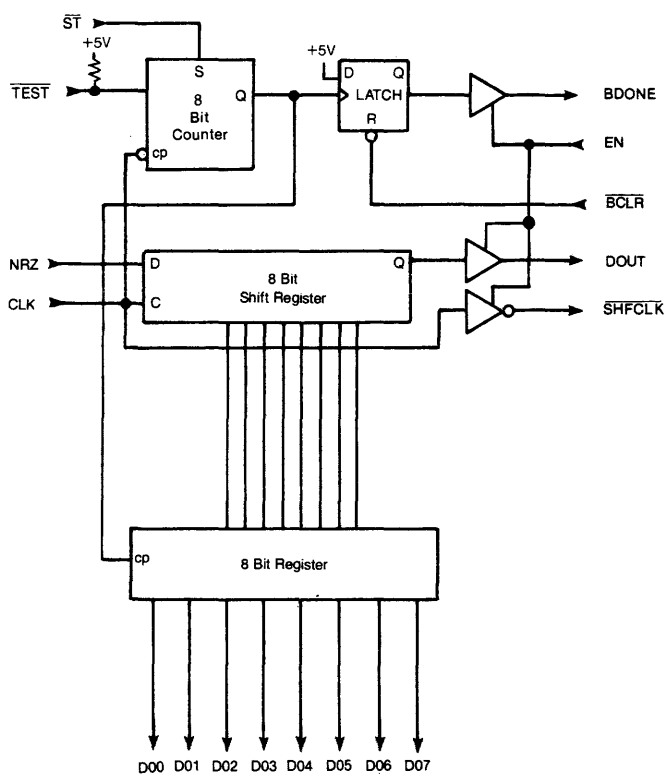
The WD1100-01 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5MBITS/SEC SHIFT RATE
- SERIAL IN/SERIAL-PARALLEL OUT
- 20 PIN DIP PACKAGE



WD1100-01
Figure 1. Pin Connections



WD1100-01
Figure 2. Block Diagrams

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (Pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9, 11-13	D00-D07	DATA0-DATA7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (Pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the WD1100-01 must be synchronized to the data stream. The $\overline{ST}$ line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. BCLR has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear off BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that $\overline{BCLR}$ be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The $\overline{TEST}$ pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin
with respect to V_{SS} ..... −0.2V to +7.0V
Power Dissipation..... 1 Watt
STORAGE TEMPERATURE
PLASTIC..... −55°C to +125°C
CERAMIC..... −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

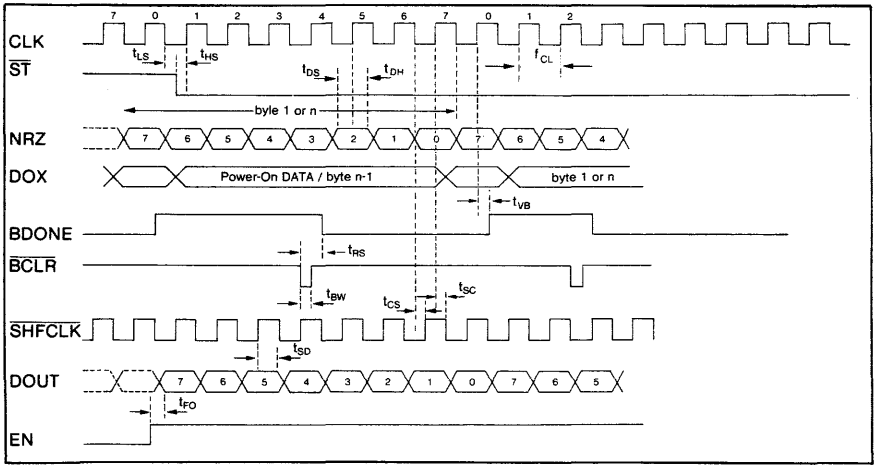
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNITS	CONDITION
f_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑CLK	15			nsec	
t_{VB}	BDONE valid from ↑CLK	65		110	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			110	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑CLK to ↓$\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓CLK to ↑$\overline{SHFCLK}$			100	nsec	EN = 1
t_{SD}	Data delay from ↑$\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑CLK	25			nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-01
Figure 3.

See page 481 for ordering information.

Western Digital
WD1100-02 MFM Generator

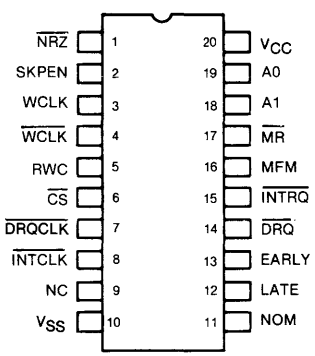
DESCRIPTION

The WD1100-02 MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-02 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

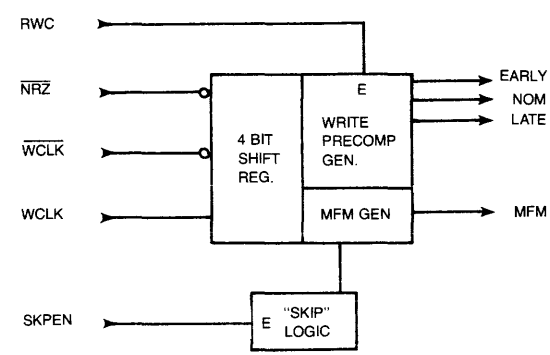
The WD1100-02 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

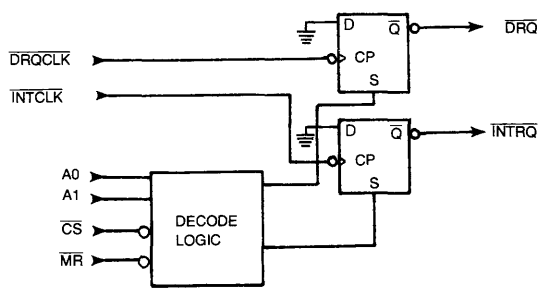
- SINGLE + 5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION
- 20 PIN DIP PACKAGE



WD1100-02
Figure 1. Pin Connections



WD1100-02
Figure 2. Block Diagram MFM Generator



WD1100-02
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	NON-RETURN-TO ZERO	NRZ data input that is strobed into the MFM generator by WCLK (↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	WRITE CLOCK	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	NC	No Connection	No Connection.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	CHIP SELECT	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	INTERRUPT REQUEST CLOCK	A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	DATA REQUEST CLOCK	A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	INTERRUPT REQUEST	This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled.
14	$\overline{DRQ}$	DATA REQUEST	This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled.
17	$\overline{MR}$	MASTER RESET	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 1, 0	When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ±10% power supply input.

DEVICE DESCRIPTION

The WD1100-02 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 8.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the $\overline{NRZ}$ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

$\overline{MR}$	A_1	A_0	$\overline{CS}$	$\overline{DRQ}$	$\overline{INTRQ}$
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only on the high-to-low transition of $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . −0.2V to + 7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE:
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C, V_{CC} = +5V ± 10%, V_{SS} = 0V

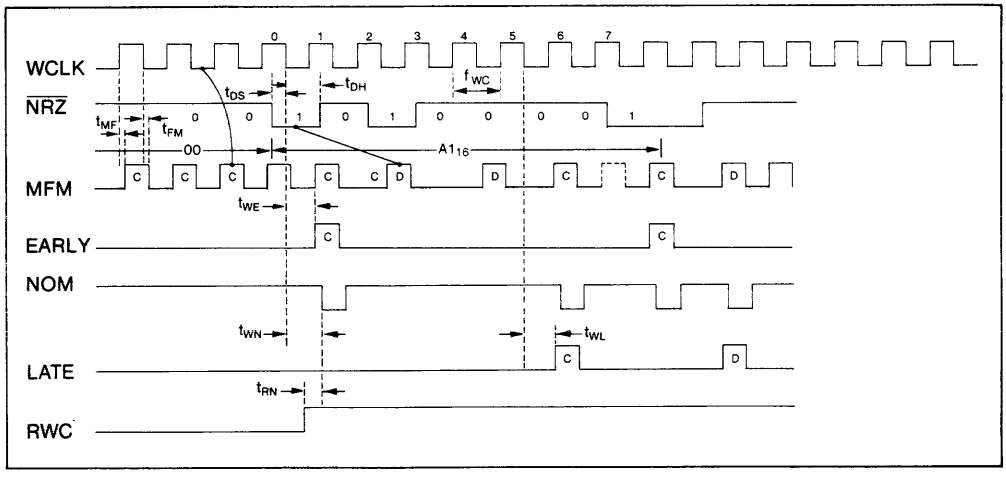
SYMBOL	PARAMETER	MIN	TYP¹	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{OC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

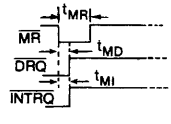
SYMBOL	PARAMETER	MIN	TYP¹	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓ WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓ WCLK	25			nsec	
t_{MF}	↑ WCLK to ↑ MFM delay			160	nsec	Pin 1 LOW
t_{FM}	↓ WCLK to ↓ MFM delay			180	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓ WCLK			190	nsec	Pin 4 = LOW
t_{WE}	Data delay to EARLY from ↓ WCLK			180	nsec	Pin 4 = LOW
t_{WL}	Data delay to LATE from ↓ WCLK			180	nsec	Pin 4 = LOW
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓ $\overline{MR}$ to ↑ $\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑$\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓$\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓$\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑$\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑$\overline{INTRQ}$			160	nsec	
t_{CD}	↓$\overline{CS}$ to ↑$\overline{DRQ}$			145	nsec	
t_{CI}	↓$\overline{CS}$ to ↑$\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			115	nsec	

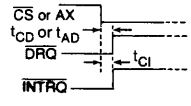
NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



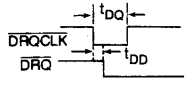
WD1100-02
Figure 4. MFM Generator Timing



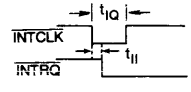
WD1100-02
Figure 5



WD1100-02
Figure 6



WD1100-02
Figure 7.



WD1100-02
Figure 8.

See page 481 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-12 Improved MFM Generator

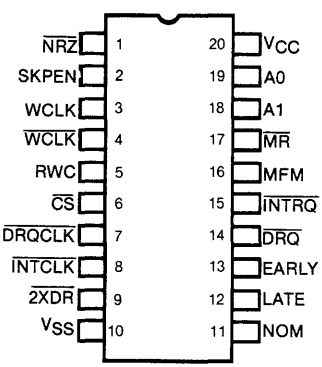
DESCRIPTION

The WD1100-12 improved MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-12 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

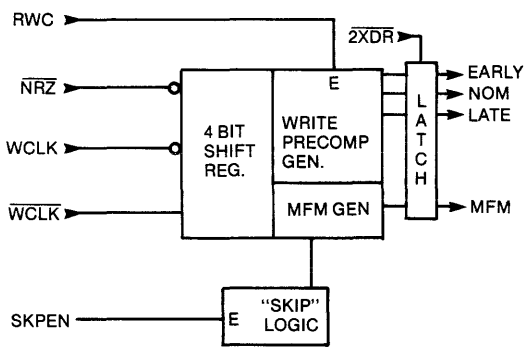
The WD1100-12 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

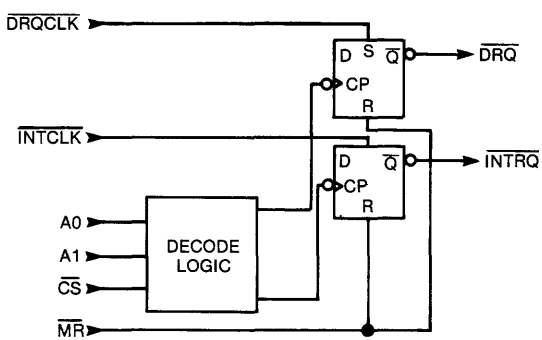
- SINGLE +5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION



WD1100-12
Figure 1. Pin Connections



WD1100-12
Figure 2. Block Diagram MFM Generator



WD1100-12
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	$\overline{NON\text{-}RETURN\text{-}TO\ ZERO}$	NRZ data input that is strobed into the MFM generator by WCLK(↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	$\overline{WRITE\ CLOCK}$	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2XDR}$	$\overline{2\ TIMES\ DATA\ RATE}$	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	$\overline{CHIP\ SELECT}$	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	$\overline{INTERRUPT\ REQUEST\ CLOCK}$	A low on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	$\overline{DATA\ REQUEST\ CLOCK}$	A low on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	$\overline{INTERRUPT\ REQUEST}$	This output is latched at a logic 0 when INTCLK (pin 8) goes/ is low.
14	$\overline{DRQ}$	$\overline{DATA\ REQUEST}$	This output is latched at a logic 0 when DRQCLK (pin 7) goes/is low.
17	$\overline{MR}$	$\overline{MASTER\ RESET}$	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 0, 1	When CS is low and the address lines go high, INTRQ is cleared; if the address lines go low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

The WD1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 4.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

MR	A_1	A_0	CS	DRQ	INTRQ
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ... −0.2V to +7.0V
Power Dissipation..... 1 Watt

STORAGE TEMPERATURE:
PLASTIC..... −55°C to +125°C
CERAMIC..... −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

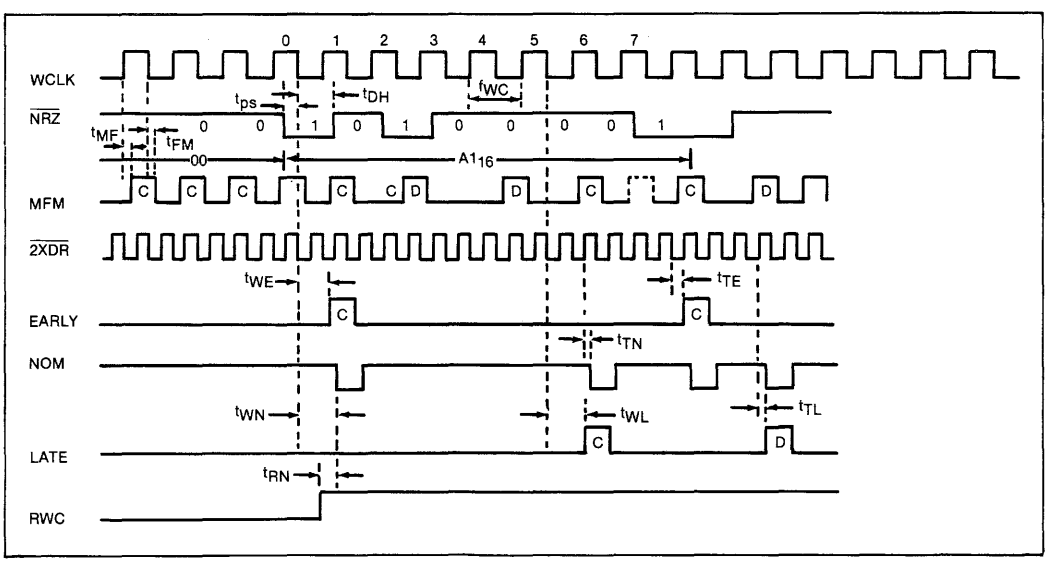
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

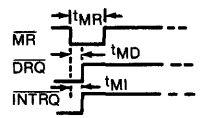
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓WCLK	25			nsec	
t_{MF}	↑WCLK to ↑MFM delay			210	nsec	Pin 1 LOW
t_{FM}	↓WCLK to ↓MFM delay			230	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓WCLK			240	nsec	
t_{WE}	Data delay to EARLY from ↓WCLK			230	nsec	
t_{WL}	Data delay to LATE from ↓WCLK			230	nsec	
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓$\overline{MR}$ to ↑$\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑ $\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓ $\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓ $\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑ $\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑ $\overline{INTRQ}$			160	nsec	
t_{CD}	↓ $\overline{CS}$ to ↑ $\overline{DRQ}$			145	nsec	
t_{CI}	↓ $\overline{CS}$ to ↑ $\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			145	nsec	
t_{TE}	↓ $\overline{2XDR}$ to ↑EARLY			75	nsec	
t_{TN}	↓ $\overline{2XDR}$ to ↑NOM			75	nsec	
t_{TL}	↓ $\overline{2XDR}$ to ↑LATE			75	nsec	

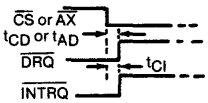
NOTES: 1. Typical Values are for $T_A = 25°C$ and $V_{CC} = +5.0V$.



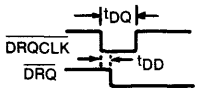
WD1100-12 Figure 4 MFM GENERATOR TIMING



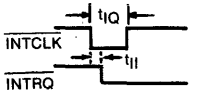
WD1100-12 Figure 5



WD1100-12 Figure 6



WD1100-12 Figure 7



WD1100-12 Figure 8

See page 481 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-03 AM Detector

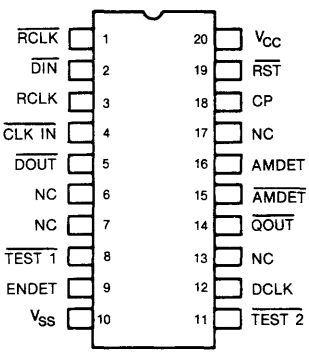
DESCRIPTION

The WD1100-03 Address Mark Detector provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM (NRZ) clocks and data are fed to the device along with a window clock generated by an external data separator. The WD1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces an AM DET signal when the pattern has been found. NRZ data is an output from the device, which can be used to drive a serial/parallel converter. An uncommitted latch is also provided for by the data separator circuitry, if required.

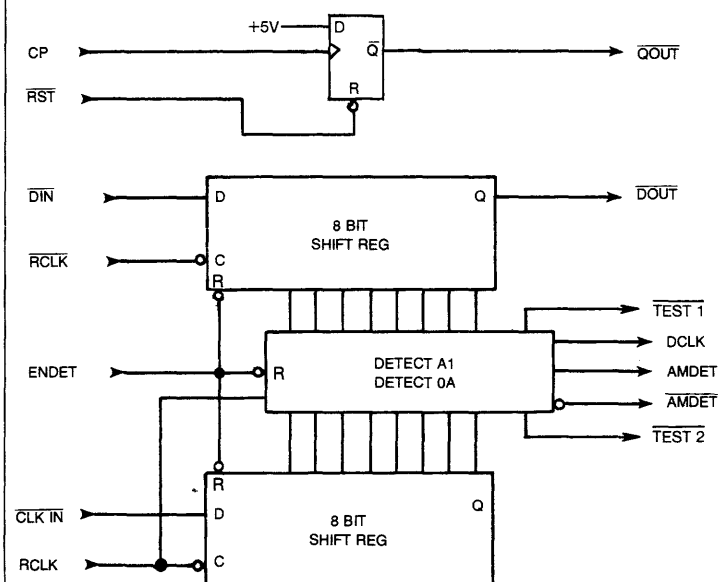
The WD1100-03 Address Mark Detector is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- SINGLE + 5V SUPPLY
- 5 MBITS/SEC DATA RATE
- DECODES $A1_{16}$-$0A_{16}$
- SYNCHRONOUS CLOCK/DATA OUTPUTS
- 20 PIN DIP PACKAGE



WD1100-03
Figure 1. Pin Connections



WD1100-03
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1 3	$\overline{\text{RCLK}}$ RCLK	$\overline{\text{READ CLOCK}}$ READ CLOCK	Complimentary clock inputs used to clock DIN and $\overline{\text{CLK}}$ IN into the AM detector.
2	$\overline{\text{DIN}}$	$\overline{\text{DATA INPUT}}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{\text{CLK IN}}$	$\overline{\text{CLOCK INPUT}}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{\text{DOUT}}$	$\overline{\text{DATA OUTPUT}}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user
8 11	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{\text{DATA OUT}}$ (Pin 5).
14	$\overline{\text{QOUT}}$	$\overline{\text{LATCH OUTPUT}}$	Signal output from the uncommitted latch.
15	$\overline{\text{AMDET}}$	$\overline{\text{ADDRESS MARK DETECT}}$	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$
16	AMDET	ADDRESS MARK DETECT	pattern is detected in the data stream.
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{\text{QOUT}}$ (Pin 14) to be latched at a logic 0.
19	$\overline{\text{RST}}$	$\overline{\text{RESET}}$	A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and $\overline{\text{AMDET}}$, AMDET, $\overline{\text{CLK}}$, and $\overline{\text{DATA OUT}}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{\text{DIN}}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{\text{RCLK}}$ (Pin 1). NRZ clocks are entered on the $\overline{\text{CLK}}$ IN line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{\text{DOUT}}$ line (Pin 5) is tied to the last stage of the internal Data Shift register and will reflect information clocked into the DIN line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$, CLK = $0A_{16}$ pattern. When this pattern is detected, AMDET will be set to a logic 0 and $\overline{\text{AMDET}}$ will be set to a logic 1. $\overline{\text{AMDET}}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{\text{DOUT}}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{\text{QOUT}}$ (Pin 14) to a logic 0. $\overline{\text{QOUT}}$ may be reset back to a logic 1 by a low level on the $\overline{\text{RST}}$ line (Pin 19).

$\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$ are output lines. $\overline{\text{TEST1}}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{\text{TEST2}}$ is active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ... −0.2V to +7.0V
Power dissipation ..... 1 Watt

STORAGE TEMPERATURE
PLASTIC ..... −55°C to +125°C
CERAMIC ..... −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

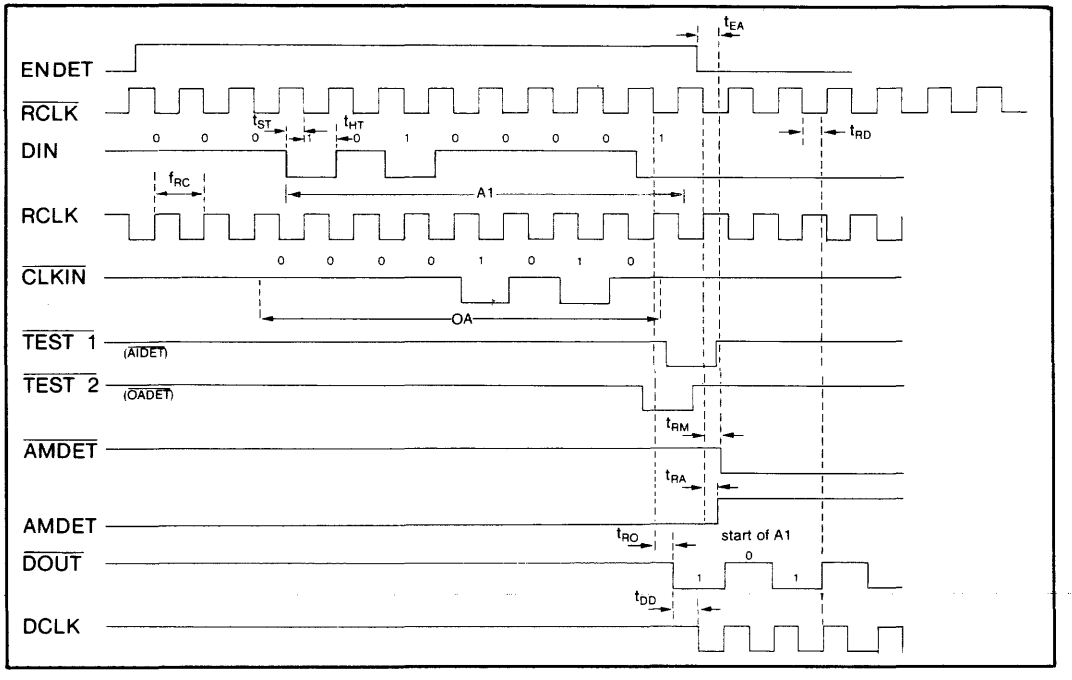
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.7	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{RC}	RCLK Frequency			5.25	MHZ	
t_{ST}	Data Setup time	40			nsec	
t_{HT}	Data Hold time	10			nsec	
t_{DD}	$\overline{DOUT}$ to DCLK DELAY			110	nsec	
t_{RD}	↓ $\overline{RCLK}$ to ↑ DCLK			120	nsec	
t_{RA}	↓ $\overline{RCLK}$ to ↑ AMDET			115	nsec	
t_{RM}	↓ $\overline{RCLK}$ to ↓ $\overline{AMDET}$			125	nsec	
t_{RO}	↓ $\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ ENDET to ↓ AMDET			130	nsec	
t_{RQ}	↓ $\overline{RST}$ to ↑ $\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse width	90			nsec	
t_{CQ}	↑ CP to ↓ $\overline{QOUT}$			106	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5V.



WD1100-03
Figure 3. Functional Timing

See page 481 for ordering information.

Printed in U.S.A

Western Digital
WD1100-04 CRC Generator/Checker

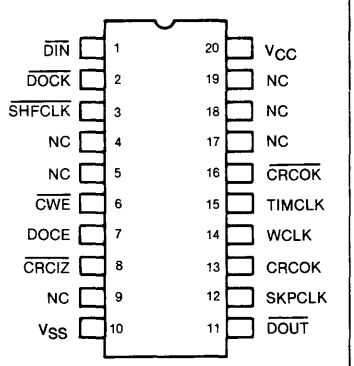
DESCRIPTION

The WD1100-04 CRC Generator/Checker is designed to generate a Cyclic Redundancy Checkword from a serial data stream, and to check a data stream against a known CRC word. Complimentary latched "CRCOK" outputs are provided to indicate CRC errors in check mode. Additional logic has been included to shift the CRC checkword out of the device by signals generated on other WD1100 family devices.

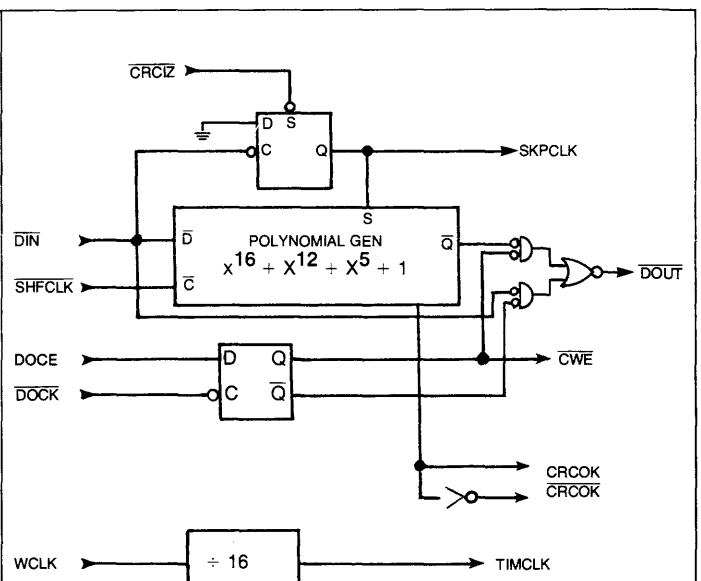
The WD1100-04 is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- GENERATES/CHECKS CRC
- SINGLE +5V SUPPLY
- LATCHED ERROR OUTPUTS
- $X^{16} + X^{12} + X^5 + 1$ (CCITT-16)
- AUTOMATIC PRESET
- 20 PIN DIP PACKAGE



WD1100-04
Figure 1. Pin Connections



WD1100-04
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode (DOCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found.
4, 5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See above.
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data thru the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the $\overline{CRCIZ}$ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on $\overline{DIN}$ (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The WD1100-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and $\overline{CRCOK}$ lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and a pseudo $\overline{DOCK}$ is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flop to gate input data to the output line $\overline{DOUT}$ (pin 11). As shown in the block diagram the $\overline{CWE}$ (pin 6) will be set high. Sometime between the next to the last and the last $\overline{DOCK}$ that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line $\overline{DOUT}$ (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, $\overline{DOUT}$ will produce a string of zeros (i.e., held high). This portion of the circuitry is dormant in the read mode.

After proper initialization, input data is entered on $\overline{DIN}$ (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the complimentary output (pin 16) is set low. These output states will be maintained as long as $\overline{DIN}$ is held high and $\overline{CRCIZ}$ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a re-try is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

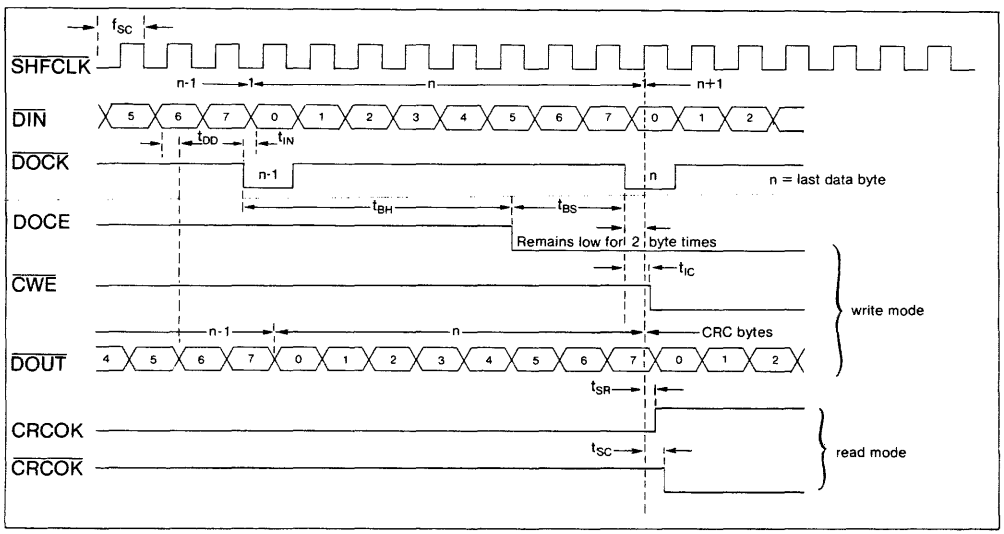
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

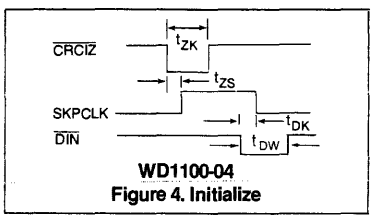
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WT}	↑WCLK to ↓TIMCLK			95	nsec	
t_{WR}	↑WCLK to ↑TIMCLK			85	nsec	
t_{ZS}	↓$\overline{CRCIZ}$ to ↑SKPCLK			120	nsec	
t_{ZK}	$\overline{CRCIZ}$ pulse width	90			nsec	
t_{BS}	DOCE set up time w.r.t. ↓$\overline{DOCK}$	20			nsec	
t_{BH}	DOCE hold time w.r.t. ↓$\overline{DOCK}$	40			nsec	
t_{DD}	$\overline{DIN}$ to $\overline{DOUT}$ delay			105	nsec	CWE set high

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DK}	↓$\overline{DIN}$ to ↓ SKPCLK			120	nsec	
t_{DW}	$\overline{DIN}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓ $\overline{DOCK}$ to ↓ $\overline{CWE}$			120	nsec	
t_{BC}	↓ $\overline{DOCK}$ to ↑ $\overline{CWE}$			120	nsec	
f_{SC}	$\overline{SHFCLK}$ frequency			5.25	MHZ	
t_{SR}	↑ $\overline{SHFCLK}$ to ↑ CRCOK			85	nsec	
t_{SC}	↑ $\overline{SHFCLK}$ to ↓ $\overline{CRCOK}$			90	nsec	
t_{IN}	↓ $\overline{DOCK}$ to ↓ $\overline{DIN}$			90	nsec	

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-04
Figure 3. Write Mode



WD1100-04
Figure 4. Initialize

See page 481 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-05 Parallel/Serial Converter

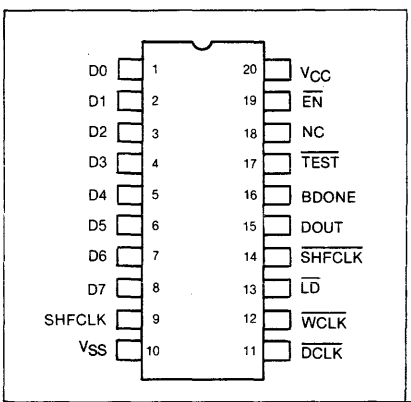
DESCRIPTION

The WD 1100-05 Parallel/Serial Converter allows the user to convert a byte of data to a serial stream when writing to a disk or any serial device. Parallel data is entered via the D0-D7 lines on the rising edge of $\overline{DCLK}$. A synchronous BYTE counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.

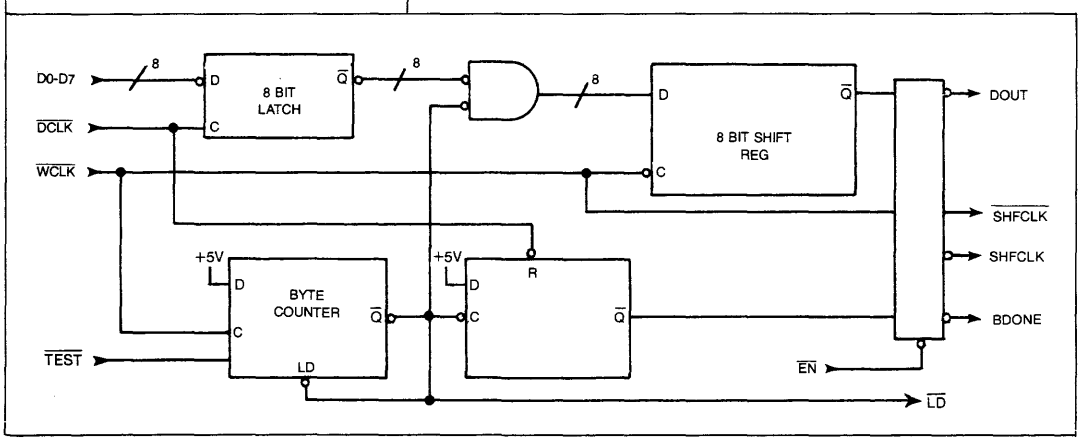
The WD1100-05 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE + 5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5 M BITS/SEC SHIFT RATE
- TRI-STATE OUTPUT CONTROL
- PARALLEL IN/SERIAL OUT
- 20 PIN DIP PACKAGE



WD1100-05
Figure 1. Pin Connections



WD1100-05
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8 bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (module 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 ± 10% power supply input.

DEVICE DESCRIPTION

Prior to loading the WD1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{\text{DCLK}}$ (pin 11). $\overline{\text{DCLK}}$ also resets BDONE (pin 16). The first BDONE that comes up simply means that the WD1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th WRITE CLOCK pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the WD1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low (↓) transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high (↑) transition of $\overline{\text{WCLK}}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 $\overline{\text{WCLK}}$ cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, $\overline{\text{SHFCLK}}$, and SHFCLK, can be placed in a high impedance state by setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'ed with the counter output to produce the $\overline{\text{LD}}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation. . . . . 1 Watt
STORAGE TEMPERATURE
PLASTIC. . . . . −55°C to +125°C
CERAMICS. . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions s 3 .ed in the DC electrical characteristics.

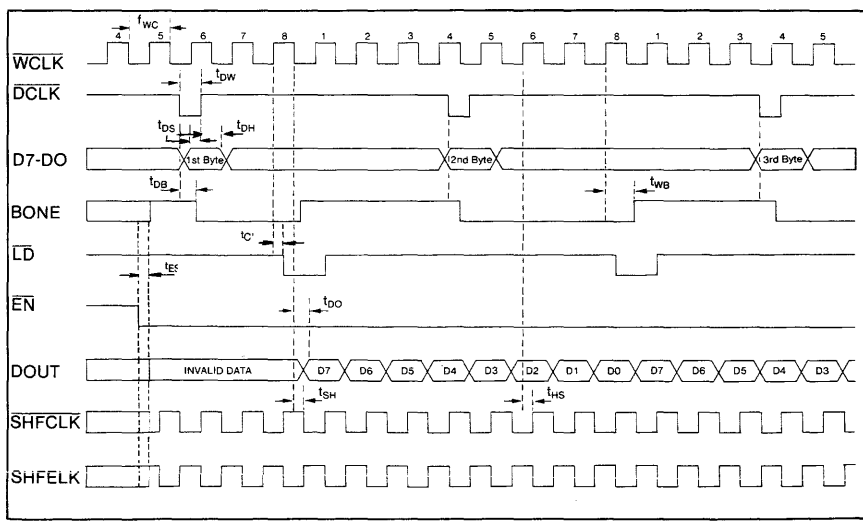
DC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{OH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5 ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK frequency			5.25	MHZ	
t_{DW}	DCLK pulse width	50			nsec	
t_{DS}	Data set-up w.r.t. ↑ DCLK	30			nsec	
t_{DH}	Data hold time w.r.t. ↑ DCLK	30			nsec	
t_{DB}	↓ DCLK to ↓ BDONE			130	nsec	EN = 0
t_{DO}	↓ WCLK to DOUT			130	nsec	EN = 0
t_{SH}	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
t_{HS}	↑ WCLK to ↑ SHFCLK			70	nsec	EN = 0
t_{WB}	↑ WCLK to ↑ BDONE	75		180	nsec	
t_{ES}	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			25	nsec	
t_{CL}	↑ $\overline{WCLK}$ to ↓ $\overline{LD}$			50	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-05
Figure 3. Functional Timing Diagram

See page 481 for ordering information.

Printed in U.S.A.

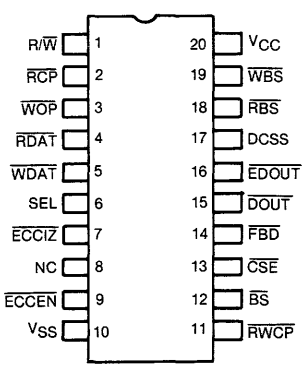
Western Digital
WD1100-06 ECC/CRC Logic

DESCRIPTION

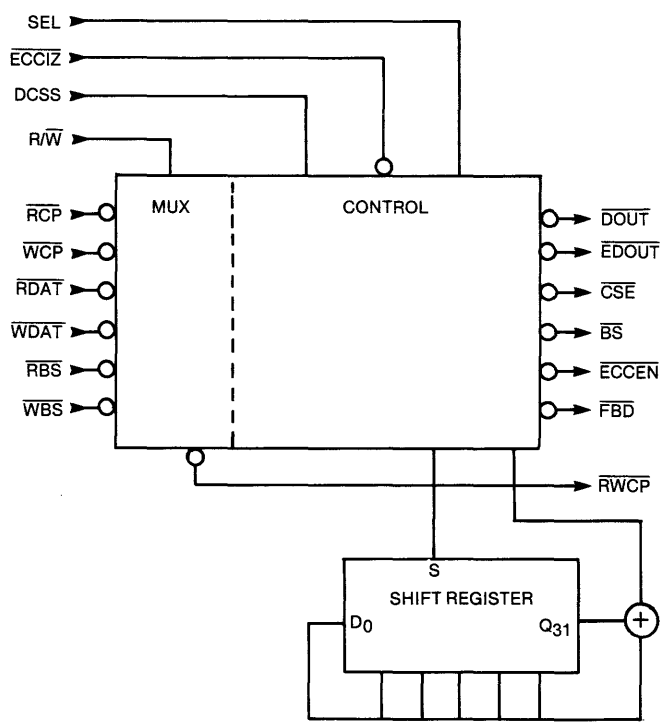
The WD1100-06 ECC/CRC logic chip gives the user of the WD1100 series of chips easy ECC or CRC implementation. With proper software, it will provide single burst correction up to 8 bits and double burst detection. The computer selected polynomial has been optimized for Winchester 5¼" and 8" drives with sector sizes up to 512 bytes.

FEATURES

- 32 bit computer selected polynomial
- Single burst correction up to 8 bits
- Multiple burst detection
- Programmable correction/detection span
- CRC or ECC software selectable
- Data transfer rates to 5.25 Mbits/sec
- Serial check/syndrome bit processing
- 128, 256, 512 byte sector sizes
- Single +5V supply
- TTL, MOS compatible
- 20 pin DIP package



WD1100-06 Figure 1.
PIN CONNECTIONS



WD1100-06 Figure 2.
BLOCK DIAGRAM

WD1100-06 ECC/CRC DEVICE PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ/WRITE	R/$\overline{W}$	Input line used to select the data, clock and CRC/ECC strobe during read/write operations. When low input signals $\overline{WDAT}$, $\overline{WCP}$, and $\overline{WBS}$ are selected. When high input signals $\overline{RDAT}$, $\overline{RCP}$, and $\overline{RBS}$ are selected.
2	$\overline{\text{READ CLOCK PULSE}}$	$\overline{RCP}$	Input pulse used by the internal shift registers to compute the 4 syndrome bytes.
3	$\overline{\text{WRITE CLOCK PULSE}}$	$\overline{WCP}$	Input pulse used by the internal shift registers to compute the 4 check bytes.
4	$\overline{\text{READ DATA}}$	$\overline{RDAT}$	Serial data input during a read operation.
5	$\overline{\text{WRITE DATA}}$	$\overline{WDAT}$	Serial data input during a write operation.
6	SELECT	SEL	This input is used to select either the CRC or the ECC polynomial for error detection/correction. SEL = 0 ECC polynomial selected. SEL = 1 CRC polynomial selected.
7	$\overline{\text{ECC INITIALIZE}}$	$\overline{ECCIZ}$	Input used to preset all the internal shift registers. Output lines $\overline{FBD}$, $\overline{EDOUT}$, $\overline{DOUT}$, and $\overline{CSE}$ will be in their inactive high states. The first low going edge of either $\overline{RDAT}$ or $\overline{WDAT}$ signals the activation of all internal circuitry.
8	NO CONNECTION	N/C	No connection.
9	$\overline{\text{ECC ENABLE}}$	$\overline{ECCEN}$	When low, the ECC/CRC process is enabled. When high, this output signal indicates that the process is disabled.
10	GROUND	V_{SS}	Ground
11	$\overline{\text{READ/WRITE CLOCK PULSE}}$	$\overline{RWCP}$	Output clock pulse during read or write operations. The input clock pulses $\overline{RCP}$ and $\overline{WCP}$ are multiplexed on this output line for use by any support logic.
12	$\overline{\text{BYTE SYNC}}$	$\overline{BS}$	The input signals $\overline{RBS}$ and $\overline{WBS}$ are gated with the appropriate clocks and multiplexed as an output on the byte sync line. Normally not used by the user.
13	$\overline{\text{CLOCK SELECT ENABLE}}$	$\overline{CSE}$	When high, this output indicates that the device is in the process of computing the check/syndrome bytes and that $\overline{EDOUT}$ and $\overline{DOUT}$ lines contain data information. When low, the device puts CRC or ECC check/syndrome bits on the output data lines.
14	$\overline{\text{FEEDBACK}}$	$\overline{FBD}$	The feedback line to the shift registers is brought out as an output line for test purposes. Normally left open by the user.
15	$\overline{\text{DATA OUTPUT}}$	$\overline{DOUT}$	Output data line carries data or CRC/ECC information depending upon the state of DCSS.
16	$\overline{\text{EARLY DATA OUTPUT}}$	$\overline{EDOUT}$	Unlatched output data line available 1 clock period earlier than $\overline{DOUT}$.

WD1100-06 ECC/CRC PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	DATA/CHECK SYNDROME SELECT	DCSS	Data or check/syndrome select input line. When high, data is output on the data lines; when low, CRC or check syndrome bits are output depending upon which polynomial is selected. DCSS goes low sometime between the last and the next to the last data byte transferred to/from the disk provided all set-up and hold-times have been met. DCSS must stay low for at least 2 byte times when the CRC polynomial selected and it must stay low for at least 4 byte times if the ECC polynomial is selected.
18	$\overline{\text{READ BYTE}}$	$\overline{\text{RBS}}$	Input used to latch the state of DCSS during the read mode.
19	$\overline{\text{WRITE BYTE}}$	$\overline{\text{WBS}}$	Input used to latch the state of DCSS during the write mode.
20	+5V	V_{CC}	+5V ±10%

DEVICE DESCRIPTION

To ensure correct operation of the WD1100-06 device, the $\overline{\text{ECCIZ}}$ line is strobed to preset the polynomial generator shift register, and reset the Data/Check-Syndrome select flip-flop. The 32 bit shift register string is preset to avoid all zero check bytes. The DCSS line is held high and appropriate signals are then applied to the rest of the inputs. Since most disk media use an Address mark of A1 (or M.S.B. set), advantage is taken of this feature to start off the ECC/CRC calculation on the data/ID fields automatically. The first active low going edge on the input data lines releases the internal SET Flip-Flop. The $\overline{\text{ECCEN}}$ output line is set low indicating that the internal circuitry is ready to begin the computation of the ECC/CRC bytes. Immediately following the Address mark, data is supplied in a serial fashion.

Sometime before the last byte of data and after the next to the last byte of data is transferred through this device, the DCSS line is set low. Since data is generally serialized/deserialized before/after processing by the WD1100-06 device, the byte-sync pulses can be easily obtained from those devices marking the byte boundaries. The byte-sync pulses are internally ANDED with the $\overline{\text{RWCP}}$ line to ensure the smooth transition of check/syndrome bytes on the $\overline{\text{DOUT}}$ output line only after the last bit of data has been entered into the device. A one bit time delay through a D Flip-Flop has been added on the $\overline{\text{DOUT}}$ line to deglitch this output line.

During a WRITE operation, the input data stream is divided by the polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^2 + 1$ and the 32 bit remainder obtained is used as the 4 check syndrome bytes. If the syndrome is zero, no errors occurred. Otherwise, the non-zero syndrome is used by a software algorithm to compute the displacement and the error vector within the bad sector. To protect the integrity of the ID field only a CRC check should be performed over this field. No attempt ought to be made to correct data in the ID field. The CRC polynomial implemented is the standard CCITT ($X^{16} + X^{12} + X^5 + 1$.) Although either polynomial may be used for both fields, the use of the CRC polynomial for the ID fields is recommended since it only requires 2 bytes instead of 4.

POLYNOMIAL SELECTION

For disk media, polynomial selection has a significant influence on data accuracy. Fire code polynomials have been widely used on OEM disk controllers, but provide less accuracy than properly selected computer generated codes.

For fixed, guaranteed correction and detection spans, data accuracy may be highly dependent on polynomial selection. Some polynomials, fire codes for example, are particularly susceptible to miscorrection on common disk type errors, while others, computer generated polynomials for example, can be selected to be less susceptible. Computer generated codes do not have the pattern sensitivity of the fire code and the miscorrection patterns are more random in nature.

More than 20,000 computer generated random polynomials of degree 32, each with 8 feedback terms, were evaluated in order to find the polynomial described in this specification.

SELECTING THE CORRECTION SPAN

The code described in this document can be used to correct up to 8 bits.

Any correction span from 1 to 8 may be selected. However, for best data accuracy, the lowest correction span should be used that meets the correction

requirements for the disk drives supported.

For most Winchester media, a 5 bit correction span is adequate.

The correction span may have to be longer if the drive uses a read/write modulation method that maps a single media bit in error into several decoded bits in error. Examples of read/write modulation methods of this type would be GCR and 2,7 code.

PROPERTIES OF THE POLYNOMIAL

The following polynomial was computer selected for insensitivity to short double bursts, good detection span and 8 feedback terms.

Forward polynomial is:
$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 0$

Reciprocal polynomial is:
$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + x^{13} + X^6 + X^4 + X^0$

Properties*

1. Maximum record length (r) = 526x8 bits (including check bits)
2. Maximum correction span (b) = 8 bits
3. Degree of polynomial (m) = 32
4. Single burst detection span without correction = 32 bits. (Detection span when the code is used for detection only)
5. Single burst detection span with correction (d) — (Detection span when the code is used for correction)
   - = 19 bits for b = 5 and r = 526x8
   - = 14 bits for b = 8 and r = 526x8
   - = 20 bits for b = 5 and r = 270x8
   - = 14 bits for b = 8 and r + 270x8
6. Double burst detection span without correction — (Doule burst detection span when code is used for correction)
   - = 3 bits for b = 5 and r = 526x8
   - = 2 bits for b = 8 and r = 526x8
   - = 4 bits for b = 5 and r = 270x8
   - = 2 bits for b = 8 and r = 270x8
7. Non-detection probability = 2.3 E-10.
8. Miscorrection probability—
   - = 1.57 E-5 for b = 5 and r = 526x8
   - = 1.25 E-4 for b = 8 and r = 526x8
   - = 8.00 E-6 for b = 5 and r = 270x8
   - = 6.40 E-5 for b = 8 and r = 270x8

NOTE:*
You should not use this polynomial for a record length or correction span beyond the maximum specified above.

SOFTWARE REQUIREMENTS

The software algorithm, developed by the user, uses the syndrome to detect an error, generate a correction pattern and a displacement vector or to determine if uncorrectable. In the correction algorithm, a simulated shift register is used to implement the reciprocal polynomial. The simulated shift register is loaded with the syndrome and shifted until a correctable pattern is found or the error is determined to be uncorrectable. Both forward and reverse displacements are computed.

Either the serial or the parallel algorithm may be implemented by the user. In almost all cases the serial software algorithm is the most applicable. Additionally, 1K of table space is required if the parallel software algorithm is selected. It is assumed that the highest order bit of a byte is serialized and deserialized first.

CORRECTION TIME PERFORMANCE

All real time operations are performed with error correction hardware. The software algorithms used get involved only after an error has been detected.

The following correction times are for a serial type algorithm such as that used on the WD1001:

a) Standard microprocessor = 30 to 60 milliseconds
b) Bit slice = 6 to 12 milliseconds
c) 8X300 (used on WD1001) = 15 to 30 milliseconds

DATA ACCURACY

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be re-read before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected erroneous data by rereading until the error goes away, or until there has been a consistant error syndrome over two previous rereads.

Another technique that can be used to give data a higher probability of recovery is write check: read back after write. Since write check affects performance, it should be optional. Alternate sector assignment and defect skipping are some of the other techniques that may be implemented by the user if so desired.

SELF-CHECKING WITH MICROCODE

Periodic microcode and/or software checking is another approach that can be used to limit the amount of undetected erroneous data transferred in case of an ECC circuit failure. Microcode or software diagnostics could be run on subsystem power up and during idle times. These diagnostics would force ECC errors and check for the proper syndrome and proper decoding of the syndrome by the correction routine of the operational microcode.

To do this, simply use a long bit in the READ and WRITE commands to the disk. This bit can then be used to suppress the transfer of check/syndrome bytes on the output data line by letting the DCSS line stay high during ECC TIME. The complete procedure is summarized below.

1. WRITE: Pass all data to the disk and generate 4 check bytes at the end of the data field.
2. READLONG: Do not generate the syndrome, instead copy the 4 check bytes as data and pass them unaltered to the host. Now the host may induce errors anywhere in the data stream as long as the induced error does not exceed the correction span of the polynomial generator.
3. WRITELONG: Write the data and check bytes supplied by the host to the disk. Prevent WD1100-06 from generating check bits by not asserting DCSS during transfer. No check bytes will be recorded.
4. READ: Read data and generate the syndrome in a normal manner. The software algorithm can now be invoked to correct the induced error.

To aid in detection of certain hardware failures, it is desirable to have non-zero check bytes for an all zeros record. This feature has been incorporated into the circuit defined in this specification.

SPECIFICATIONS

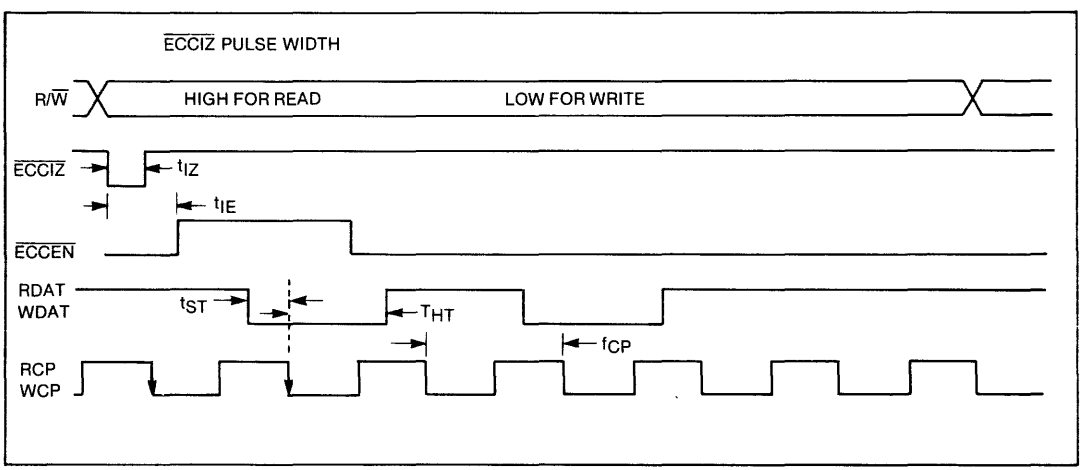
ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2V to +7.0V
Power dissipation ..... 1 Watt
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −55°C to +150°C

NOTE:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		75	150	mA	All outputs open



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS}

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{CP}	Clock Frequency			5.25	MHZ	
t_{IZ}	ECCIZ Pulse Width	50			nSec	
t_{IE}	ECCIZ ↓ to ECCEN ↑			100	nSec	
t_{ST}	R/WDAT Setup Time	50		1 Clock Period	nSec	
t_{HT}	R/WDAT Hold Time	0			nSec	

See page 481 for ordering information.

PRELIMINARY

WD1100-07

Western Digital
WD1100-07 Host Interface Logic

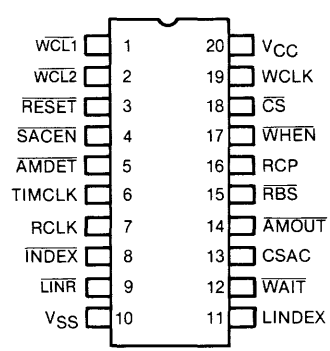
DESCRIPTION

The WD1100-07 Host Interface Logic chip simplifies the design of a Winchester Hard Disk Controller using the WD1100 chip series. It does this by performing logic functions that would otherwise require considerable discrete logic. Additionally, there are signals provided for ECC implementation.

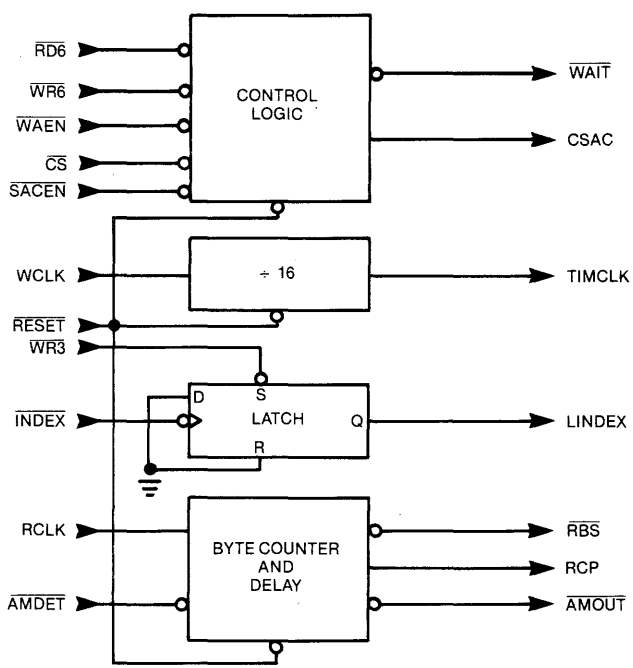
The WD1100-07 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic Dual-in-Line package.

FEATURES

- SINGLE +5V SUPPLY
- WAIT SIGNAL GENERATION
- TIMING CLOCK GENERATION
- INDEX PROPAGATION
- CARD ACCESS CONTROL
- COMPLIMENTS ECC ARCHITECTURE
- 20 PIN DIP PACKAGE



WD1100-07 Figure 1.
PIN CONNECTIONS



WD1100-07 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAIT CLEAR 1	$\overline{WCL1}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
2	WAIT CLEAR 2	$\overline{WCL2}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
3	RESET	$\overline{RESET}$	An input used to set TIMCLK & reset $\overline{WAIT}$, $\overline{AMOUT}$ and $\overline{RBS}$.
4	SELECT ADDRESS ENABLE	$\overline{SACEN}$	This is an input signal that is used to enable card select for host access.
5	ADDRESS MARK DETECT	$\overline{AMDET}$	An input that must go active when a DATA = A1(HEX) or clock = 0A(HEX) pattern is detected in the data stream
6	TIMING CLOCK	TIMCLK	An output used to provide reference timing signals to SA100 type drives
7	READ CLOCK	RCLK	This input, the same as used to clock in data and clocks to the AM detector, is used to produce $\overline{AMOUT}$.
8	INDEX PULSE	$\overline{INDEX}$	This input is provided by the drive once each revolution of the disk
9	LINDEX RESET	$\overline{LINR}$	An input used to reset LINDEX.
10	GROUND	V_{SS}	Ground
11	LATCHED INDEX	LINDEX	An output that is $\overline{INDEX}$ delayed by one clock time.
12	WAIT	$\overline{WAIT}$	This output goes true when controller is internally accessing data or has not accepted data from the host during a WRITE.
13	CARD SELECT ADDRESS	CSAC	An output that is the result of $\overline{CS}$ qualified with $\overline{SACEN}$.
14	ADDRESS MARK DELAYED OUTPUT	$\overline{AMOUT}$	This output is a delayed version of $\overline{AMDET}$.
15	READ BYTE STROBE	$\overline{RBS}$	This output strobes once for each byte of READ data. Initialized by $\overline{AMDET}$.
16	READ CLOCK PULSE	RCP	This output is delayed from RCLK through propagation. Not normally used.
17	WAIT ENABLE	$\overline{WAEN}$	An input that is used to enable the internal WAIT circuitry.
18	CARD SELECT	$\overline{CS}$	An input from host that selects controller.
19	WRITE CLOCK	WCLK	This input is used to produce TIMCLK on low to high transitions.
20	+5VDC	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

Upon power up or reset, $\overline{WAIT}$, $\overline{AMOUT}$, and $\overline{RBS}$ are reset and TIMCLK is set. This is the only interactive signal between the four sections of the chip. Each section will be described separately.

Control Logic

This section provides $\overline{WAIT}$ (pin 12) and CSAC (pin 13). $\overline{WAIT}$ is set in its active low state when $\overline{WAEN}$ (pin 17) is active low by the falling edge of $\overline{CS}$ (pin 18). $\overline{WAIT}$ is reset by the falling edge of either $\overline{WCL1}$ or $\overline{WCL2}$ depending on whether in a read or write mode. CSAC (pin 13) is enabled by setting $\overline{SACEN}$ (pin 4) low after $\overline{WAIT}$ has been enabled. CSAC is reset by $\overline{WCL1}$ or $\overline{WCL2}$.

Timing Clock

TIMCLK (pin 6) is a divided by sixteen version of WCLK (pin 19). It is used with SA1000 type drives.

Index Pulse

Lindex (pin 11) is a delayed version of $\overline{INDEX}$ (pin 8). It remains high until reset by $\overline{LINR}$ (pin 9).

Read Byte Sync

$\overline{RBS}$ (pin 15) will go true on the eighth negative going transition of RCLK (pin 7) after $\overline{AMDET}$ (pin 5) goes true. $\overline{RBS}$ will remain true for one clock cycle.

Read Clock Pulse

RCP (pin 16) is a delayed version of RCLK and is normally left open by the user.

Address Mark Delayed Output

$\overline{AMOUT}$ (pin 14) is the same as $\overline{AMDET}$ delayed by two clock times.

These circuits were developed to work with the other chips in the WD1100 series. They are used on the WD1001 the timing relationships must be observed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ..... −0.2V to +7.0V
Power Dissipation ..... 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

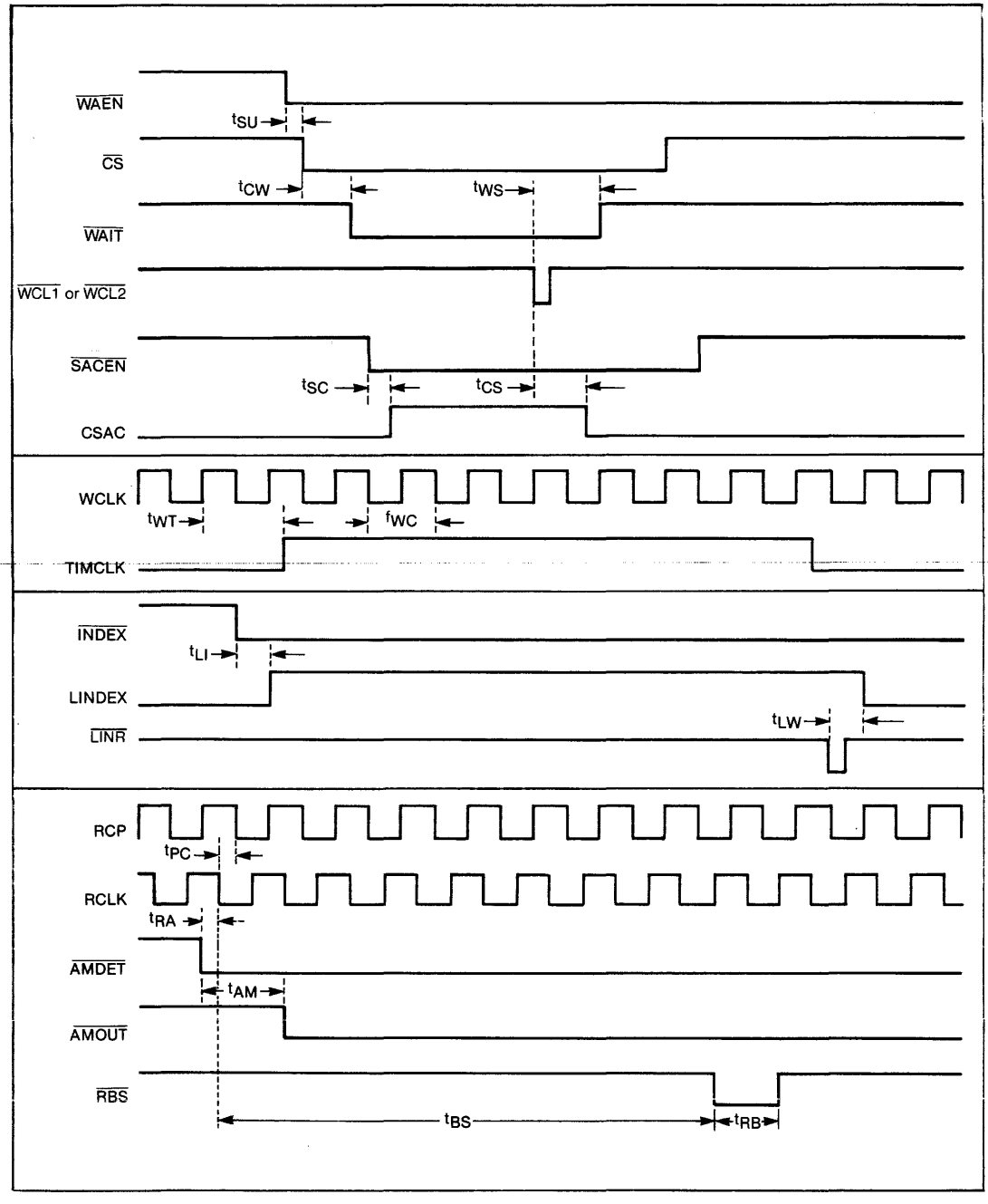
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{CW}	$\overline{CS}$↓ to $\overline{WAIT}$↓		50	160	nSec	
t_{WS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ to $\overline{WAIT}$↑		170	195	nSec	
t_{SU}	$\overline{WAEN}$ Setup Time	50			nSec	
t_{SC}	$\overline{SACEN}$↓ to CSAC↑		5	70	nSec	$\overline{WAIT}$ TRUE
t_{CS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ to CSAC↓		45	155	nSec	$\overline{WAIT}$ TRUE
t_{WT}	WCLK↑ to TIMCLK↑			250	nSec	
t_{LI}	$\overline{INDEX}$↓ to LINDEX↑		50	100	nSec	
t_{LW}	$\overline{LINR}$↓ to LINDEX↓		30	100	nSec	
t_{PC}	RCLK↓ to RCP↓		30	75	nSec	
t_{RA}	$\overline{AMDET}$ Setup Time	30	50		nSec	
t_{AM}	$\overline{AMDET}$↓ to $\overline{AMOUT}$↓		2 CLOCK CYCLES	2 CLOCK CYCLES +45	nSec	
t_{BS}	RCLK↓ to $\overline{RBS}$↓		8 CLOCK CYCLES	8 CLOCK CYCLES +165	nSec	
t_{RB}	$\overline{RBS}$ Period		1 CLOCK CYCLE			

[1] NOTE: Typical Values are for T_A = 25°C and V_{CC} = +5V



See page 481 for ordering information.

Western Digital
WD1100-09 Data Separator Support Logic

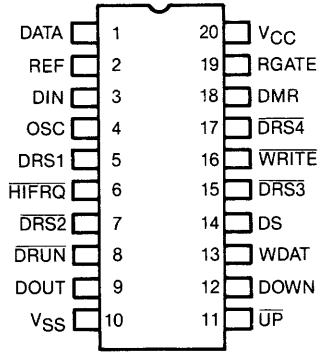
GENERAL DESCRIPTION

The WD1100-09 Data Separator Support Logic, when used with the other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester hard disk data separator. The chip provides the pump signals to an external error amplifier, control signals to an internal bus and a special drive selection signal also to an internal bus.

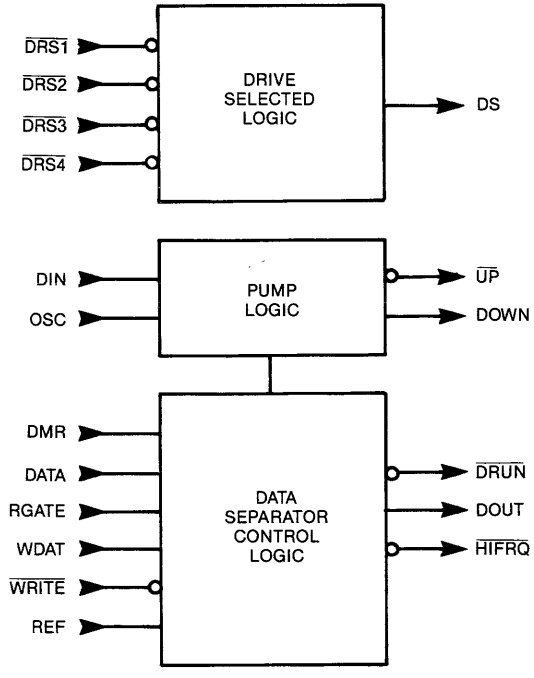
The WD1100-09 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic package.

FEATURES

- SINGLE +5V SUPPLY
- DRUN GENERATION
- DATA SEPARATION CONTROL SIGNALS
- 20 PIN DIP PACKAGE



WD1100-09 Figure 1.
PIN CONNECTIONS



WD1100-09 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ DATA	DATA	Input that is used in $\overline{\text{DRUN}}$ generation.
2	REFERENCE	REF	An input that is 2 times the data rate that keeps the VCO on center frequency during non-read times.
3	DELAYED DATA IN	DIN	This input is a delayed version of DOUT. An external delay line is used. The signals are compared to provide pumps.
4	OSCILLATOR	OSC	An input from the external VCO that is used in pump development
5, 7, 15, 17	$\overline{\text{DRIVE SELECT}}$ 1- $\overline{\text{DRIVE SELECT}}$ 4	$\overline{\text{DRS1}}$- $\overline{\text{DRS4}}$	Input signals indicating which drive has been selected.
6	$\overline{\text{HIGH FREQUENCY}}$	$\overline{\text{HIFRQ}}$	Output to controller microprocessor that indicates 16 ones or zeros have been entered on the DATA line.
8	$\overline{\text{DATA RUNNING}}$	$\overline{\text{DRUN}}$	Output that indicates to the controller microprocessor the completion of 16 ones or zeros on the data line. Used to switch from REF to DATA via firmware.
9	DATA OUT	DOUT	Output data line. Can be REF or DATA or WDATA depending on the condition of $\overline{\text{WRITE}}$, $\overline{\text{DMR}}$ and RGATE.
10	GROUND	V_{SS}	Ground
11	$\overline{\text{UP PUMP}}$	$\overline{\text{UP}}$	An output that indicates REF is leading DATA. Goes to error amp. Open collector.
12	DOWN PUMP	DOWN	An output that indicates DATA is leading REF. Goes to error amp. Open collector.
13	WRITE DATA	WDATA	MFM Write data input. Output appears at DOUT.
14	DRIVE SELECTED	DS	An output that indicates that one of four drives have been selected.
16	$\overline{\text{WRITE MODE}}$	$\overline{\text{WRITE}}$	This input is active during a write operation and enables WDAT.
18	DATA MASTER RESET	DMR	This input is used to provide time-out for $\overline{\text{DRUN}}$ and $\overline{\text{HIFRQ}}$ in the event that 16 ones or zeros are not present.
19	READ GATE	RGATE	This input, usually provided by the controller microprocessor, places chip in read mode.
20	+5VDC	V_{CC}	+5VDC ± 10%

DEVICE DESCRIPTION

The WD1100-09 is divided into three sections. Each section will be described separately.

Drive Select Logic

DS (pin 14) will go active high if any input $\overline{\text{DSR1}}$ through $\overline{\text{DRS4}}$ (pins 5, 7, 15, 17) are active low.

Pump Logic

Internal logic causes the $\overline{\text{UP}}$ (pin 11) and the DOWN (pin 12) to be set, initially to their inactive states. DIN (pin 3) is the delayed data developed by passing DOUT through a delay line. OSC (pin 4) is the output of the data separator VCO. Whichever reaches the pump logic first will determine whether UP PUMP or DOWN PUMP is produced. These signals are then sent to an external error amplifier and used for VCO correction. During a write, the DIN must be locked to a crystal oscillator clock and will hold the VCO on frequency.

Data Separator Control Logic

Read Mode

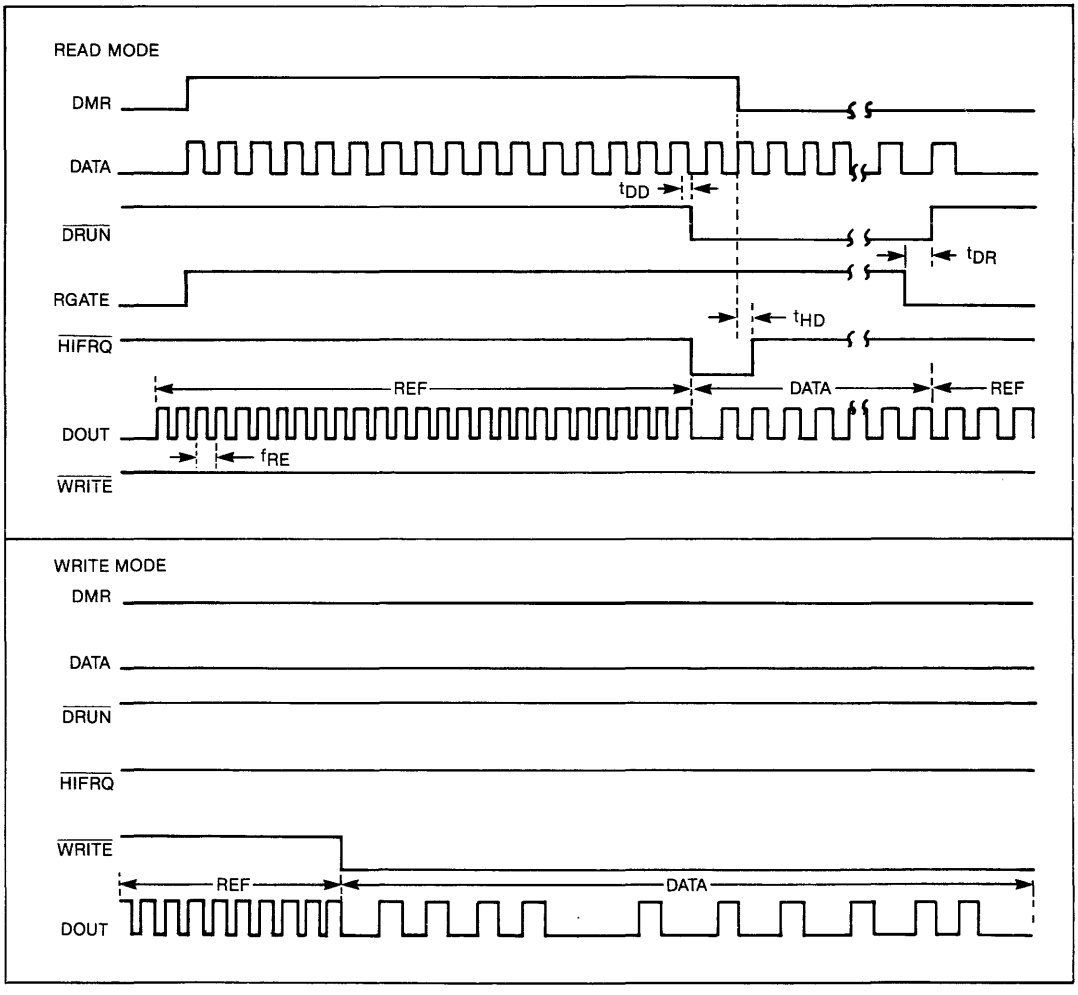
In order to prevent the external VCO from locking onto a harmonic of its operating frequency, REF (pin 2) is provided with a signal twice the data rate that is crystal controlled. With $\overline{\text{WRITE}}$ (pin 6) and RGATE (pin 19) inactive, this signal will appear at DOUT (pin 9). This signal is applied to the pump logic (see above).

The switching function is initiated immediately after RGATE goes true. DMR (pin 18) will be set active as a result of high frequency pulses applied to an external one shot whose pulse width is such that its output is a single stretched pulse. The high frequency pulses are applied to the DATA (pin 1) line and after 16 consecutive pulses, $\overline{\text{DRUN}}$ (pin 8) and $\overline{\text{HIFRQ}}$ (pin 6)

go true. At this point REF is switched out and the DATA stream is switched in and appears at DOUT. $\overline{DRUN}$ is reset when RGATE goes inactive and $\overline{HIFRQ}$ goes inactive when DMR goes inactive.

Write Mode

When $\overline{WRITE}$ (pin 16) goes active, REF is switched out and WDAT (pin 13) will appear at DOUT. Since WDAT is a crystal controlled signal (usually the MFM write data); the VCO is held locked and will not drift (see pump logic above).



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DD}	DATA↓ to $\overline{DRUN}$↓			170	nSec	
t_{DR}	RGATE↓ to $\overline{DRUN}$↑			90	nSec	
t_{HD}	DMR↓ to $\overline{HIFRQ}$↑			90	nSec	
f_{RE}	REF frequency		2 TIMES DATA RATE	10	MHz	

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2V to +7.0V
Power Dissipation ..... 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

NOTE: $\overline{UP}$ and DOWN are open collector outputs and provide 12mA I_{OL} @ .5V.

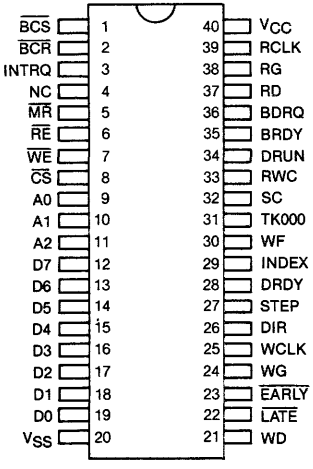
See page 481 for ordering information.

Printed in U.S.A

WD1010-00/01 Winchester Disk Controllers

FEATURES

- ST506/SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY
- AUTOMATIC RETRIES (WD1010-00 ONLY)
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1010 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5¼" and 8" products utilizing the same type of interface. On the host side, an 8 bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010.

Operating from a single 5 volt supply, the WD1010 is implemented in NMOS silicon gate technology and is available in a 40 pin dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
12-19	DATA 7 - DATA 0	D7-D0	Eight bit tristate bidirectional bus used for transfer of commands, status, and data.
6	READ ENABLE	$\overline{RE}$	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	WRITE ENABLE	$\overline{WE}$	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
9-11	ADDRESS 0 - ADDRESS 2	A0-A2	These three inputs select the register to receive/transmit data on D0-D7.
8	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTERRUPT REQUEST	INTRQ	Active high output which is set to a logic high in the completion of any command.
5	MASTER RESET	$\overline{MR}$	A logic low in this input will initialize all internal logic.
1	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing of the external sector buffer.
35	BUFFER READY	BRDY	This rising edge activated input is used to inform the controller that the sector buffer is full or empty.
2	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed by the WD1010 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
36	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the sector buffer.
40	+5 VOLT	V_{CC}	+5V ±5% Power supply input.
20	GROUND	V_{SS}	Ground
4	NO CONNECT	NC	
21	WRITE DATA	WD	This open drain output contains the MFM clock and data pulses to be written on the disk.
25	WRITE CLOCK	WCLK	4.34 or 5.0 Mhz clock input used to derive all internal write timing.
24	WRITE GATE	WG	This output is set to a logic high before writing is to be performed on the disk.
23, 22	EARLY, LATE	$\overline{EARLY}$, $\overline{LATE}$	Precompensation open drain outputs used to delay the WD pulses externally.
37	READ DATA	RD	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	READ CLOCK	RCLK	A nominal square wave clock input derived from the external data recovery circuits.
38	READ GATE	RG	This output is set to a logic high when data is being inspected from the disk.
34	DATA RUN	DRUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
27	STEP PULSE	STEP	This output generates a pulse for stepping the drive motor.
26	DIRECTION	DIR	This output determines the direction of the stepping motor.
28	DRIVE READY	DRDY	This input must be at a logic high in order for commands to execute.
30	WRITE FAULT	WF	An error input to the WD1010 which indicates a fault condition at the drive.

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	TRACK 000	TK000	An input to the WD1010 which indicates positioning over track 000.
29	INDEX PULSE	INDEX	A logic high on this input informs the WD1010 when the index hole has been encountered.
33	REDUCED WRITE CURRENT	RWC	This output can be programmed to reduce write current on a selected starting cylinder.
32	SEEK COMPLETE	SC	This input informs the WD1010 when head settling time has expired.

ARCHITECTURE

The WD1010 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. Two versions of the WD1010 are available. The WD1010-00 has automatic retries on errors. The WD1010-01 terminates the command execution on errors. These differences are noted in the following text and flowcharts. The internal architecture of the WD1010 is shown in Figure 1. Its major functional blocks are:

PLA Controller
The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator
A 10 bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

CRC Logic
Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is X16 + X12 + X5 + 1.

MFM Encode/Decode
Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect
The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = H'A1', Clock = H'0A') used in each ID and data field.

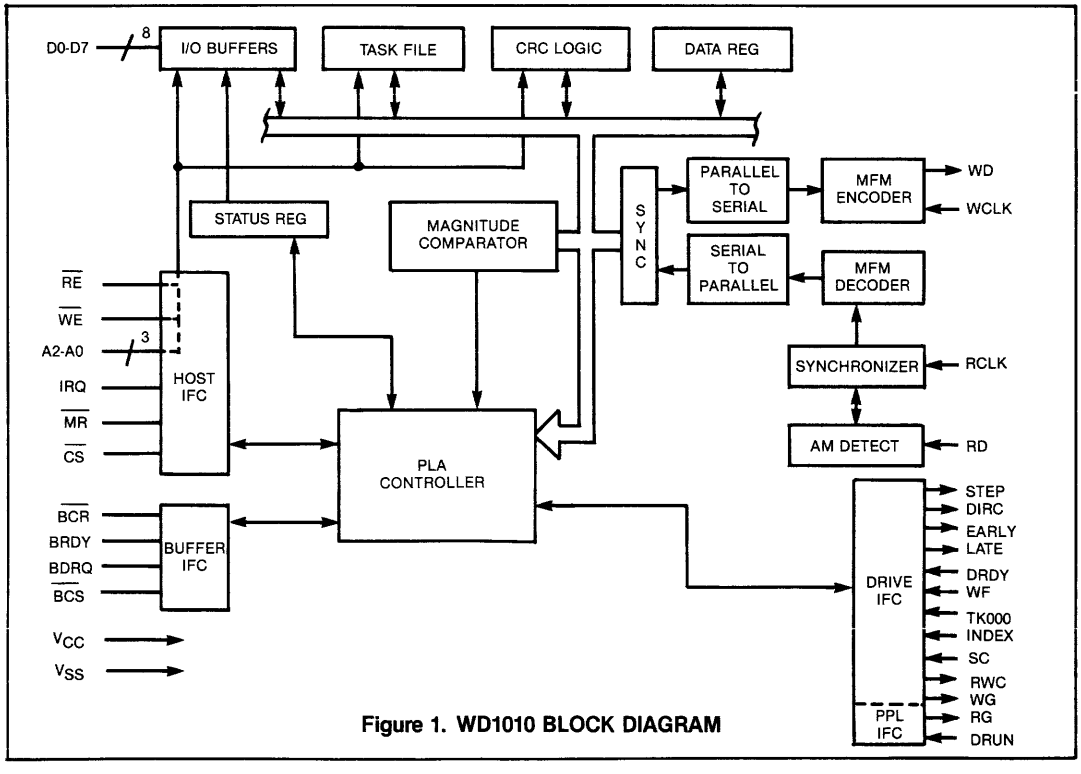


Figure 1. WD1010 BLOCK DIAGRAM

Host/Buffer IFC
This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC
This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010 interacts with the data separator through the DATA RUN (DRUN) and Read Gate (RG) signals. The block diagram of the data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010, the reference multiplexor, and a retriggerable one shot. The read gate (Pin 38) output will be low when the WD1010 is not inspecting data. The PLL at this time should remain locked to the reference clock.

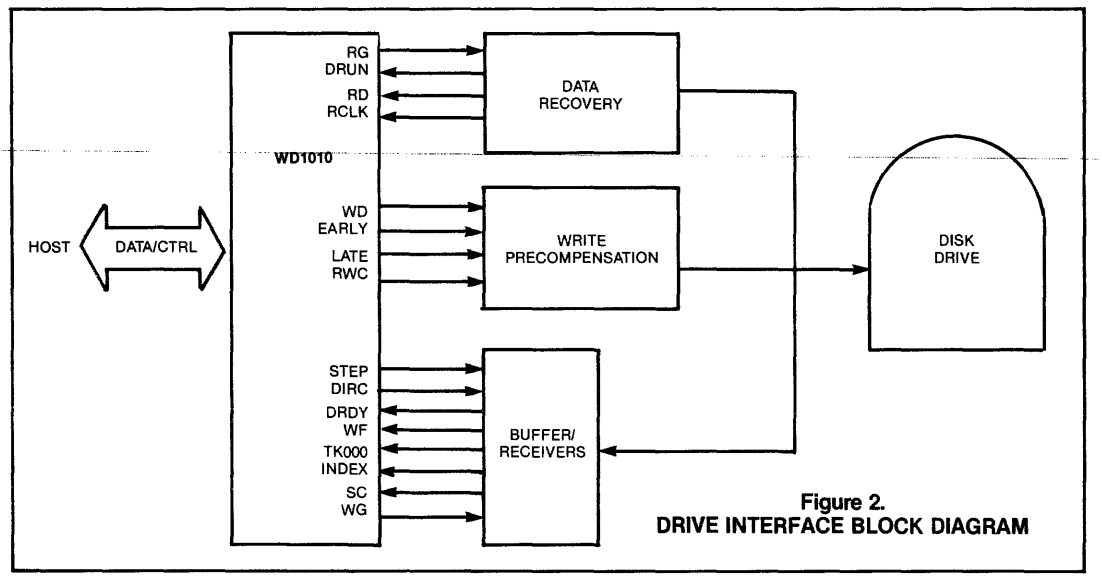


Figure 2.
DRIVE INTERFACE BLOCK DIAGRAM

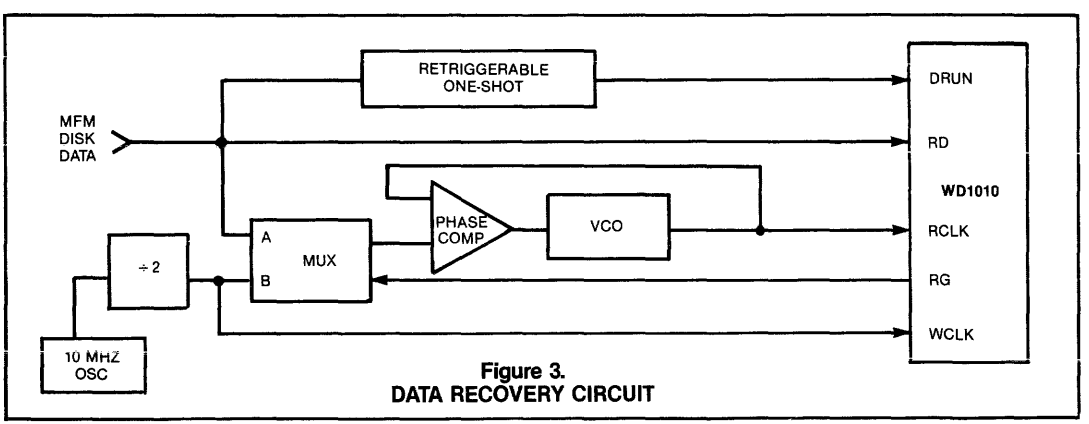


Figure 3.
DATA RECOVERY CIRCUIT

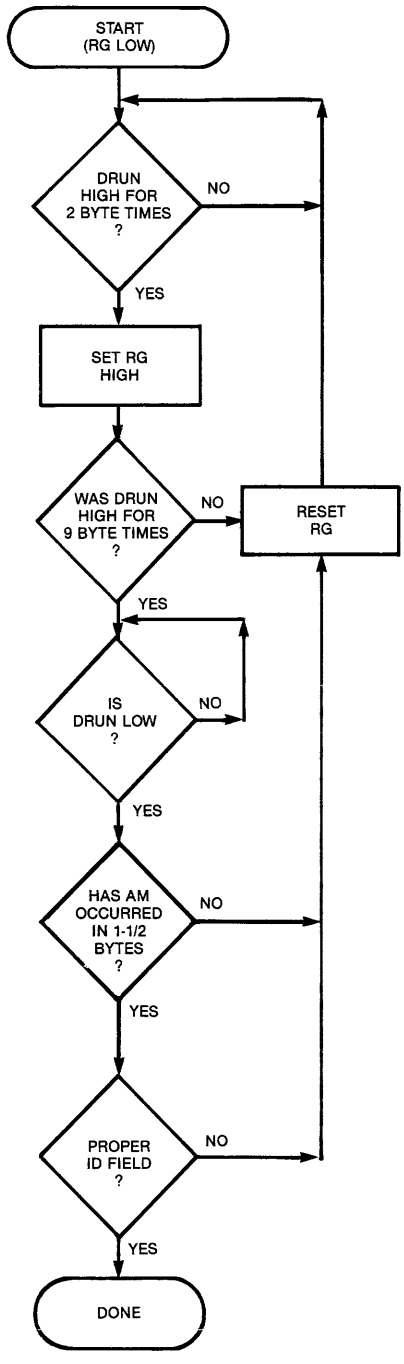


Figure 4.
PLL CONTROL SEQUENCE

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeros. An internal counter times out to see that DRUN is high for 16 bits (2 byte times). Since all address marks are preceded by 12 bytes of zeros, an attempt is made to read an address mark. If DRUN falls prior to 64 bit times, the process is repeated. Read gate is then set by the WD1010, switching the data separator to lock onto the incoming data stream. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals Reduce Write Current (RWC), Early and Late. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder.

The signals $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{Early}}$ occurs after the fact, write data should be delayed one interval when both Early and Late are high; two intervals when Late is low; and no delay when $\overline{\text{Early}}$ is low. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{Early}}$ or $\overline{\text{Late}}$ will be active slightly ahead of the write data pulse; Early and Late will never be low at the same time. Regardless of the contents of the RWC register, $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will always be active.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010 is through an 8-bit bidirectional bus. This bus is used to transmit/receive data to both the WD1010 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory. Whenever the WD1010 is not using the sector buffer, the Buffer Chip Select ($\overline{\text{BCS}}$) is high (disabled). This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_0-A_2 are '000'; an unused address in the WD1010. A binary counter is enabled whenever $\overline{\text{RE}}$ or $\overline{\text{WE}}$ goes active and in-

cremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-$A_2 \neq$ '000'; allowing access to the WD1010's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. It then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the Buffer Ready (BRDY) signal is made active (by the "carry" out of the counter), informing the WD1010 that the buffer is full. (BRDY is a rising edge activated signal.) The Buffer Chip Select ($\overline{BCS}$) is then made active, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010 to allow it access to the buffer. When the WD1010 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar matter, except the buffer is loaded by the WD1010 instead of the host.

Another control signal called Buffer Data Request (BDRQ; not used in Figure 5) is a DMA signal that can inform a direct memory access controller when the WD1010 is requesting data. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command, interrupts are generated at the termination of a command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The interrupt line (INTRQ) is cleared either by reading the status register or by writing a new command in the command register.

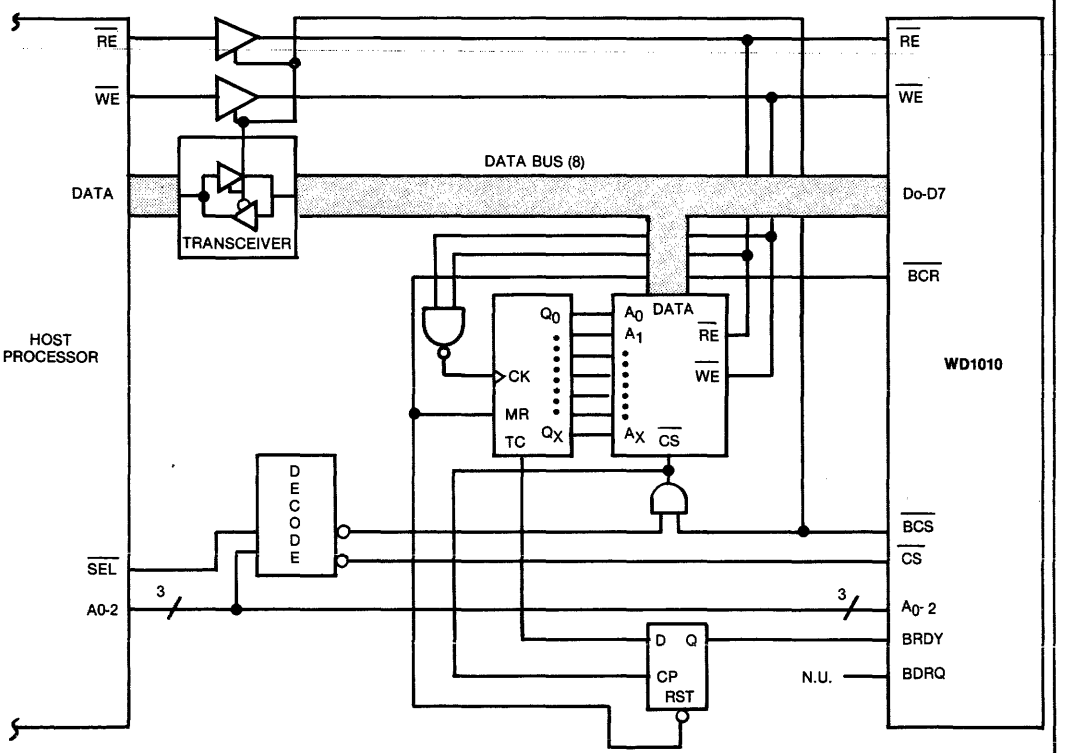


Figure 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addreses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are **not** cleared by master reset ($\overline{MR}$).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a data field CRC error has occurred or the Data Address Mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 — Reserved
Not used; forced to a zero.

Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY (Pin 28) line is low or the WF (30) line is low. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — TK000 Error
This bit is set only by the restore command. It indictes that the TK000 (Pin 31) line has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC (Pin 33) line is asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of H'01' will cause RWC to activate on cylinder 4; H'02' on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . 1020. The RWC will be asserted when the present cylinder is equal to a greater than the value in this register. For example, the ST506 requires precomp on cylinder 128 (H'80') and above. Therefore, the write precomp cylinder register should be loaded with 32 (H'20').

SECTOR COUNT

This register holds the number of sectors that are needed to be transferred to the buffer:

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant 8 bits of the desired cylinder number:

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:

7	6	5	4	3	2	1	0
EXT	SIZE		DRIVE		HEAD		

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a formatting command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE		0	0	HEAD #		
7	6	5	4	3	2	1	0

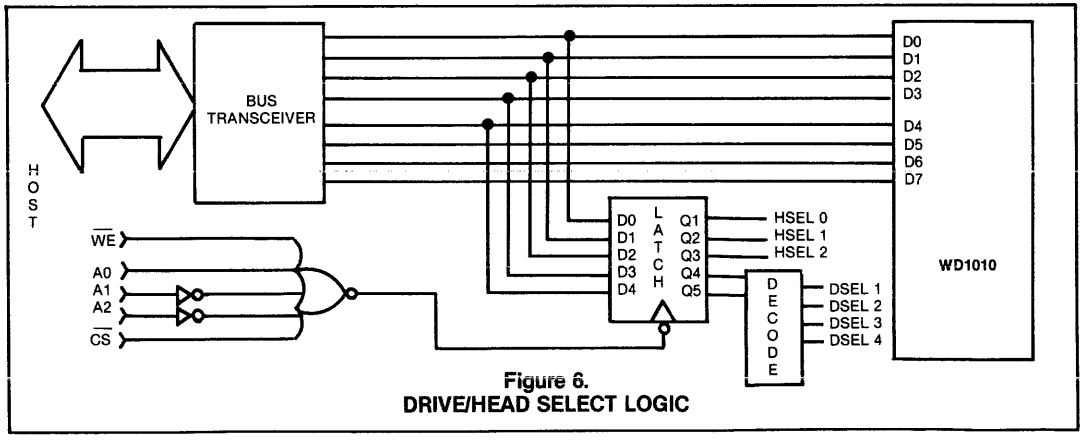


Figure 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7 — Busy
This bit is set whenever the WD1010 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled.

Bit 6 — Ready
This pin normally reflects the state of the DRDY (Pin 28) line.

Bit 5 — Write Fault
This bit reflects the state of the WF (Pin 30) line. Whenever the WF pin goes high, an interrupt will be generated.

Bit 4 — Seek Complete
This bit reflects the state of the SC (Pin 32) line. Certain commands will pause until seek complete is true.

Bit 3 — Data Request
This bit reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BDRQ signal can be used in DMA interfacing, while the DRQ bit can be used for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host.

Bit 0 — Error
This bit is set whenever any bits in the error register are set. It is the logical 'or' of the error register and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
COMMAND							

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ (Pin 3) line, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:
R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands

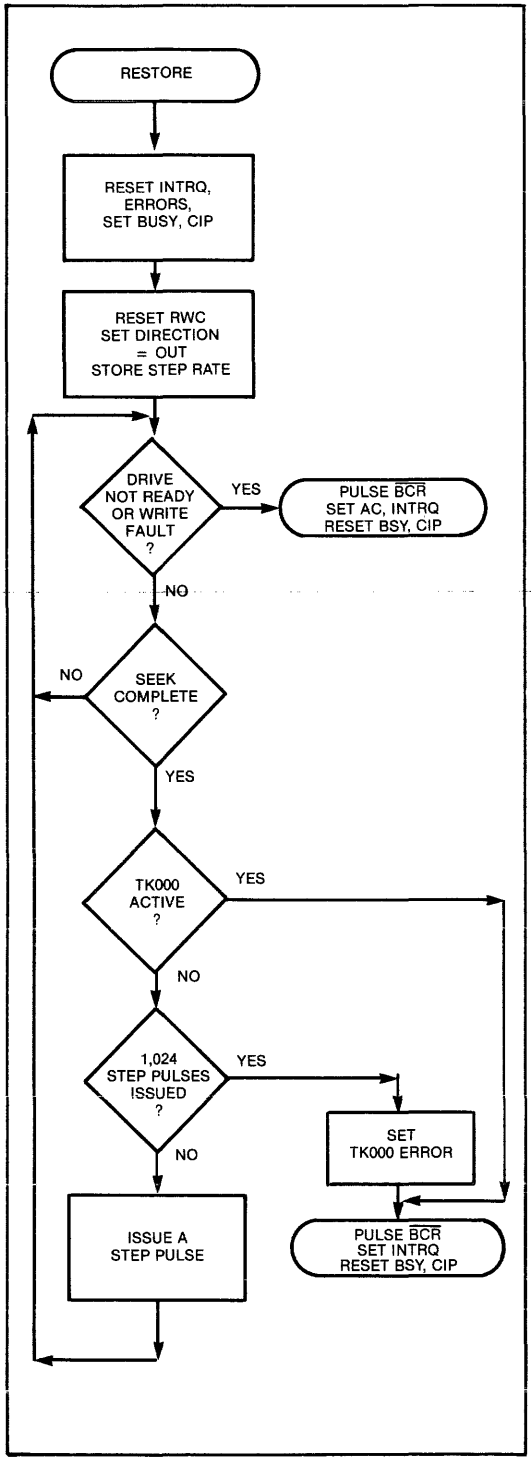
Should be set to 0 for WD1010-00
Should be set to 1 for WD1010-01

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010 waits for the Seek Complete line to go active before issuing the next pulse. If after 1,024 stepping pulses, the TK000 line does not go active, the WD1010 will set the TK000 error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

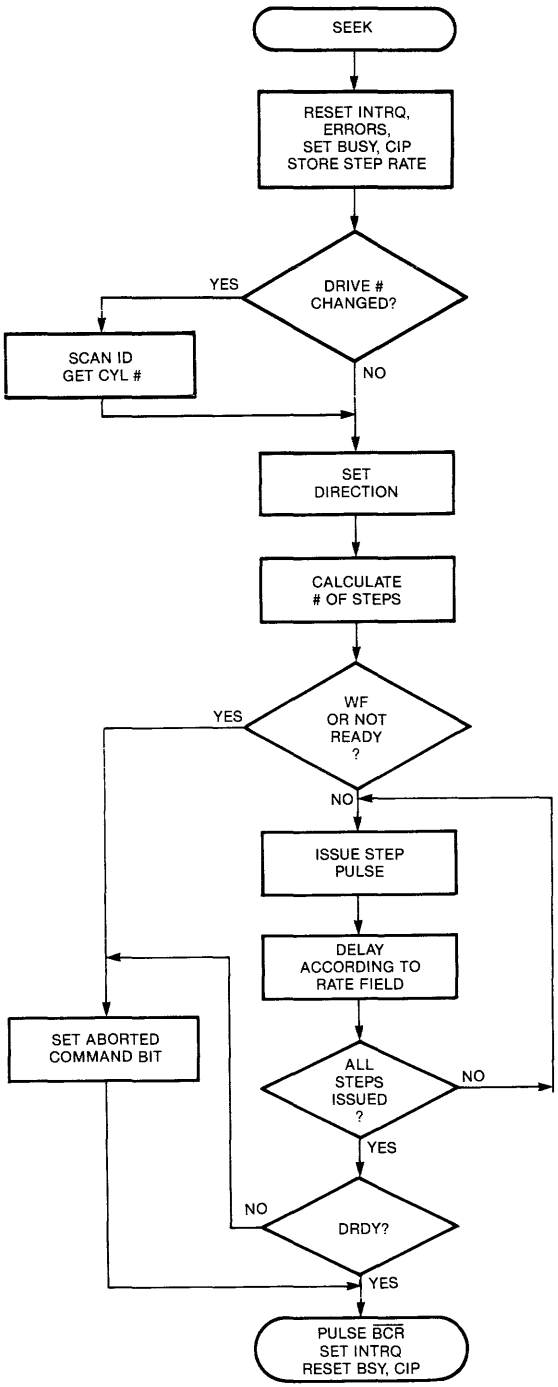
Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

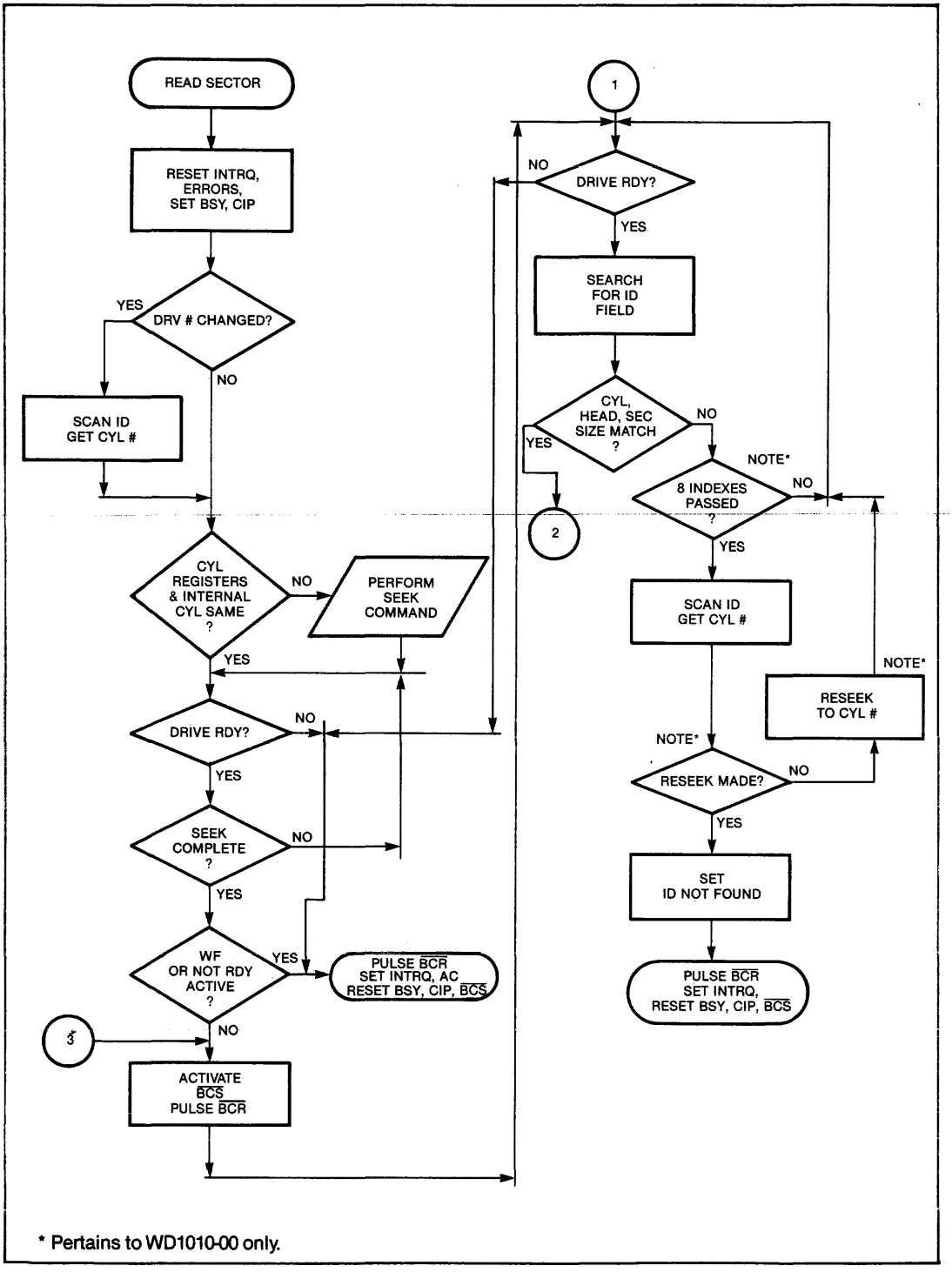
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

READ SECTOR

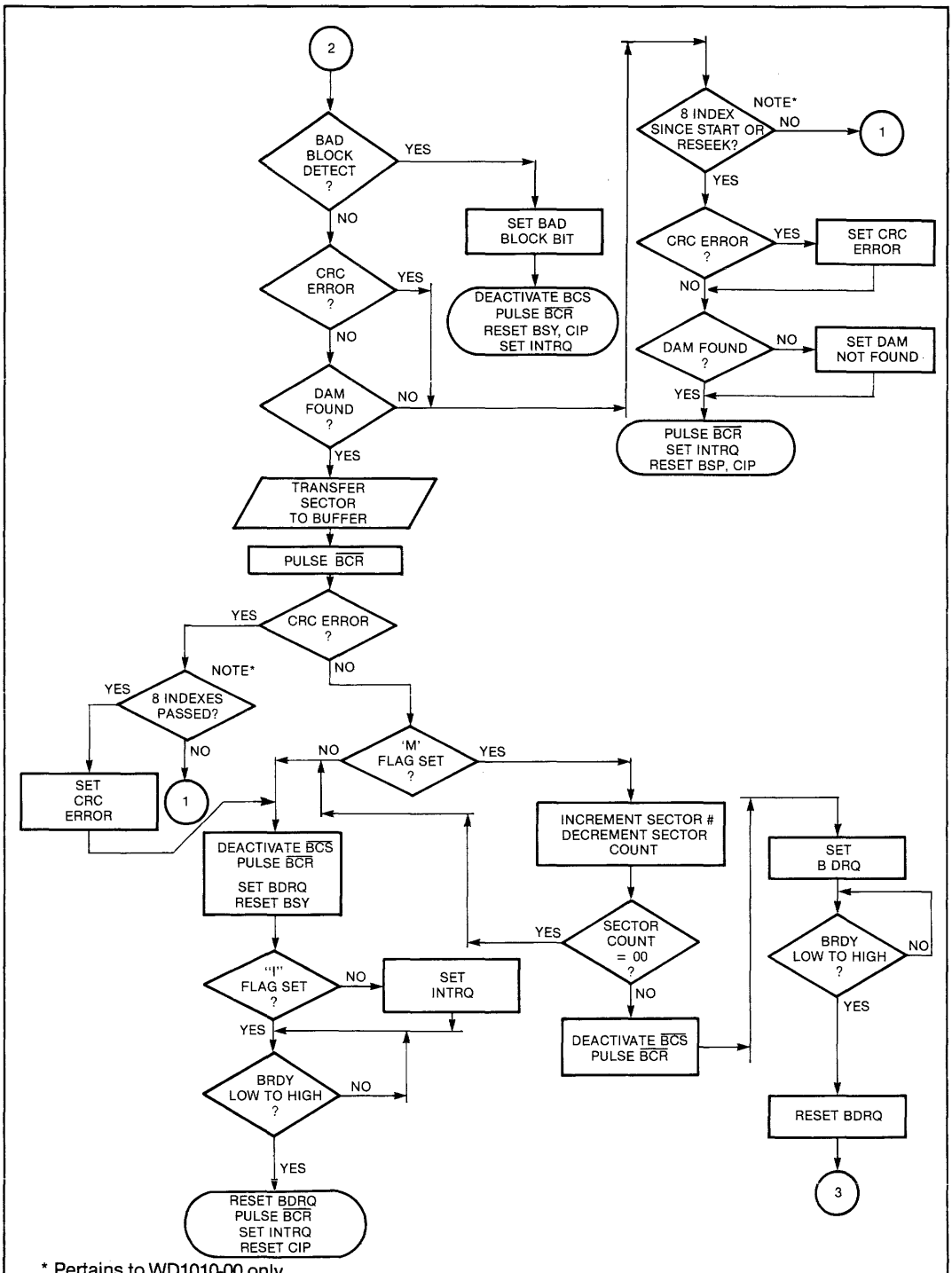
The read sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1010 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a seek takes place. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-00 must find an ID with the correct cylinder, head, sector size, and CRC within 8 revolutions; else the appropriate error bits will be set and the command terminated. If not, eight retries are performed with the ID-NOT-FOUND error bit set and the command terminated. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.


SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY ?
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED ?
NO
YES
DRDY?
NO
YES
PULSE BCR
SET INTRQ
RESET BSY, CIP



* Pertains to WD1010-00 only.



* Pertains to WD1010-00 only.

When the data address mark is found, the WD1010 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e. after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero or BRDY goes inactive. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BDRY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

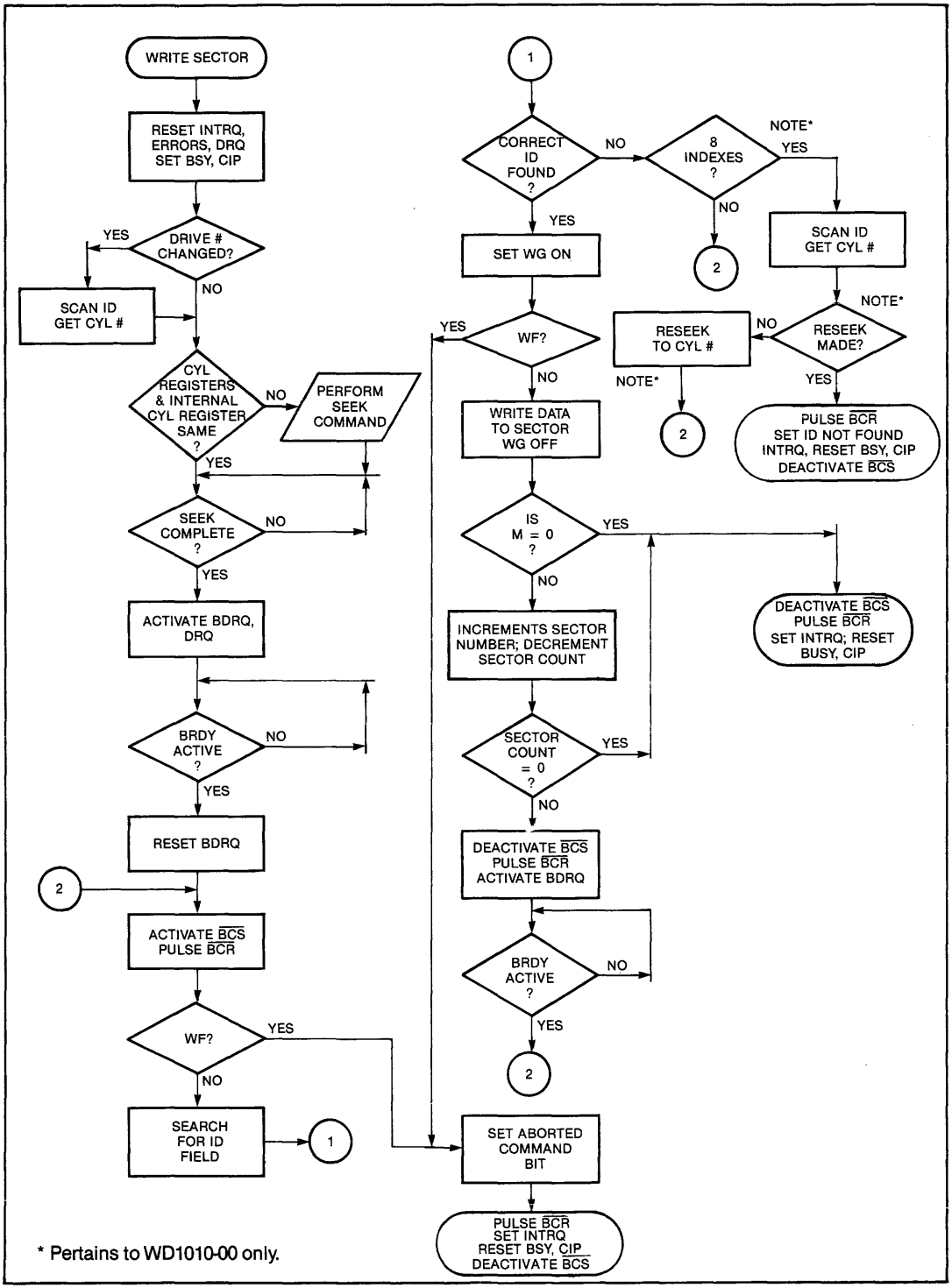
When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. If the ID field cannot be found within 8 revolutions, the ID not found bit is set and the command is terminated.


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME ?
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE ?
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE ?
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF?
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND ?
NO
8 INDEXES ?
NOTE*
YES
NO
2
SCAN ID GET CYL #
NOTE*
RESEEK MADE?
NO
YES
RESEEK TO CYL #
NOTE*
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
YES
SET WG ON
WF?
YES
NO
WRITE DATA TO SECTOR WG OFF
IS M = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENTS SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE ?
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
* Pertains to WD1010-00 only.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1010-00/01 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-00/01 will raise BDRQ and wait for the host to place more data in the buffer.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by WE strobes).
(4)	1010:	Waits for BRDY = low to high.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010 will retry up to 8 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'00' is normal; a H'80' indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of H'4E' are written for Gap 1 and Gap 3.

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

Figure 7.
FORMAT COMMAND BUFFER CONTENTS

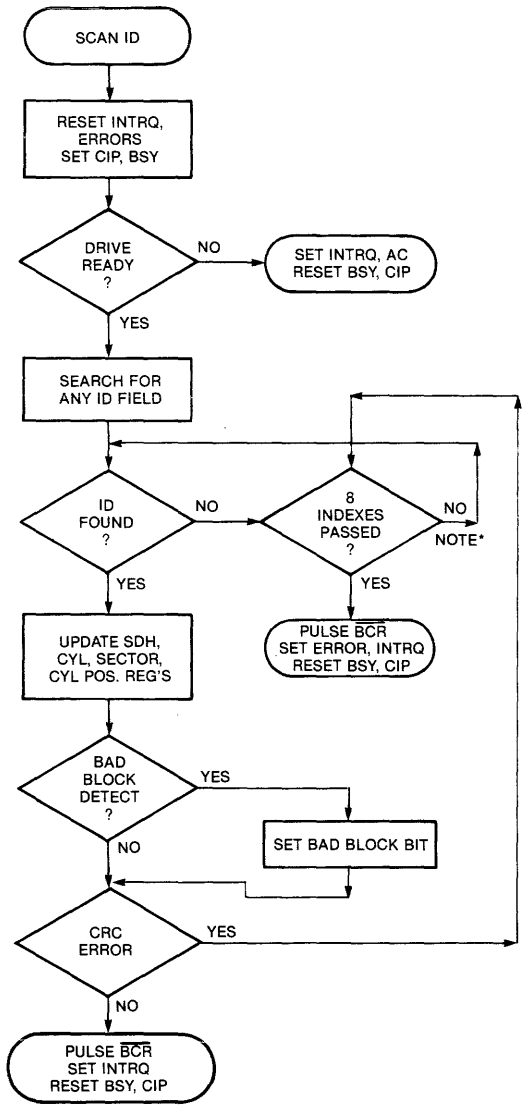
The data fields are filled with H'FF,' and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, H'4E' is filled until index. Like all commands, a write fault or drive not ready condition will terminate the command. Figure 8 shows the format that the WD1010 will write on the disk.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 value is:

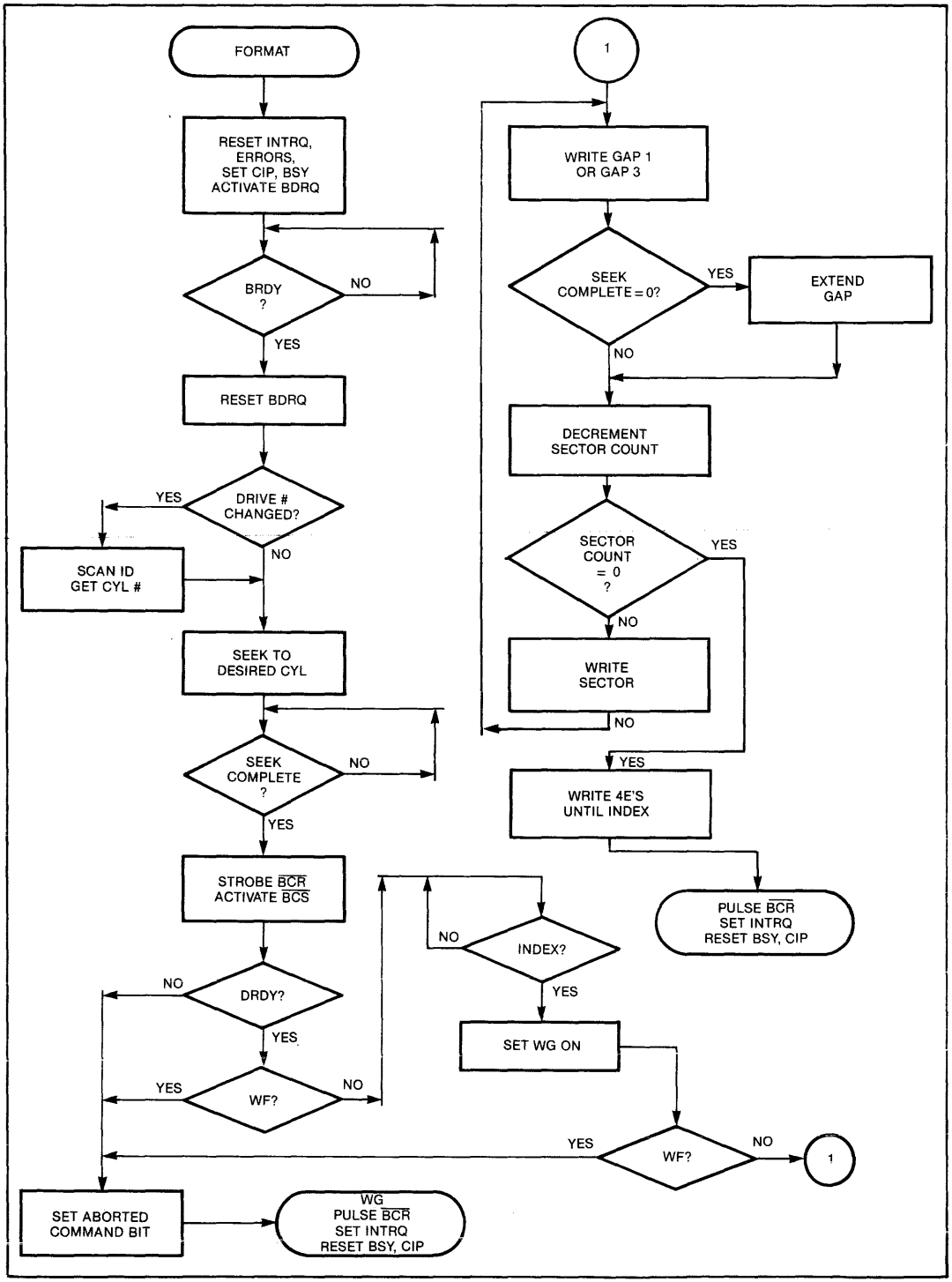
Gap 3 = 2*M*S + K + E

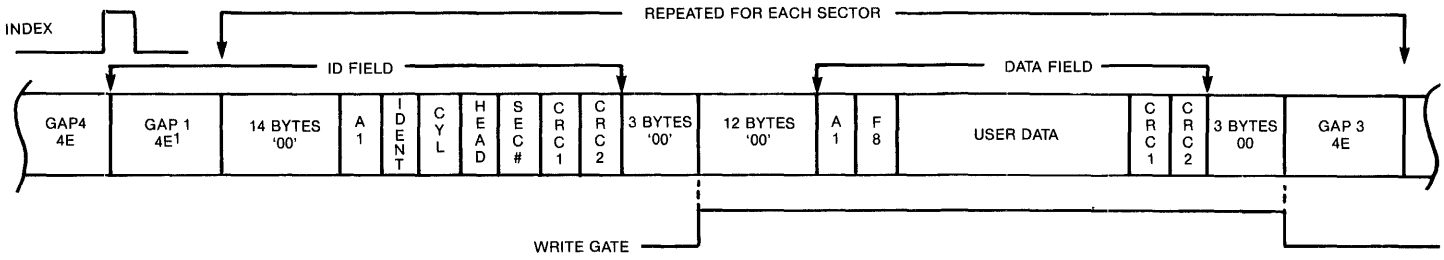
M = motor speed variation (e.g. .03 for + – 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010 will write on the Disk.



* Pertains to WD1010-00 only.


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY ?
NO
YES
RESET BDRQ
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE ?
NO
YES
STROBE BCR ACTIVATE BCS
DRDY?
NO
YES
WF?
YES
NO
SET ABORTED COMMAND BIT
WG PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0?
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
WRITE SECTOR
NO
YES
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP
NO
INDEX?
YES
SET WG ON
YES
WF?
NO
1



ID FIELD

A1 = H'A1' with H'0A' clock.

IDENT = MSB of Cylinder Number
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark

Sec # = Logical Sector Number

DATA FIELD

A1 = H'A1' with H'0A' Clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 128 to 1024 Bytes[2]

NOTES:
1. GAP1 and 3 length determined by sector number register contents during formatting.
2. If EXT bit in SDH register is set to 1 then an additional 7 data bytes are written, no CRC bytes are written.

Figure 8.
FORMAT

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

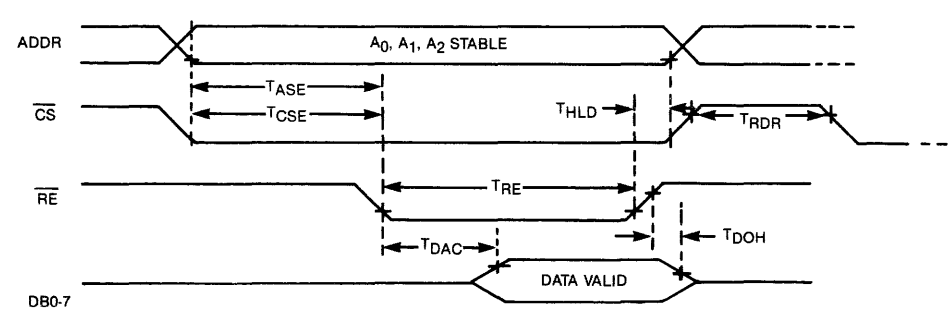
DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

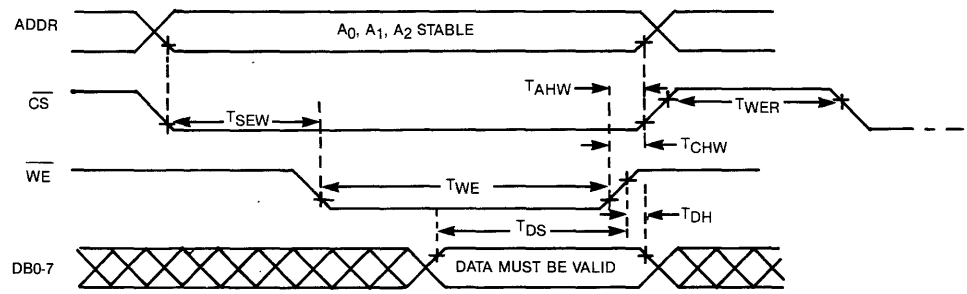
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To	0		ns	



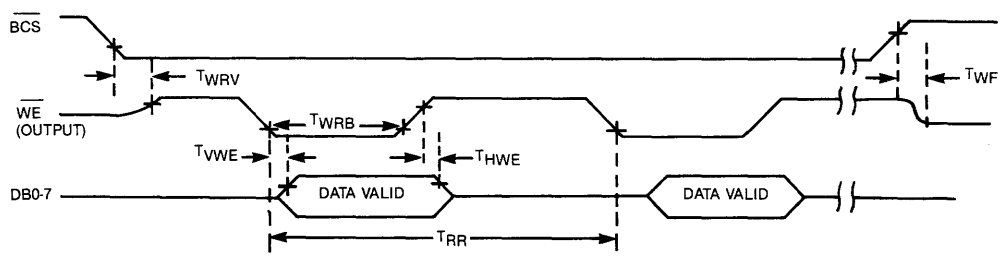
HOST READ TIMING



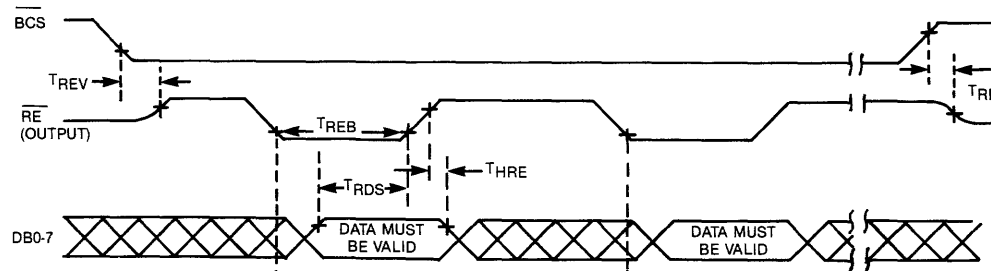
HOST WRITE TIMING

HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, $\overline{CS}$ Setup to $\overline{WE}$	0	10	μs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μs	
T_{WE}	Write Enable Pulse Width	.2	10	μs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		μs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time	0			



BUFFER WRITE TIMING



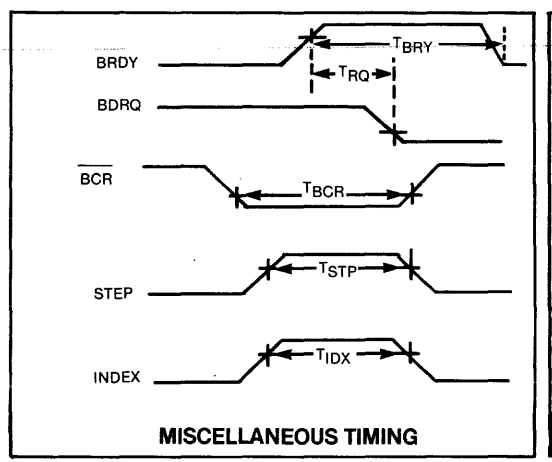
BUFFER READ TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

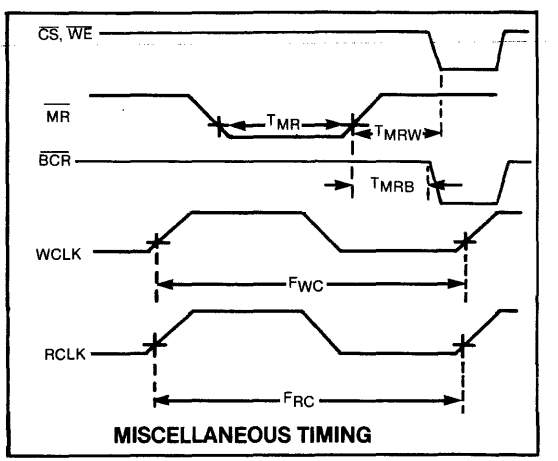
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			110	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf

BUFFER READ TIMING (WRITE SECTOR CMD)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	RE Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



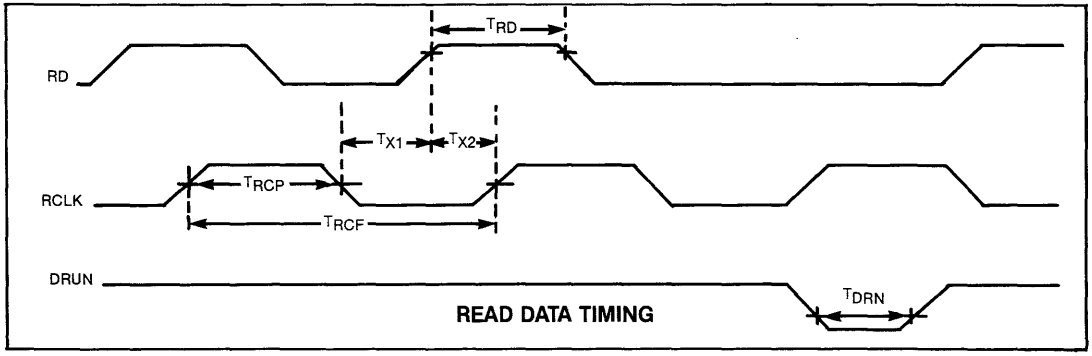
MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

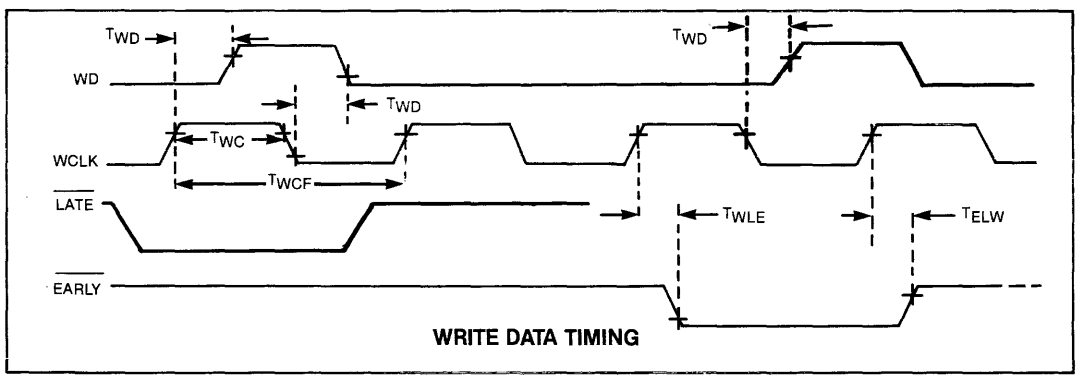
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	µs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	µs	See Note 2
T_{IDX}	Index Pulse Width	5		15	µs	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
F_{RC}	Read Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	µs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			µs	See Note 2



READ DATA TIMING

READ DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		$T_{RCP} \div 2$	ns	
T_{X2}	RD to RCLK Transition	20		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6



WRITE DATA TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

NOTES:
1. AC timing measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$, $C_L = 50$ pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. BRDY must be >4 μs or a spurious BDRQ pulse may exist for up to 27 μs after rising edge of BRDY.
6. $T_{RCF} = T_V$ ± 15%.

See page 481 for ordering information.

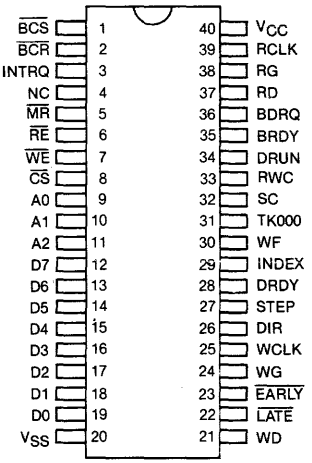
Printed in U.S.A.

PRELIMINARY

WD1010-05/08 Winchester Disk Controllers

FEATURES

- ST506/SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY WITH EXTERNAL ECC GENERATOR/CHECKER
- PROGRAMMABLE RETRIES
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1010-05/08 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5¼" and 8" products utilizing the same type of interface. On the host side, an 8 bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010-05/08.

Operating from a single 5 volt supply, the WD1010-05/08 is implemented in NMOS silicon gate technology and is available in a 40 pin dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
12-19	DATA 7 - DATA 0	D7-D0	Eight bit tristate bidirectional bus used for transfer of commands, status, and data.
6	READ ENABLE	$\overline{RE}$	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010-05/08 is reading the buffer.
7	WRITE ENABLE	$\overline{WE}$	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010-05/08 is writing to the buffer.
9-11	ADDRESS 0 - ADDRESS 2	A0-A2	These three inputs select the register to receive/transmit data on D0-D7.
8	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTERRUPT REQUEST	INTRQ	Active high output which is set to a logic high in the completion of any command.
5	MASTER RESET	$\overline{MR}$	A logic low in this input will initialize all internal logic.
1	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing of the external sector buffer.
35	BUFFER READY	BRDY	This rising edge activated input is used to inform the controller that the sector buffer is full or empty.
2	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed by the WD1010-05/08 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
36	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the sector buffer.
40	+5 VOLT	V_{CC}	+5V ±5% Power supply input.
20	GROUND	V_{SS}	Ground
4	NO CONNECT	NC	
21	WRITE DATA	WD	This output contains the MFM clock and data pulses to be written on the disk.
25	WRITE CLOCK	WCLK	4.34 or 5.0 Mhz clock input used to derive all internal write timing.
24	WRITE GATE	WG	This output is set to a logic high before writing is to be performed on the disk.
23, 22	EARLY, LATE	$\overline{EARLY}$, $\overline{LATE}$	Precompensation outputs used to delay the WD pulses externally.
37	READ DATA	RD	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	READ CLOCK	RCLK	A nominal square wave clock input derived from the external data recovery circuits.
38	READ GATE	RG	This output is set to a logic high when data is being inspected from the disk.
34	DATA RUN	DRUN	This input informs the WD1010-05/08 when a field of one's or zeroes have been detected.
27	STEP PULSE	STEP	This output generates a pulse for stepping the drive motor.
26	DIRECTION	DIR	This output determines the direction of the stepping motor.

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
28	DRIVE READY	DRDY	This input must be at a logic high in order for commands to execute.
30	WRITE FAULT	WF	An error input to the WD1010-05/08 which indicates a fault condition at the drive.
31	TRACK 000	TK000	An input to the WD1010-05/08 which indicates positioning over track 000.
29	INDEX PULSE	INDEX	A rising edge on this input informs the WD1010-05/08 when the index hole has been encountered.
33	REDUCED WRITE CURRENT	RWC	This output can be programmed to reduce write current on a selected starting cylinder.
32	SEEK COMPLETE	SC	A rising edge on this input informs the WD1010-05/08 when head settling time has expired.

ARCHITECTURE

The WD1010-05/08 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. The WD1010-05/08 may be programmed to either automatically retry errors, or to terminate the command. The internal architecture of the WD1010-05/08 is shown in Figure 1. Its major functional blocks are:

PLA Controller
The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator
A 10 bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

CRC Logic
Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is X16 + X12 + X5 + 1.

MFM Encode/Decode
Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from

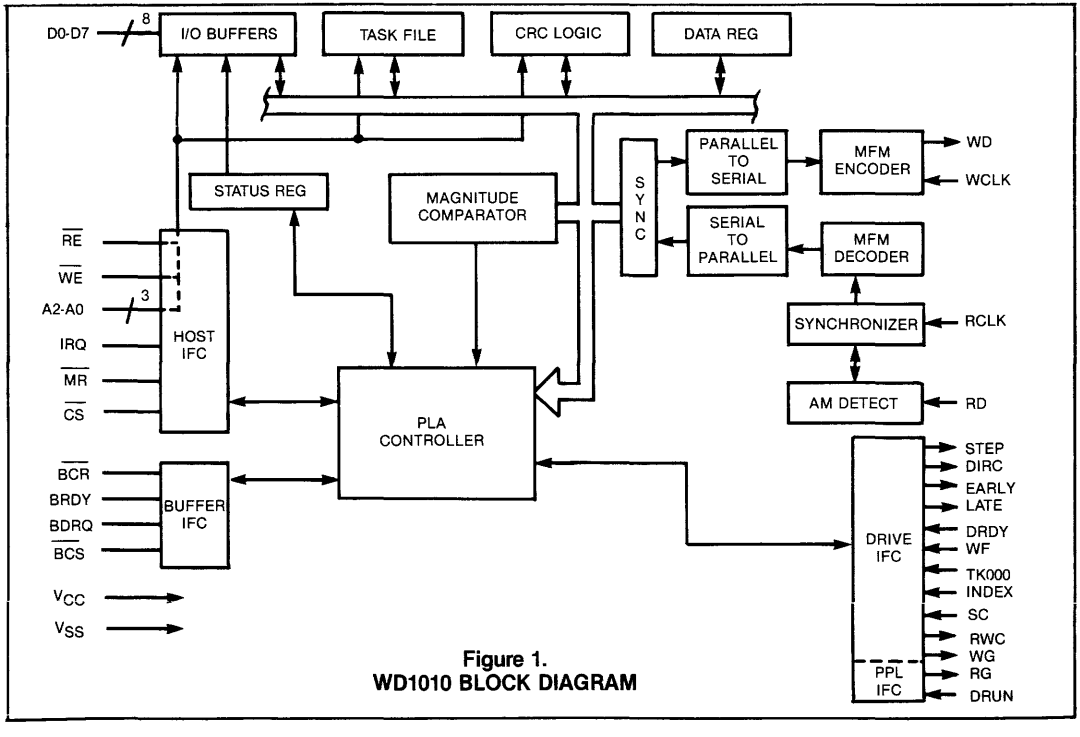


Figure 1.
WD1010 BLOCK DIAGRAM

WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect
The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = H'A1', Clock = H'0A') used in each ID and data field.

Host/Buffer IFC
This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC
This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010-05/08 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010-05/08 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010-05/08 interacts with the data separator through the DATA RUN (DRUN) and Read Gate (RG) signals. The block diagram of the data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010-05/08, the reference multiplexor, and a retriggerable one shot. The read gate (Pin 38) output will be low when the WD1010-05/08 is not inspecting data. The PLL at this time should remain locked to the reference clock.

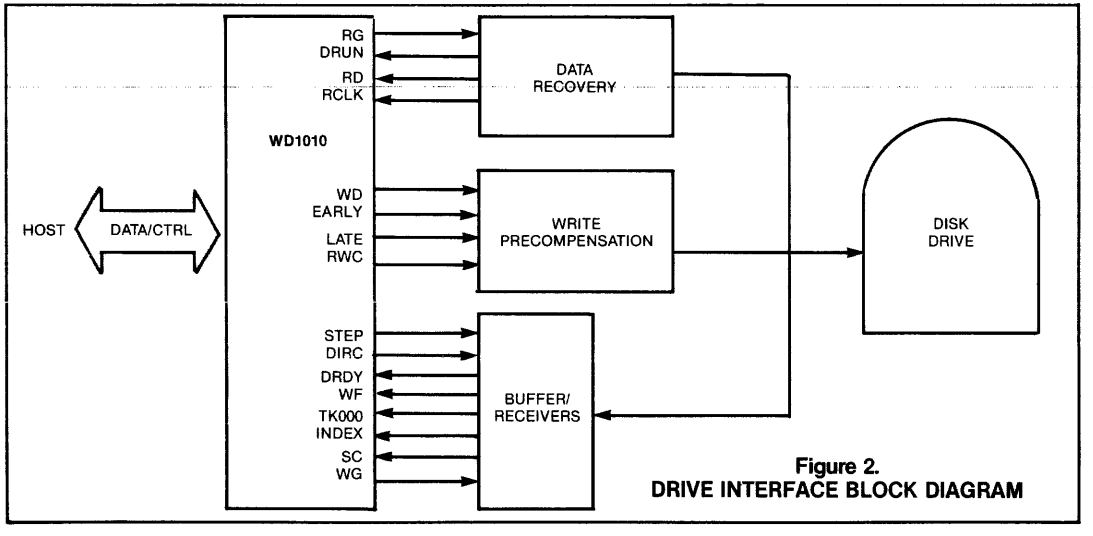


Figure 2.
DRIVE INTERFACE BLOCK DIAGRAM

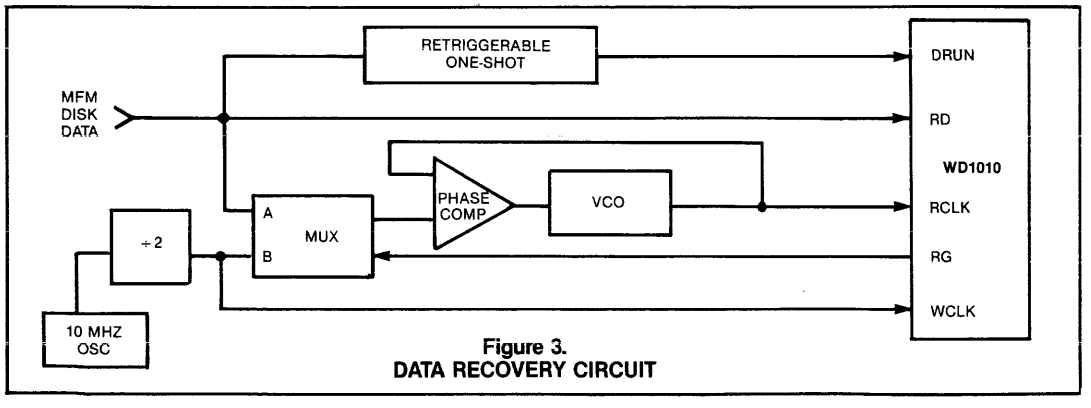


Figure 3.
DATA RECOVERY CIRCUIT

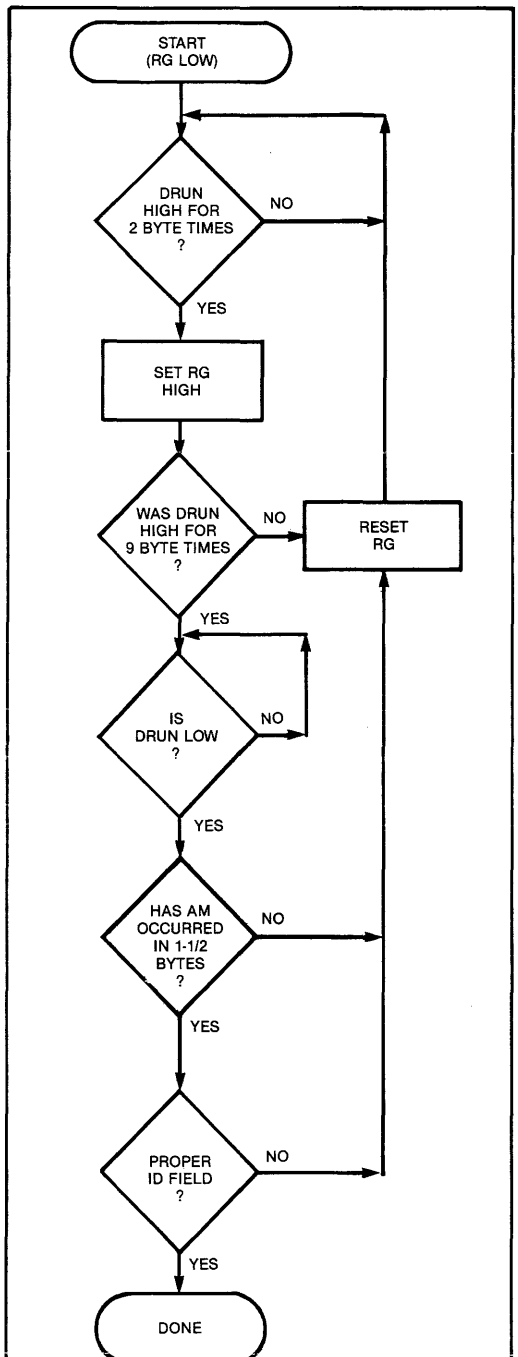


Figure 4.
PLL CONTROL SEQUENCE

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeros. An internal counter times out to see that DRUN is high for 16 bits (2 byte times). Read gate is set by the WD1010-05/08, switching the data separator to lock onto the incoming data stream. If DRUN falls prior to 72 bit times RG is lowered and the process is repeated. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals Reduce Write Current (RWC), $\overline{\text{Early}}$ and $\overline{\text{Late}}$. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder. If the write precomp register value is ff, then RWC will always be low.

The signals $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{Early}}$ occurs after the fact, write data should be delayed one interval when both $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are high; two intervals when $\overline{\text{Late}}$ is low; and no delay when $\overline{\text{Early}}$ is low. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{Early}}$ or $\overline{\text{Late}}$ will be active slightly ahead of the write data pulse; $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will never be low at the same time. Regardless of the contents of the RWC register, $\overline{\text{Early}}$ and $\overline{\text{Late}}$ will always be active.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010-05/08 is through an 8-bit bidirectional bus. This bus is used to transmit/receive data to both the WD1010-05/08 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010-05/08 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory. Whenever the WD1010-05/08 is not using the sector buffer, the Buffer Chip Select ($\overline{\text{BCS}}$) is high (disabled). This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_0-A_2 are '000'; an unused address in the WD1010-05/08. A binary counter is enabled when-

ever $\overline{RE}$ or $\overline{WE}$ goes active and incremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-$A_2 \neq$ '000'; allowing access to the WD1010-05/08's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. The WD1010 then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the Buffer Ready (BRDY) signal is made active (by the "carry" out of the counter), informing the WD1010-05/08 that the buffer is full. (BRDY is a rising edge activated signal.) The Buffer Chip Select ($\overline{BCS}$) is then made active, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010-05/08 to allow it access to the buffer. When the WD1010-05/08 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar matter, except the buffer is loaded by the WD1010-05/08 instead of the host.

Another control signal called Buffer Data Request (BDRQ; not used in Figure 5) is a DMA signal that can inform a direct memory access controller when the WD1010-05/08 is requesting data. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command, interrupts are generated at the termination of a command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The interrupt line (INTRQ) is cleared either by reading the status register or by writing a new command in the command register.

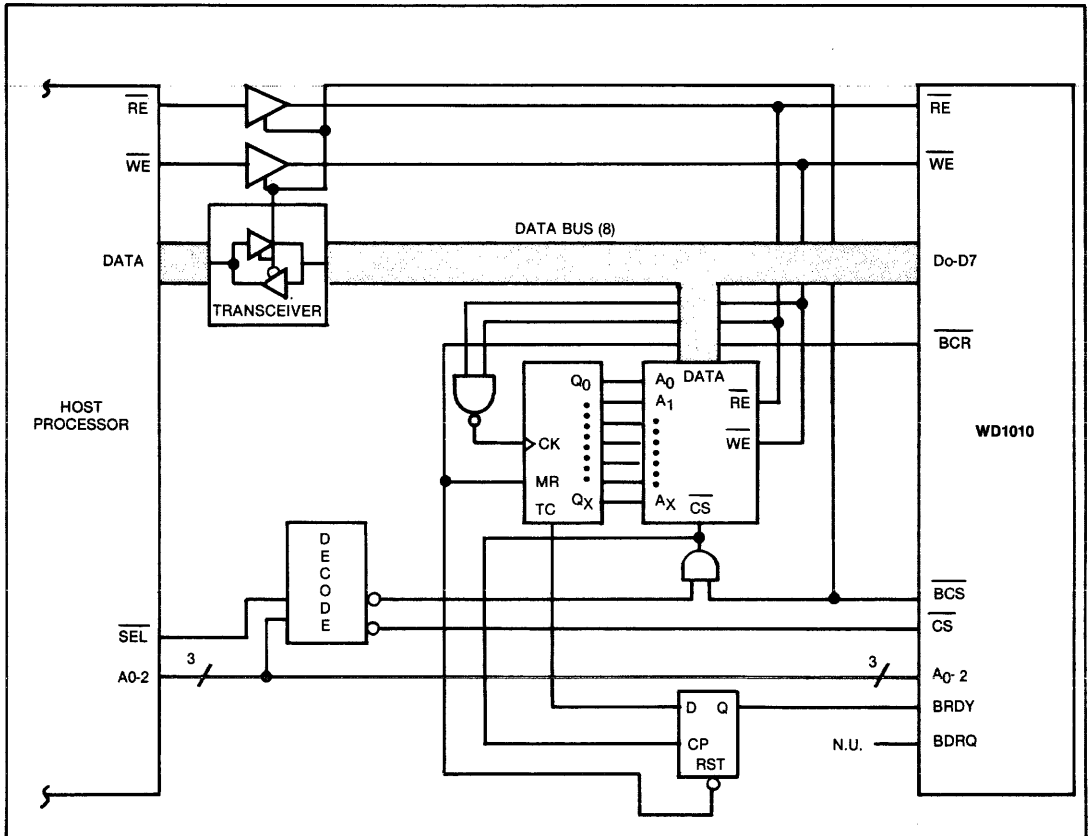


Figure 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addreses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are **not** cleared by master reset (MR).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a data field CRC error has occurred or the Data Address Mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 — Reserved
Not used; forced to a zero.

Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY (Pin 28) line is low or the WF (30) line is low. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — TK000 Error
This bit is set only by the restore command. It indictes that the TK000 (Pin 31) line has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC (Pin 33) line is asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of H'01' will cause RWC to activate on cylinder 4; H'02' on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . The RWC will be asserted when the present cylinder is equal to a greater than the value in this register. For example, the ST506 requires precomp on cylinder 128 (H'80') and above. Therefore, the write precomp cylinder register should be loaded with 32 (H'20').

A value of H'ff' will always cause RWC to be low, no matter what the cylinder number values are.

SECTOR COUNT

This register holds the number of sectors that are needed to be transferred to the buffer.

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector.

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant 8 bits of the desired cylinder number.

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010-05/08, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010-05/08 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:

7	6	5	4	3	2	1	0
EXT	SIZE		DRIVE		HEAD		

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010-05/08, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a formatting command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE		0	0	HEAD #		
7	6	5	4	3	2	1	0

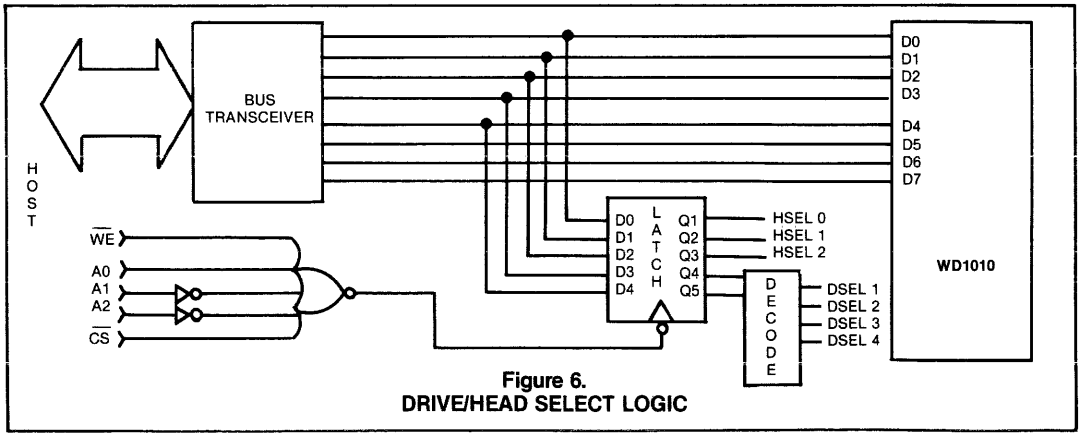


Figure 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7 — Busy
This bit is set whenever the WD1010-05/08 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010-05/08 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled. When the BUSY bit is set, no other bits in either the status or other registers are valid.

Bit 6 — Ready
This pin normally reflects the state of the DRDY (Pin 28) line. The state of this pin is latched after an 'aborted command' error

Bit 5 — Write Fault
This bit reflects the state of the WF (Pin 30) line. Whenever the WF pin goes high, an interrupt will be generated. The state of this pin latched after an 'aborted command' error.

Bit 4 — Seek Complete
This bit reflects the state of the SC (Pin 32) line. Certain commands will pause until seek complete is true. The state of this pin is latched after 'aborted command' error.

Bit 3 — Data Request
This bit reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BDRQ signal can be used in DMA interfacing, while the DRQ bit can be used for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host. Only the status register may be read. If other registers are read, the status register contents are returned.

Bit 0 — Error
This bit is set whenever any bits in the error register are set. It is the logical 'or' of the error register and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
		COMMAND					

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ (Pin 3) line, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	T
WRITE SECTOR	0	0	1	1	0	M	0	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:
R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands

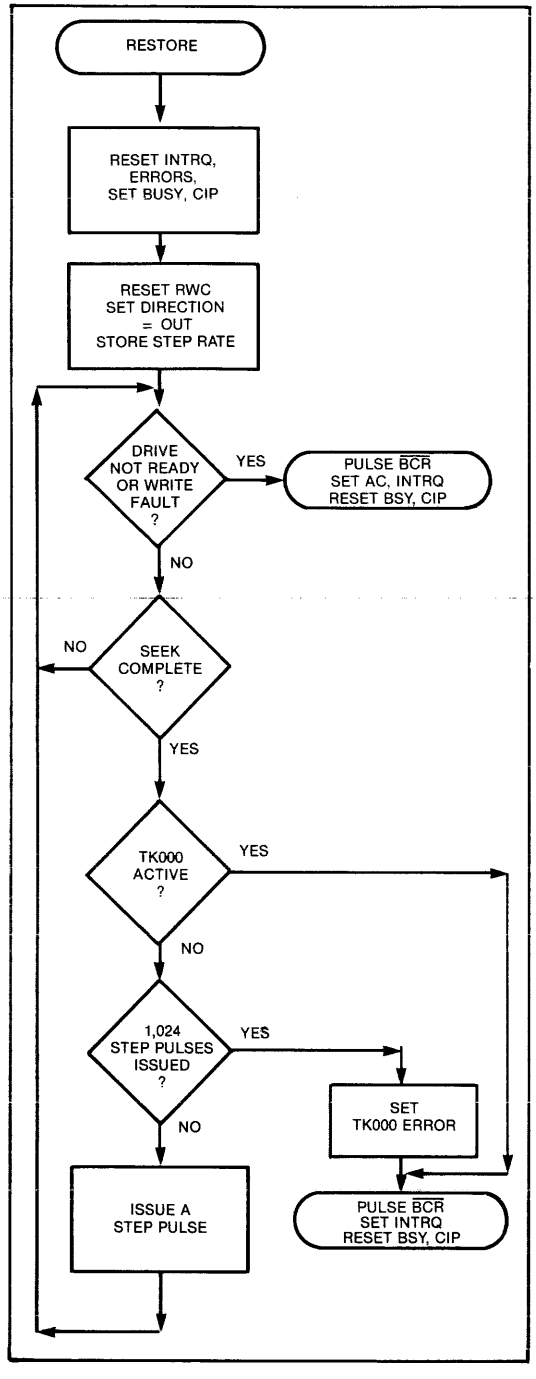
T = 0 Enable retries
T = 1 Disable retries

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010-05/08 waits for a rising edge on the seek complete line before issuing the next pulse. If 8 index pulses are received without a rising edge of seek complete, the WD1010 will switch to sensing the level of the SC line. If after 1,024 stepping pulses, the TK000 line does not go active, the WD1010-05/08 will set the TK000 error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

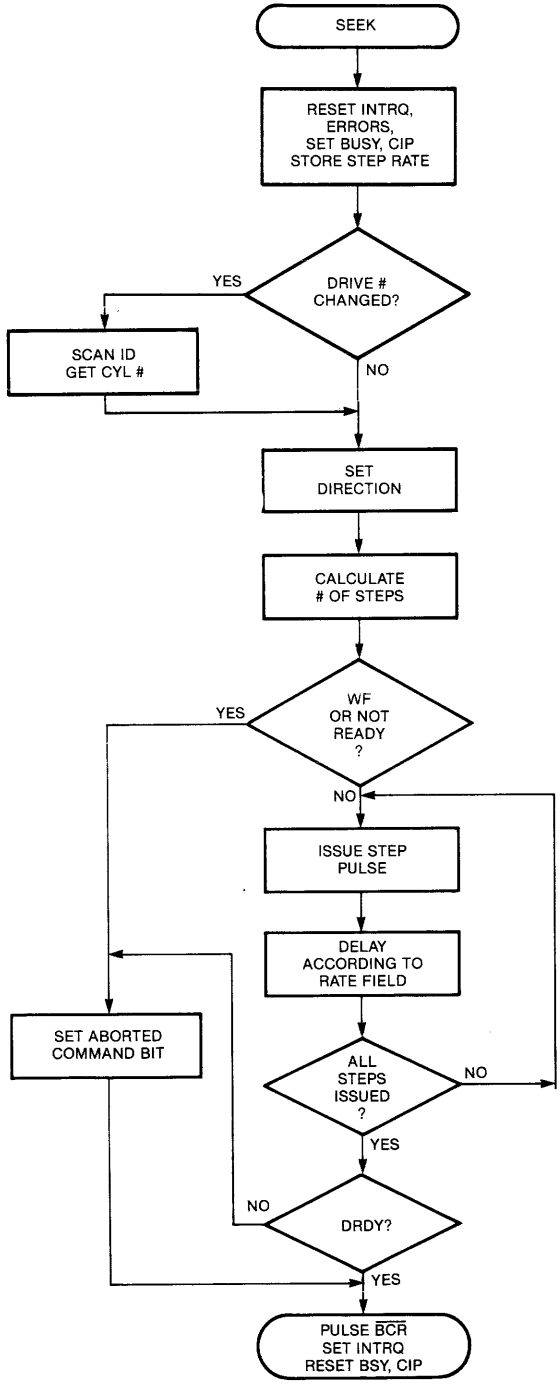
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

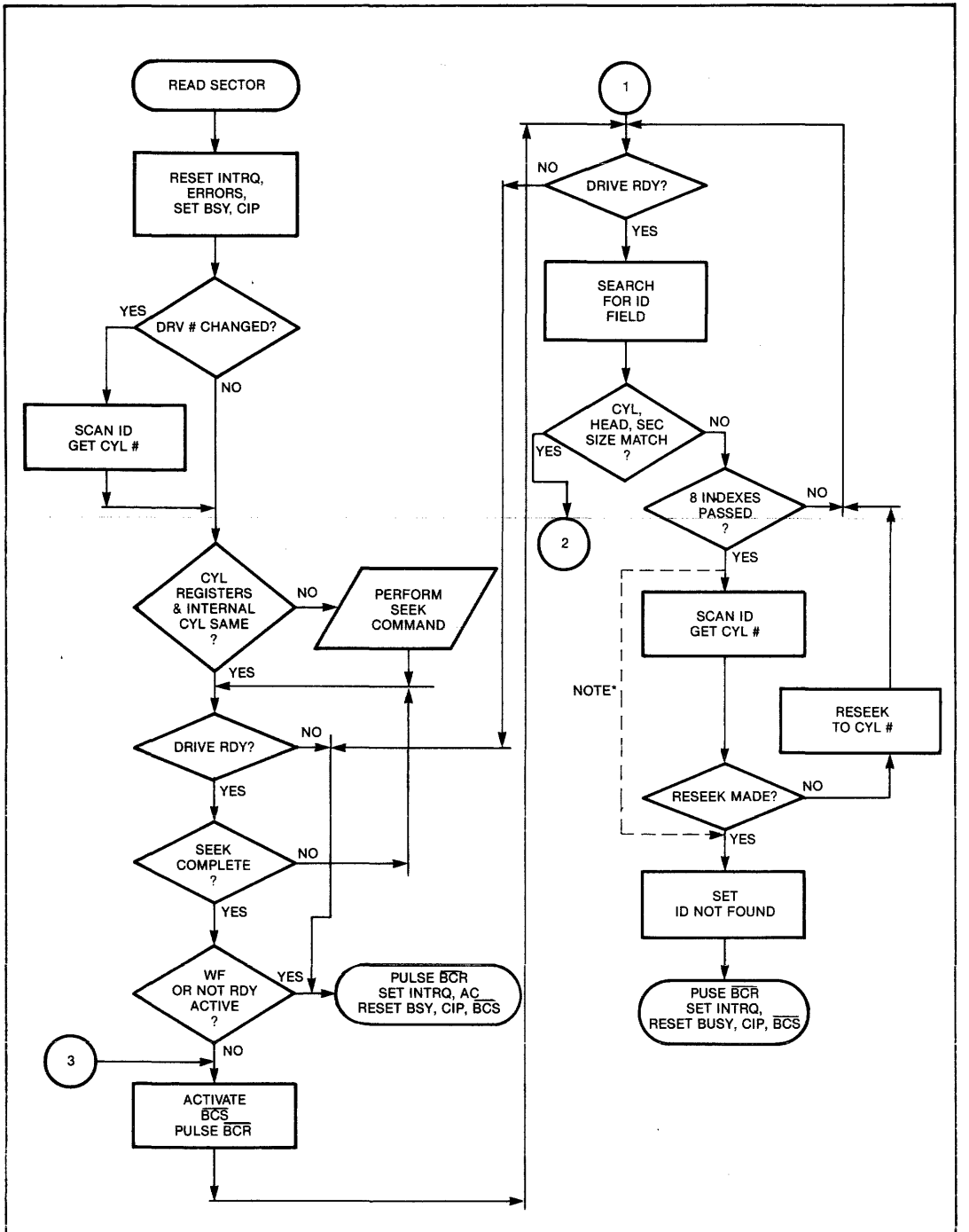
If an implied seek was performed, the WD1010-05/08 will search until a rising edge of Seek Complete is received.

READ SECTOR

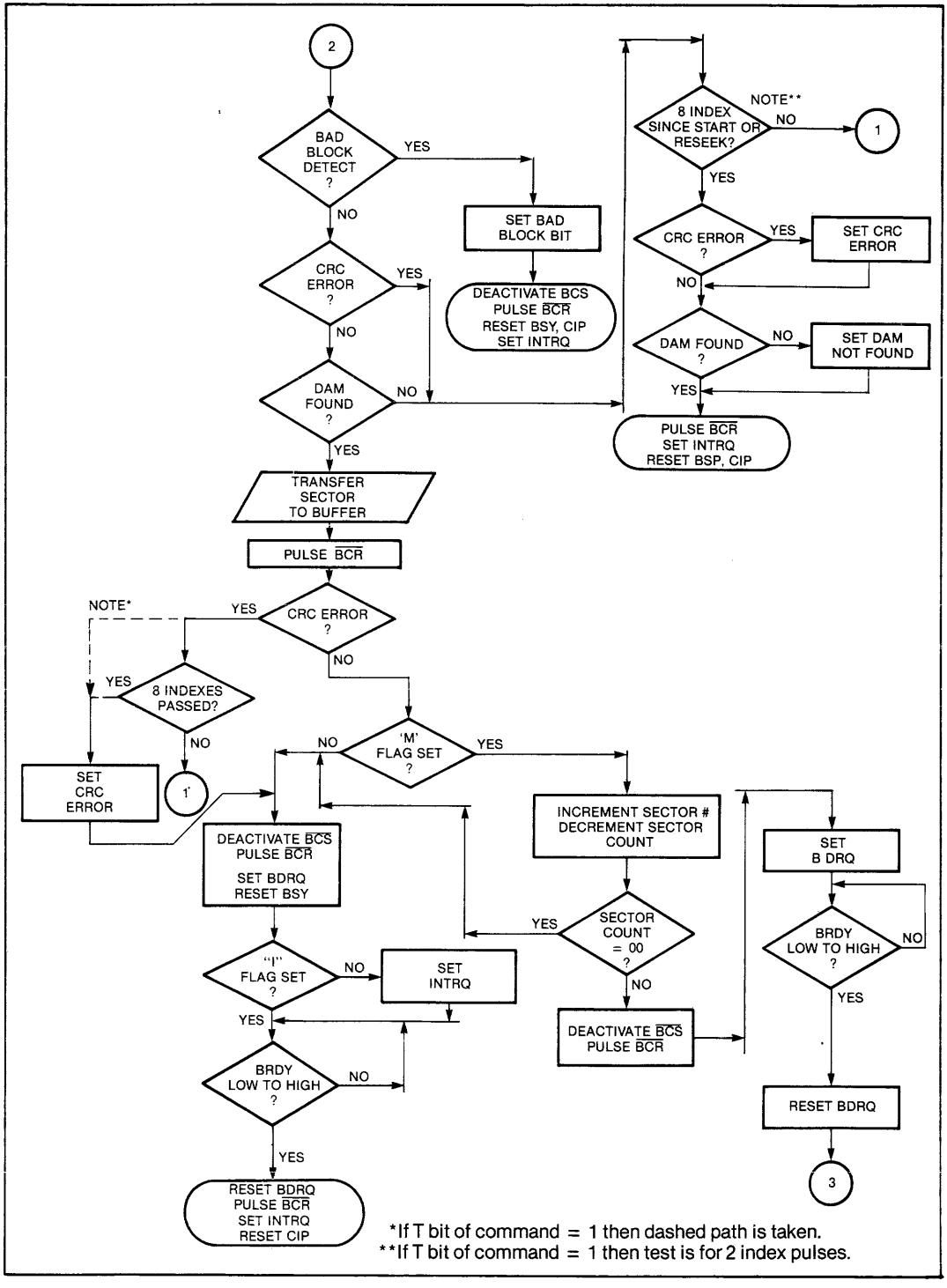
The read sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05/08 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a seek takes place. If an implied seek was performed, the WD1010-05/08 will search until a rising edge of seek complete is received. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-05/08 must find an ID with the correct cylinder, head, sector size, and CRC within 8 revolutions if T bit of command is zero, and within 2 revolutions if T = 1; else the appropriate error bits will be set and the command terminated if T = 1. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command. If T = 0, an automatic scan ID is performed to obtain cylinder position information and then, if necessary, a seek is performed. The search for the correct ID field is continued for 8 more disk rotations.


SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY ?
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED ?
NO
YES
DRDY?
NO
YES
PULSE BCR SET INTRQ RESET BSY, CIP



*If T bit of command = 1 then dashed path is taken after 2 index pulses.



*If T bit of command = 1 then dashed path is taken.
**If T bit of command = 1 then test is for 2 index pulses.

When the data address mark is found, the WD1010-05/08 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e. after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010-05/08 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero or BRDY goes inactive. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BDRY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

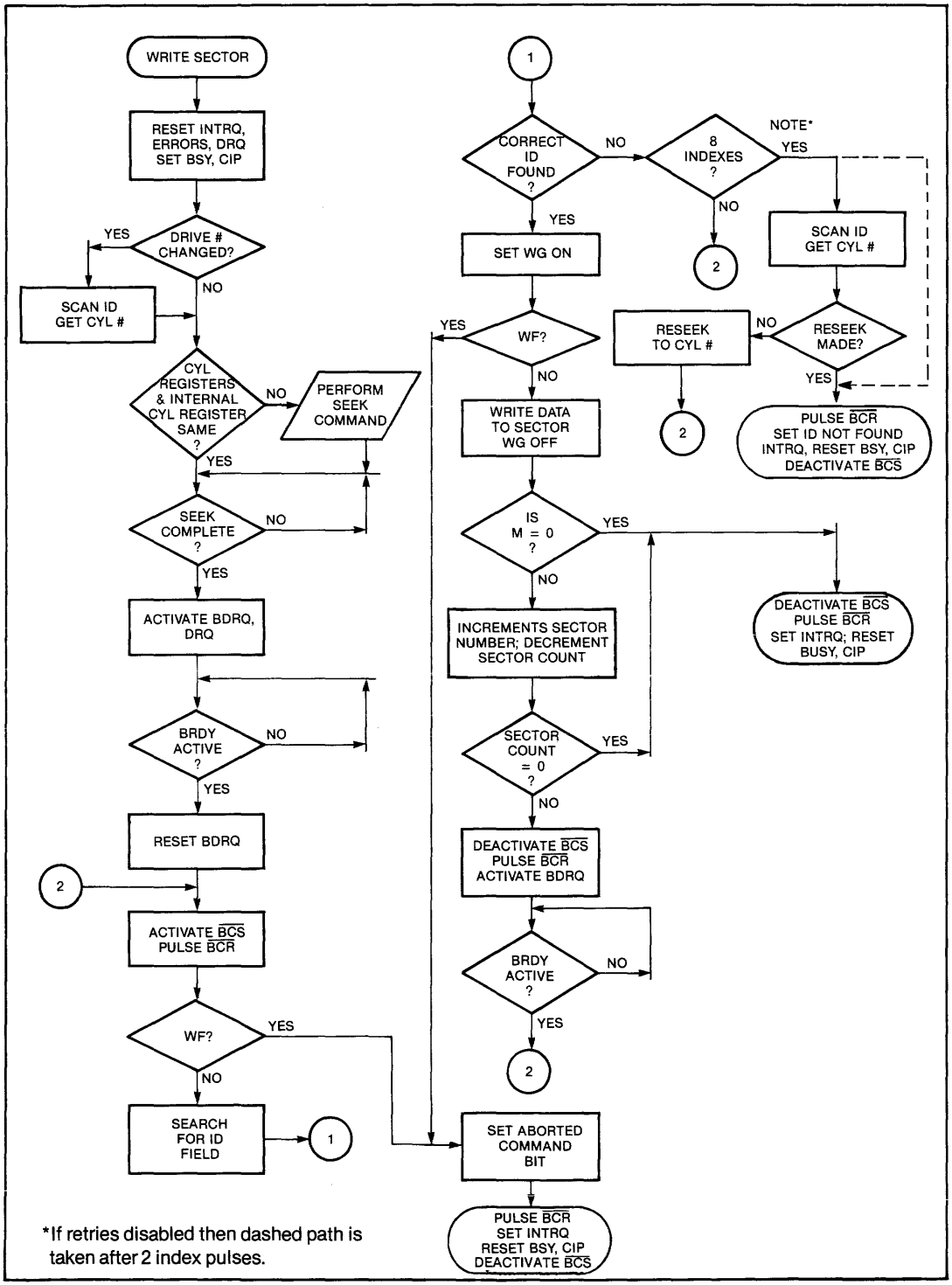
WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05/08 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010-05/08 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. If retries are disabled and if the ID field cannot be found within 2 revolutions, the ID not found bit is set and the command is terminated.

If retries are enabled, and the ID field cannot be found within 8 revolutions, an automatic scan ID and seek commands are performed. The ID Not Found error bit is set if the ID field is not found after 8 more revolutions.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1010-05/08 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-05/08 will raise BDRQ and wait for the host


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME ?
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE ?
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE ?
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF?
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND ?
NO
8 INDEXES ?
NOTE*
YES
NO
2
SCAN ID GET CYL #
RESEEK MADE?
NO
YES
RESEEK TO CYL #
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
YES
SET WG ON
WF?
YES
NO
WRITE DATA TO SECTOR WG OFF
IS M = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENTS SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE ?
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
*If retries disabled then dashed path is taken after 2 index pulses.

to place more data in the buffer.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by $\overline{WE}$ strobes).
(4)	1010:	Waits for BRDY = 1: then reset DRQ, BDRQ.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010-05/08 will retry up to 8 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'00' is normal; a H'80' indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010-05/08 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of H'4E' are written for Gap 1 and Gap 3. The data fields are filled with H'FF,' and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, H'4E' is filled until index.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

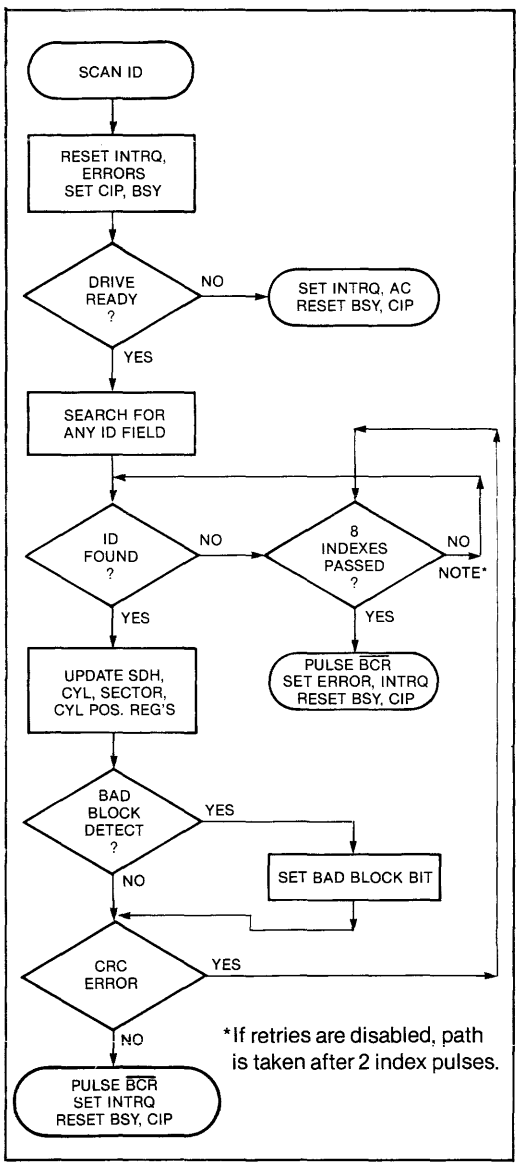
Figure 7.
FORMAT COMMAND BUFFER CONTENTS

factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E

M = motor speed variation (e.g. .03 for + − 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010-05/08 will write on the Disk.



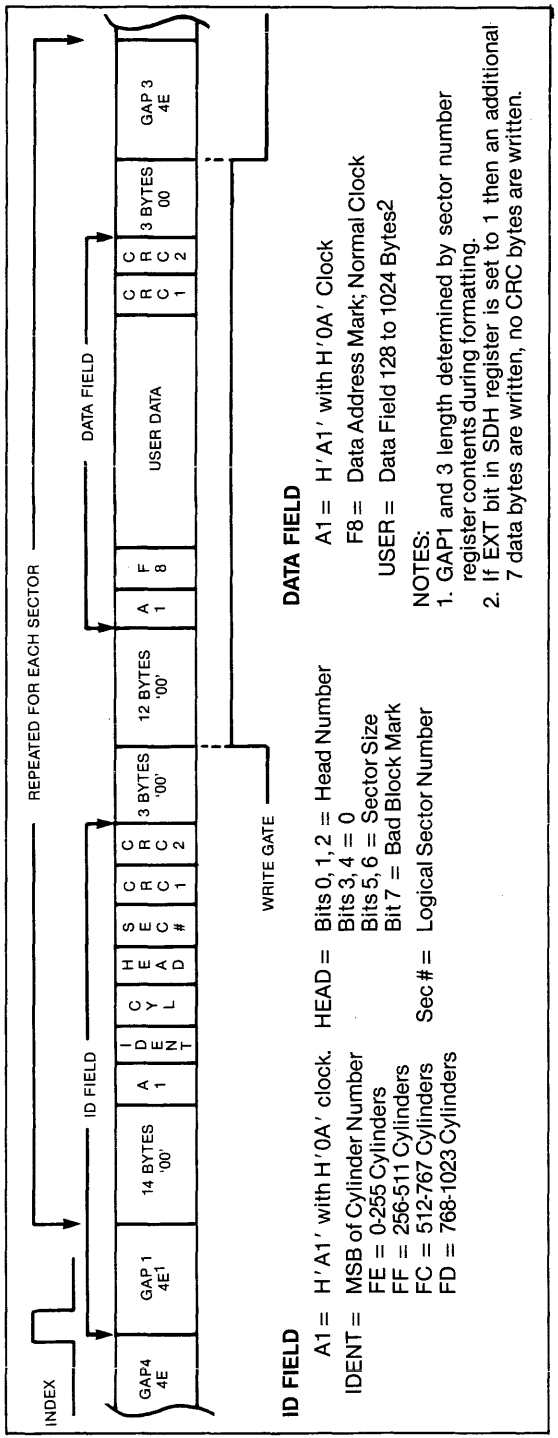
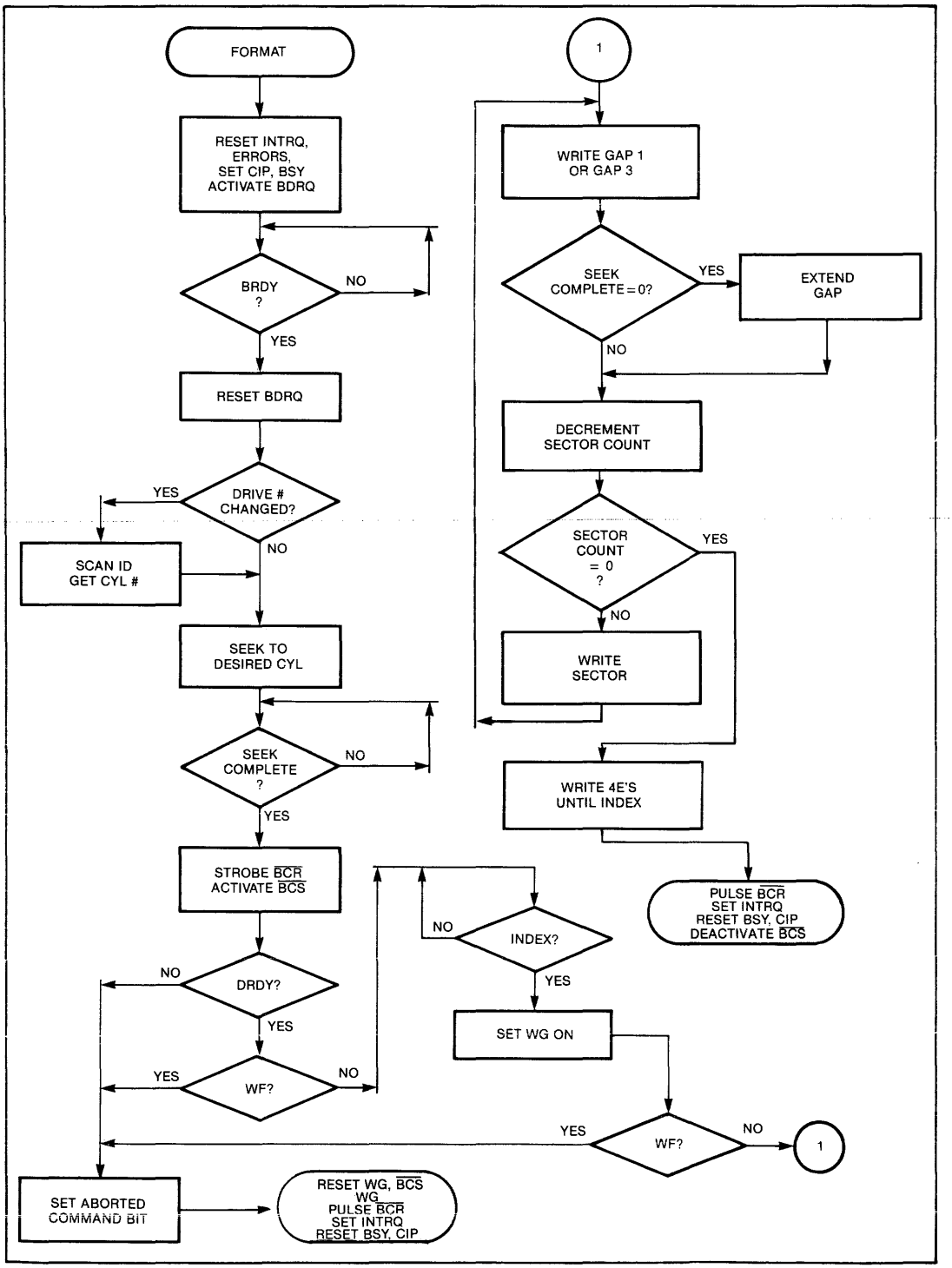


Figure 8. FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY ?
NO
YES
RESET BDRQ
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE ?
NO
YES
STROBE BCR ACTIVATE BCS
DRDY?
NO
YES
WF?
YES
NO
SET ABORTED COMMAND BIT
RESET WG, BCS WG PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0?
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
WRITE SECTOR
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
INDEX?
NO
YES
SET WG ON
WF?
YES
NO
1

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

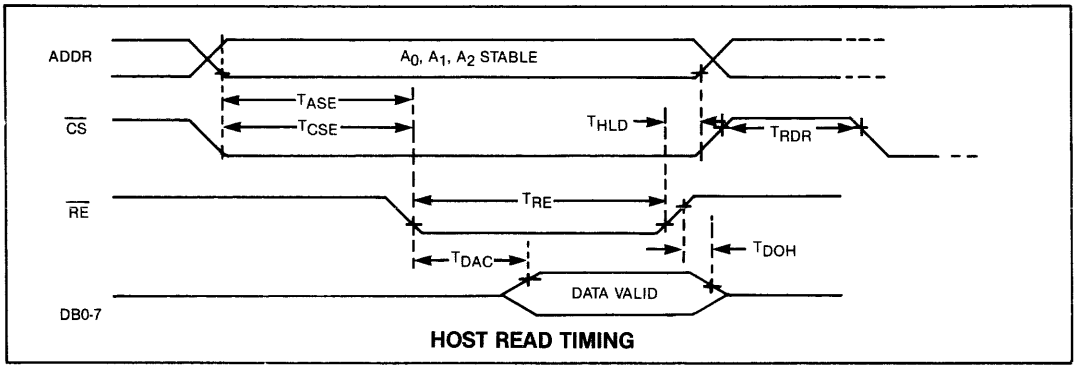
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

HOST READ TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To $\overline{RE}$	0		ns	

HOST READ TIMING WD1010-08 WC = 8 MHZ

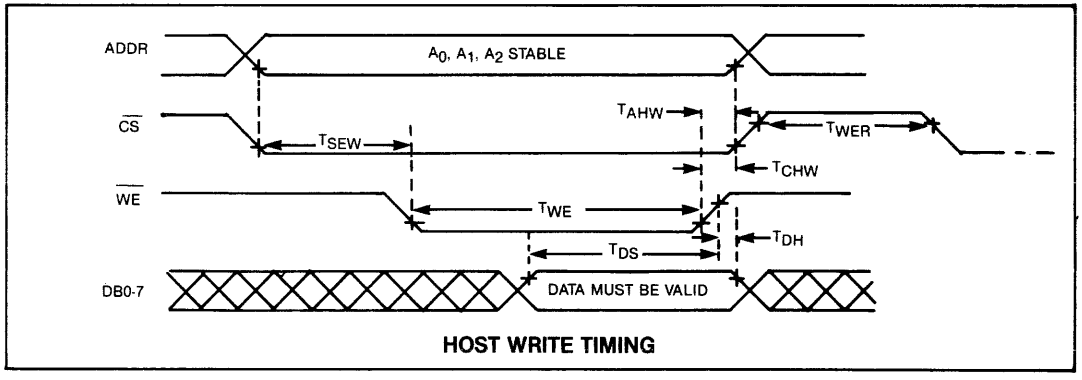
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		250	ns	
T_{RE}	Read Enable Pulse Width	.3	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	100	ns	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To $\overline{RE}$	0		ns	



HOST READ TIMING

HOST WRITE TIMING WD1010-05/08

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, CS Setup to $\overline{WE}$	0	10	μs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μs	
T_{WE}	Write Enable Pulse Width	.2	10	μs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		μs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time	0			



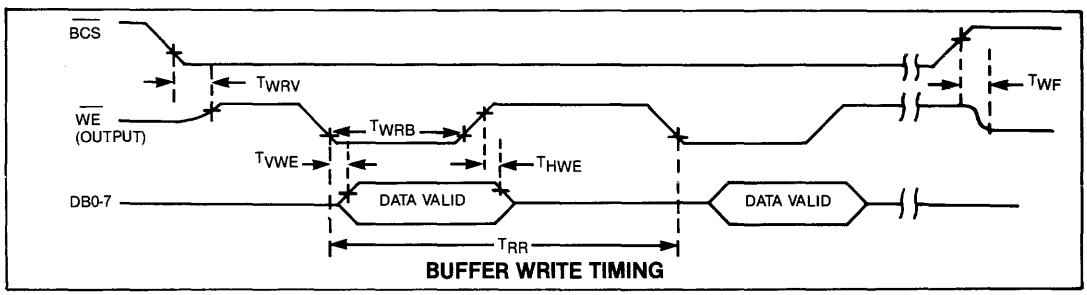
HOST WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			110	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-08 WC = 8 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	200	250	500	ns	See Note 7
T_{VWE}	Data Valid from $\overline{WE}$			100	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	.75	1.0	1.25	µs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf



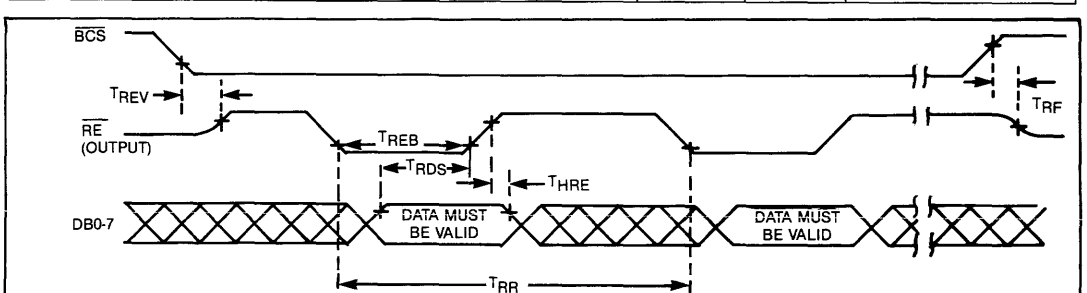
BUFFER WRITE TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-05 WC = 5 MHZ

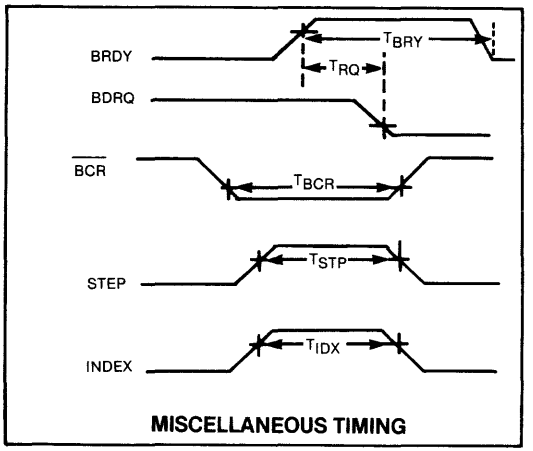
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	RE Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-08 WC = 8 MHZ

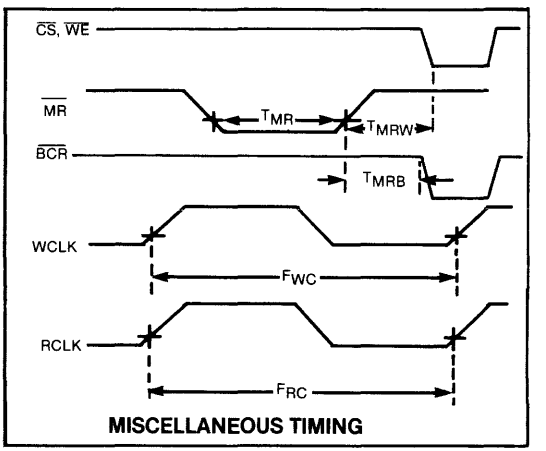
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	RE Output Pulse Width	200	250	300	ns	See Note 7
T_{RDS}	Data Setup to RE	100			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	.75	1.0	1.25	µs	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



BUFFER READ TIMING



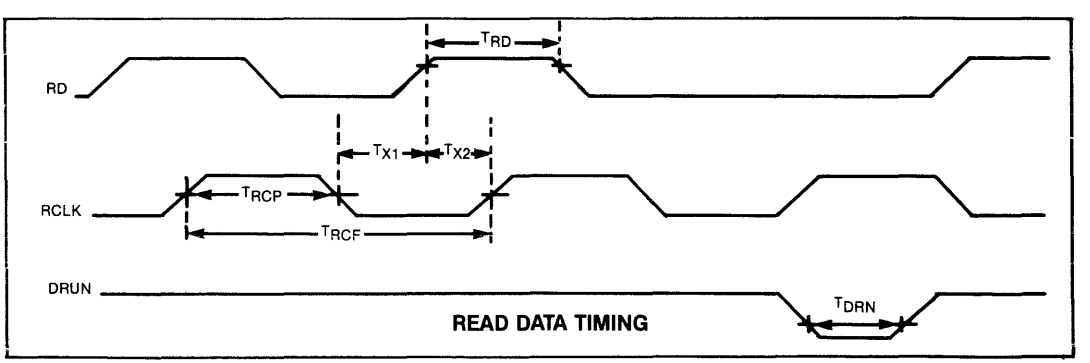
MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	µs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	µs	See Note 2
T_{IDX}	Index Pulse Width	500			ns	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
$F_{WC(-05)}$	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle, WD1010-05
$F_{RC(-05)}$	Read Clock Frequency	.25	5.0	5.25	MHz	See Note 6
$F_{WC(-08)}$	Write Clock Frequency	.25	8.0	8.4	MHz	50% Duty Cycle, WD1010-08
$F_{RC(-08)}$	Read Clock Frequency	.25	8.0	8.4	MHz	See Note 6
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	µs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			µs	See Note 2



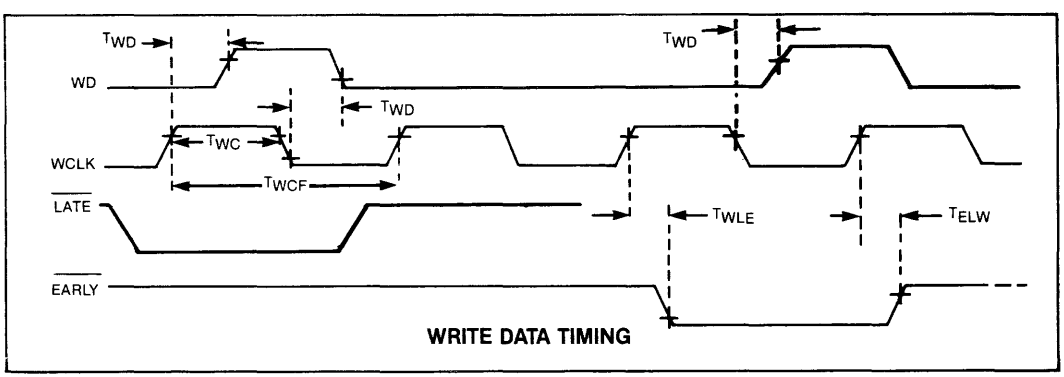
READ DATA TIMING

READ DATA TIMING WD1010-05 WD = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		$T_{RCP} \div 2$	ns	
T_{X2}	RD to RCLK Transition	20		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6

READ DATA TIMING WD1010-08 WD = 8 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	60		2000	ns	50% Duty Cycle
T_{X1}	RC Transition to Next Leading RD	0		$T_{RCP} \div 2$	ns	
T_{X2}	Leading RD to Next RC Transition	10		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	30		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	25			ns	
T_{RCF}	RCLK Frequency	.250		8.4	MHZ	See Note 6



WRITE DATA TIMING

WRITE DATA TIMING WD1010-05 WD = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

WRITE DATA TIMING WD1010-08 WD = 8 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		45	ns	
T_{WLE}	WCLK to Leading Early/Late	10		45	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		8.4	MHZ	See Note 6

NOTES:
1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V, C_L = 50 pf.
2. Based on WCLK = 5.0 MHz. Multiply timings by .625 for 8 MHz operation.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. BRDY must be >4 μs or a spurious BDRQ pulse may exist for up to 4 μs after rising edge of BRDY.
6. T_{RCF} = T_{WCF} ± 15%.
7. 2 WCLK ± 50 ns.

See page 481 for ordering information.

Printed in U.S.A.

WD1010 Application Notes

FLEXIBLE CONTROLLER MATES WITH POPULAR WINCHESTER DRIVES

To take advantage of the growing demand for Seagate Technology-type 5¼-in. Winchester disk drives in personal computers, electronic work stations, and small-business systems, designers need an appropriate controller that is inexpensive. In fact, today's designs must implement the control link between a host CPU and a disk drive at far lower cost than the drive itself. That requires a single-chip controller rather than discrete, gate-array-intensive circuits that take up valuable board space in ever smaller computer equipment.

Such a device is now available in the form of an LSI single-chip Winchester controller-formatter. The chip incorporates 80% of the circuitry required for Winchester control, eliminating between 50 and 75 SSI and MSI devices used in earlier designs.

A controller that claims Seagate compatibility must be sufficiently flexible to meet not only the company's original ST506 specifications, but also the various deviations from them. The basic specifications include a data rate of 5.0 Mbits/s and open-collector outputs and differential signal inputs for the separate control and data interface cables. The recording format is modified frequency modulation (MFM), but more importantly, the structure of the format defines both specific address-mark bytes and ID fields. These are fixed specifications, but manufacturers of Seagate-type drives sometimes make other changes. For example, the track density on high-capacity drives may be greater than that in the original ST506 specifications. Also, the number of sectors and bytes per sector on each cylinder can vary according to the application. In each case, a compatible controller must be able to handle the original specifications plus the deviations.

The ST506 interface is a spinoff of the Shugart Associates SA1000 drive, first introduced in 1979. Two important differences between the interfaces are the data rates and a timing-clock differential signal on the SA1000. The latter operates at 4.34 Mbits/s vs 5 Mbits/s for the ST506, but the remaining signals have enough similarity to permit a single controller design to run either an 8-in. SA1000 drive or the 5¼-in. ST506 drive. The advantage of the WD1010 Winchester controller-formatter is that it works with either and with other manufacturers' variations as well.

Operation of the drive begins when a host processor initiates a command after first loading a set of internal task registers called the task file. Information such as cylinder, sector, and head number is written to these registers, which are selected by address lines. The memory-mapped register scheme allows individual accesses to each register. Thus the host need not waste valuable time reading all the registers to obtain a specific parameter.

The WD1010, which comes in a 40-pin DIP, is run by an internal microcontroller — a PLA (programmable logic array) serving as a state machine (Fig. 1). This logic controls the flow of data throughout the chip, recognizes and processes commands, and formats the data.

WRITING AND READING DATA

During a write operation, parallel data is read from the data bus and written to a specific sector. But first the cylinder and sector must be located on the requested disk drive. The WD1010's micro-controller accesses its internal cylinder-position data and compares it with the requested cylinder number. If necessary, a seek is performed automatically to position the head assembly over the desired cylinder.

If the drive requested is changed before a seek command is executed, the WD1010 enables its read logic and searches for an ID field on the currently selected drive. Then it reads the cylinder number from the new ID field and determines whether to seek in or out to find the requested cylinder. This so-called implied seek is a feature of all commands (see "Macro Commands Provide Multiple Options").

After the WD1010 finds an ID field that matches the cylinder, head, sector, sector size and CRC (cyclic redundancy check) value, it writes a field of 0s and a new address mark — later these two fields will be used for synchronization during a read operation. The chip then reads parallel data in from the data bus, serializes it, and converts it into the MFM format. Next, a new CRC value is calculated for the incoming data and is appended to the end of the data field (after the last byte). If the original command specified multiple sectors, the next logical sector must be searched for and the process repeated. After the last sector is written, the WD1010 gives the bus back to the host and waits for the next command.

Although the chip does not generate an error correction signal, an optional command bit can be set to disable cyclic redundancy checks of the data field. The sector is extended by seven bytes to allow the host to write its 56-bit error detection and correction code. Later, during a read operation, these seven bytes are transferred back to the host to permit it to identify a syndrome and correct any errors that were encountered. For systems that require such operations, the WD1014 error detection and correction and

WD1015 buffer controller chips are available.

Reading is similar to writing except that data is sent out on the data bus and written into the sector buffer at the host. MFM data is entered on the RD pin along with a synchronous clock (RCLK) generated from an external data separator (Figure 2).

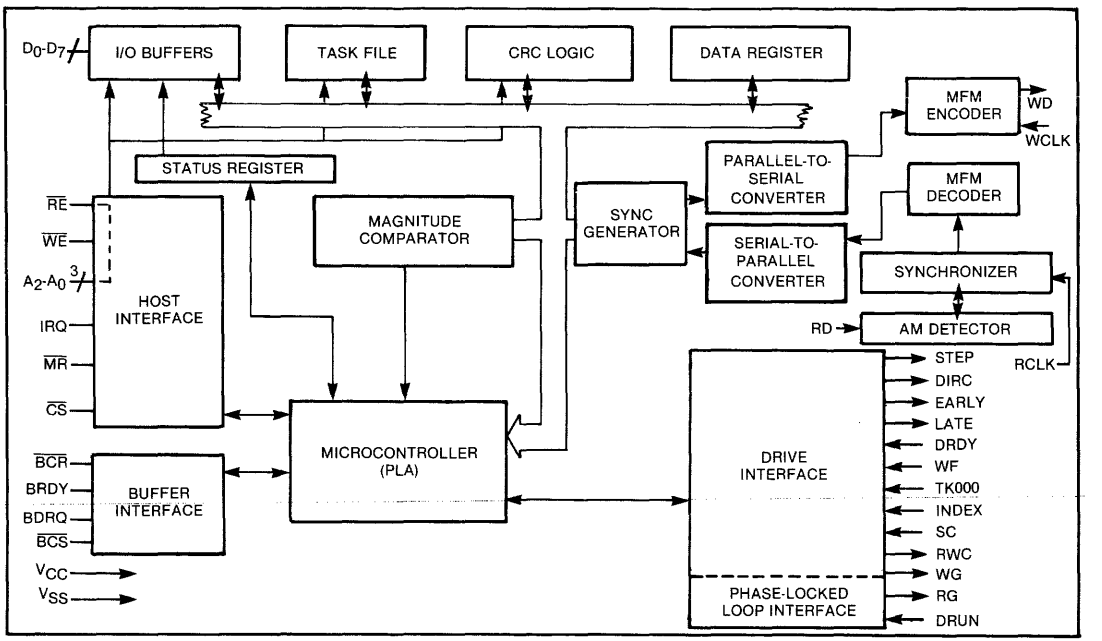


Figure 1.

The architecture of the WD1010 Winchester controller-formatter chip is designed to reduce a host processor's overhead burden. An internal microcontroller (PLA) manages data flow, incoming commands, and formatting.

Since the data rate is relatively high, the data separator must instruct the controller to lock on to the incoming data stream only during a field of 1s and 0s. A Data Run (DRUN) signal to the WD1010 indicates such an occurrence. When DRUN is active, the WD1010 counts off 16 bits — 2 byte times — sets the Read Gate (RG) signal, and starts to search the data stream for an address mark.

IMPLEMENTING THE PRECOMPENSATION ALGORITHM				
ALREADY SENT		SENDING	TO BE SENT	SHIFT REQUIRED
X	1	1	0	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

NOTE: All other patterns produce no shift.

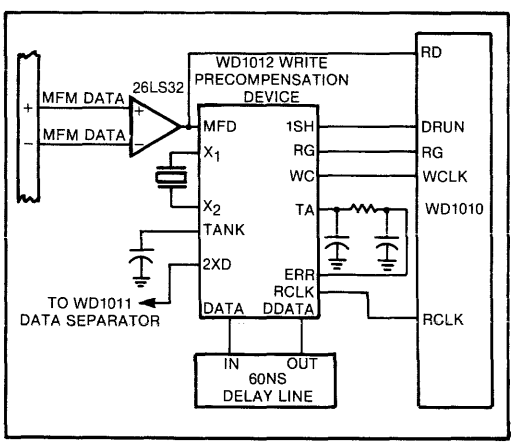


Figure 2.

A separate IC — the WD1012 — performs the data separation for the WD1010. The data separator sends a DRUN signal to the controller when it encounters a data field (1s and 0s).

An address mark is a unique pattern of clock and data bits that does not appear in any place that normal MFM data appears. If an address mark is not detected within nine bytes or if a non-0 pattern is detected within nine bytes, RG is turned off and the search repeated. Since data fields within sectors can contain 0s or all 1s, the DRUN algorithm is also triggered in these cases. But the address mark will not be detected, preventing erroneous data from being transferred.

After the ID field is compared and verified, a search begins for the address mark. Resynchronization occurs and the data is transferred to an internal MFM-to-NRZ converter. Data is then shifted through a double-buffered shift register and placed on the data bus for loading to the buffer. Either the cyclic redundancy code at the end of the data field is checked or the error detection and correction bytes are transferred in parallel to the host, depending on which option is used. Then the host processor can read the data from its local buffer.

Like all magnetic recording media, Winchester disks are not immune to the effects of bit shifts at high recording densities. The WD1010 uses an algorithm that informs external delay circuits when to shift outgoing data. A register within the task file specifies which cylinder receives reduced write current and if precompensation is needed. Typically, both occur on the same cylinder about half way down the disk surface.

The WD1010's precompensation signals are called $\overline{\text{Early}}$ and $\overline{\text{Late}}$. Depending on the bit pattern leaving the device, data will be shifted early, late, or not at all. A WD1011 data separator implements the precompensation delay network (Figure 3).

Since the $\overline{\text{Early}}$ signal and the current data (or clock) bits leaving the WD1010 have already occurred, the WD1011 performs no delay function on $\overline{\text{Early}}$. If both $\overline{\text{Early}}$ and $\overline{\text{Late}}$ are inactive, the WD1011 inserts a 12-ns delay; if only $\overline{\text{Late}}$ is active, it inserts a 24-ns delay. The result is a ± 12-ns shift of the data from its nominal position. An inactive Reduced Write Current (RWC) signal from the WD1010 disables the WD1011. The WD1010 then furnishes precompensation signals independent of current cylinder position.

INTERFACING WITH CABLES AND BUSES

The remaining function on the drive side is to provide sufficient buffers to drive the cables between the chip and the interface connectors. Single-ended open-collector signals are used for the control cable, and differential receiver-drivers are used for the data cable (Figure 4). Each line must have such buffers, since the controller is designed to drive one TTL load on all inputs and outputs.

At a 5-Mbit/s data transfer rate to the host interface, a byte of data must be read every 1.6 μs — in 8-bit parallel form. Few microprocessors can access a port and check status within this period. Consequently, a design objective of the WD1010 is compatibility with a programmed I/O environment, as well as the support of off-line error detection and correction. Moreover, the chip can transfer multiple sectors on one command. To achieve such performance within the constraints of a 40-pin package, the WD1010 relies on a unique approach to the traditional peripheral interface.

Three modes of communication can exist at the host interface: between the host and the WD1010, between the host and the buffer, and between the WD1010 and the buffer. For host-WD1010 commun-

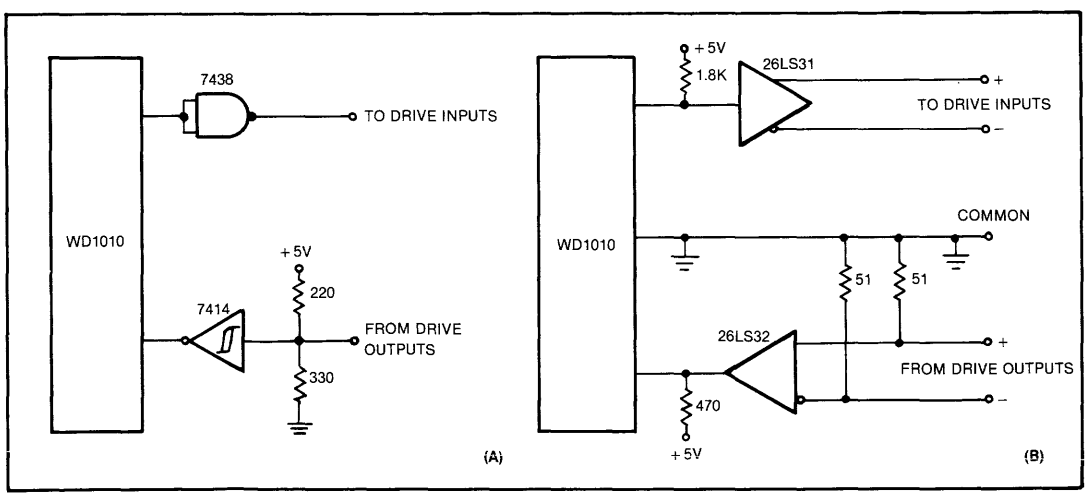


Figure 3.
Buffering circuits from the WD1010 to the control cable (A) and the data cable (B) must be used because the controller has a rather limited drive capability (one TTL load each on inputs and outputs).

ication the chip, like many microprocessors, talks over an 8-bit bidirectional bus, plus Read, Write and chip select lines (Figure 5). Three address lines access registers within the chip.

In host-buffer or WD1010-buffer communications (Figure 6), when the chip reads or writes to the buffer, the Buffer Chip Select ($\overline{BSC}$) line is pulled low. This signal should be used to disconnect the host data

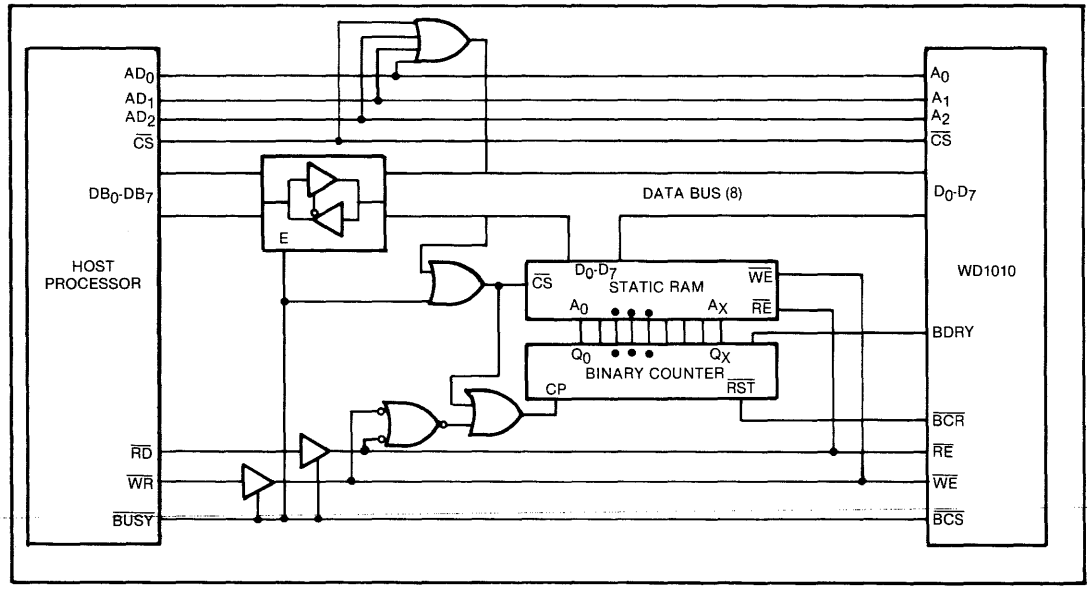


Figure 4.

Communications between a host and the WD1010 can be effected with the static RAM and binary counter circuitry shown here. These devices form a sector buffer that stores data sent from the host or the controller. This hardware handles both read and write operations on multiple sectors.

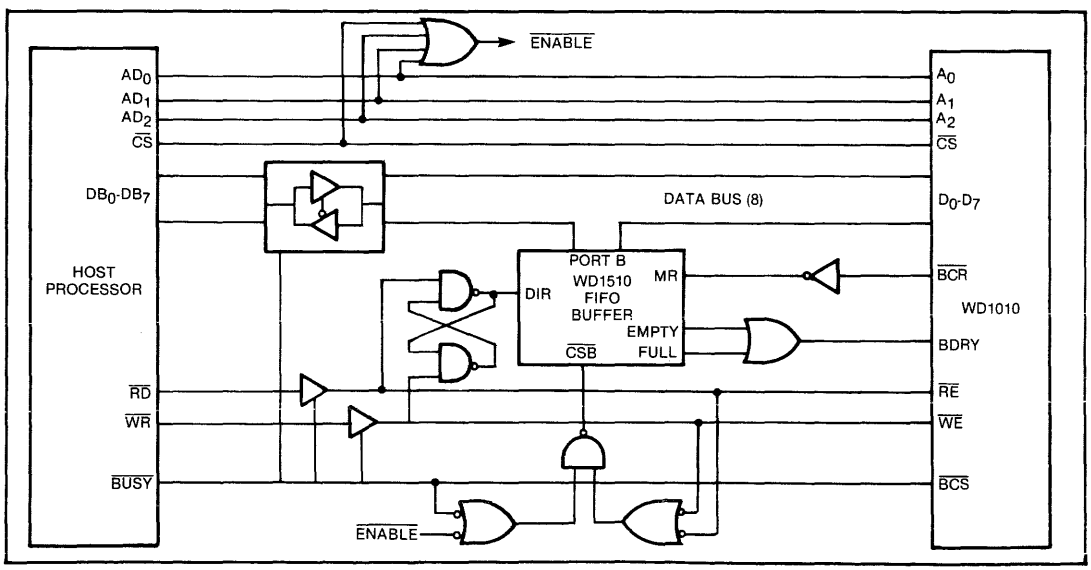


Figure 5.

A variation on the circuit of Figure 6 uses a WD1510 FIFO buffer to replace the counter-RAM circuitry. The scheme works well at high throughout rates since the buffer need not be filled to transfer data supplied by the WD1010 to the host.

bus and Read and Write lines from the WD1010. The Read ($\overline{RE}$) and Write ($\overline{WR}$) lines become outputs from the WD1010 and are strobed as each byte is placed on the bus.

The sector buffer in Figure 6 is implemented with a binary counter and a static RAM. With each $\overline{RE}$ or $\overline{WE}$ strobe, the counter is incremented so that the following byte can be read from or written to the next sequential location in the RAM. After all memory locations are written to, a carry signal from the counter goes to the Buffer Ready (BRDY) line of the WD1010. This signal informs the controller that the counter has rolled over and that the buffer is either full or empty, depending on the command.

During multiple-sector transfers, the RAM can be as large as the available sectors on each cylinder. The controller continues to load the RAM with data when a sector is being read. When no more memory is available. BRDY signals the WD1010. The command will then pause, wait for the host to dump the memory, and then begin filling the RAM again. This scheme permits both read and write operations on multiple sectors.

Signals for host and buffer control include the Buffer Counter Reset ($\overline{BCR}$) line, which is pulsed when $\overline{BCS}$ makes an active transition. $\overline{BCR}$ resets the binary counter before a read or write operation. Since address location 000 does not exist in the WD1010, a decoder can be used to make this address location enable the RAM and simulate a data register. For DMA applications, the Buffer Data Request (BRDQ) line is activated when data is available for host use.

Numerous other methods can be used with these same control signals. For example, a first-in, first-out buffer (Figure 7) can replace the counter-RAM. In this scheme, the host can dump data before the WD1010 fills the buffer. With sufficient throughput, the FIFO buffer need not have the storage capacity of an entire sector if the host can empty it quickly enough with a burst mode. In that case, the BRDY signal becomes the OR function of the Empty and Full signals from the FIFO buffer.

MACRO COMMANDS PROVIDE MULTIPLE OPTIONS

Each of the WD1010 Winchester controller-formatter's six macro commands contains several option flags. These flags allow the selection of stepping rates, multiple-sector transfers, and interrupt timing. The WD1010's task file contains additional options that are programmed before the command is actually issued. The operations of each command are as follows:

Restore causes the read/write head assembly to move to track 000. The stepping rate is determined by the state of Seek Complete (pin 32), which is activated by the drive to indicate its readiness. The stepping rate specified in the Restore command is not actually used but retained internally for an implied seek later on.

Activation of a Seek causes a seek operation for any desired cylinder. The selected cylinder is loaded into the cylinder register. Then the controller decides which way to seek and how many steps to use. The Seek Complete line is not checked, making possible overlapping seek operations on several drives.

The actual transfer of data from the WD1010 to sector buffer is performed under the Read Sector command. This command also causes a search for the specified cylinder, drive, head, and sector. Multiple sectors are specified and enabled through the sector count register. If the multiple-option flag is set, the number of sectors specified are transferred to the buffer.

Data in the sector buffer is written on the disk under the Write Sector command. Like the Read Sector command, it specifies and enables multiple drives through the sector count register.

Both the Read and Write Sector commands will retry up to eight times before automatically performing a restore operation. After a restoration, the controller seeks out the marginal sector and tries to determine whether an error condition was caused by a mispositioning of the head or a problem in the actuator.

The Format command is used to initialize a track with ID fields, gaps, and all information necessary for subsequent read and write operations. The sector buffer plays a unique role in this command, since it provides information on error mapping and inter-leaving rather than data from a sector. The order in which each sector is to be recorded is specified in the buffer, together with information indicating whether a sector contains a bad block or an error flag. Gap sizes, number of sectors, and other information are specified in the task file to allow further control over the format. By incrementing the cylinder number register, an entire surface can be formatted by accessing just two registers.

THE WD1010'S MACRO COMMANDS

	CODE							
	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R_3	R_2	R_1	R_0
Seek	0	1	1	1	R_3	R_2	R_1	R_0
Read Sector	0	0	1	0	1	M	0	0
Write Sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0

M = Multiple Sector Flag

M = 0 — transfer 1 sector
M = 1 — transfer multiple sectors

I = Interrupt Enable

I = 0 — Interrupt at BDRQ time
I = 1 — Interrupt at end of command

A MULTIPLE-DRIVE SYSTEM

For multiple drive-head configurations, the WD1010's sector-drive-head (SDH) register is decoded at address 110 to produce individual, latched drive-selection signals whenever the host writes to this address location. Binary head selection does not require a separate decoder, since one is located at the drive.

When the WD1010 senses a change in drive number, it automatically reads a cylinder. This takes place before the execution of the current command. The chip records the new cylinder number it has read and stores it internally as a reference for future seek operations on the current drive.

After the execution of any command, the WD1010 informs the host processor of any errors encountered during execution. On-board status and error registers report error conditions and signal status from the drive. To eliminate tedious error detection procedures, the host processor need only check the error bit in the status register to determine whether any bits are set in the error register.

Bit 0 of the status register is set if any of 5 bits in the 8-bit error register are set — bit 0 establishes the logical OR of the status register. Other error indicators include a Bad Block Detect bit, which is activated when an ID field contains a bad block mark, and an ID Not Found bit, which is set when the desired cylinder, head, sector, or size parameter is not found after 16 revolutions of the disk. The latter is also set if the data address mark of the data field is incorrect when a read is executed.

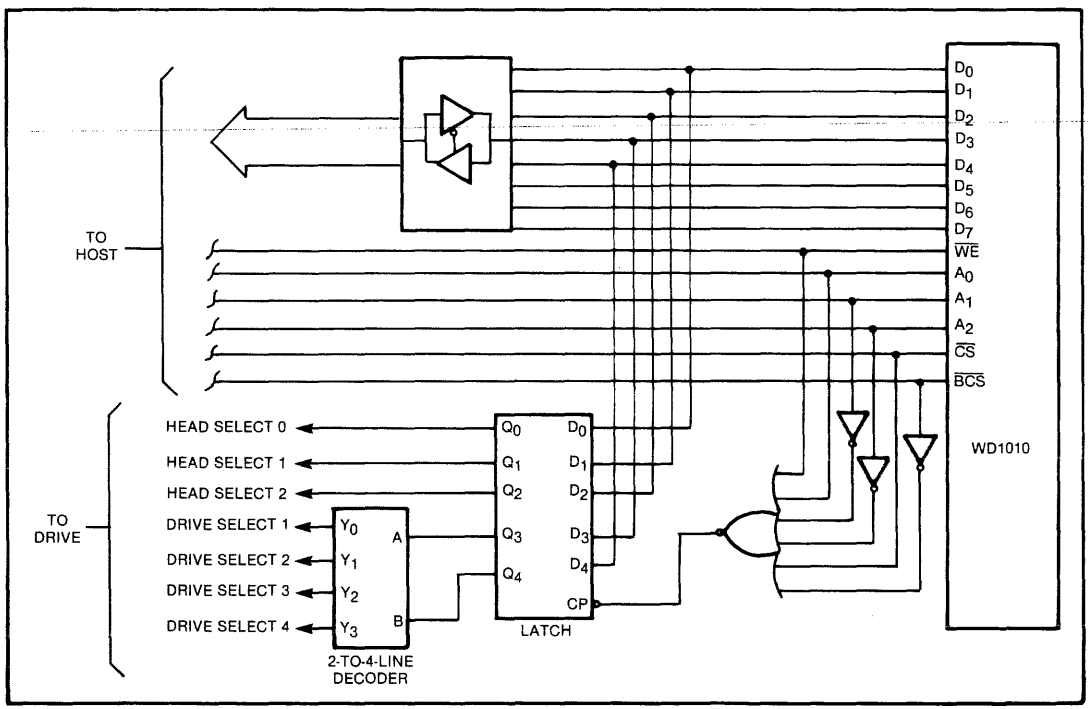


Figure 6.
Four Winchester drives can be controlled by the WD1010 using an external latch and a 2-to-4-line decoder. If the drive being accessed changes, the controller performs an automatic read operation. It records the cylinder number of the read for future seeks.

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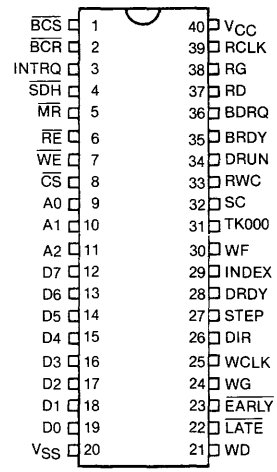
ADVANCED INFORMATION

WD2010 Winchester Disk Controller

FEATURES

- COMPATIBLE VIA 8-BIT DATA BUS WITH MOST MICROPROCESSORS
- UP TO 5 MBITS/S DATA RATE WITH AUTOMATIC ERROR CORRECTION
- MULTIPLE SECTOR READ/WRITE COMMANDS
- FORMATTING AND SECTOR INTERLEAVE CAPABILITY
- SEEK COMBINED WITH READ/WRITE COMMANDS
- SINGLE OR MULTIPLE SECTOR BUFFER USING FIFO OR RAM/COUNTER
- BUFFER ACCESS VIA PROGRAMMED I/O OR DMA
- 32 BIT ECC OR 16 BIT CRC SELECTABLE
- SELECTABLE 128, 256, 512, OR 1024 BYTE LENGTH SECTORS
- PROGRAMMABLE RETRY ALGORITHM
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD2010 Winchester Disk Controller is a single chip controller designed for use with the Shugart Associates SA1000 8" Winchester disk drive or the Seagate Technology ST506 5.25" Winchester disk drive. The WD2010 is designed to be software compatible with the WD1010. The WD2010 will read or write MFM data at a rate of up to 5 Mbits per second, with selected parts at a rate of up to 10 Mbits per second.

The WD2010 interfaces directly with TTL logic, is packaged in a 40-pin DIP, and requires only a single +5V supply. The WD2010 is designed to operate with an external sector buffer memory, or with an external DMA controller. Data bytes are transferred to or from the buffer every 1.6 usec. with a 5 Mbit per second drive. The buffer may consist of either a WD1510 128x9 FIFO memory, or a combination of a 256x8 static RAM and an 8-bit resettable counter. The WD2010 generates counter control signals to minimize external gating. Buffer to CPU transfers may be made via programmed I/O or DMA. The WD2010 also generates handshake signals to control DMA operation for multiple sector transfers.

A 32-bit ECC (Error Correction Code) polynomial or a 16-bit CRC polynomial may be selected. If a RAM/Counter sector buffer is used, the WD2010 can be programmed to automatically access the sector buffer and correct the data in error.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing of the external sector buffer.
2	BUFFER COUNTER RESET	$\overline{BCR}$	Active low output that is strobed by the WD1010 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
3	INTERRUPT REQUEST	INTRQ	Active high output which is set to a logic high in the completion of any command.
4	SDH LATCH ENABLE	$\overline{SDH}$	Provides a latch enable signal when the SDH register is addressed.
5	MASTER RESET	$\overline{MR}$	A logic low in this input will initialize all internal logic.
6	READ ENABLE	$\overline{RE}$	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	WRITE ENABLE	$\overline{WE}$	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
8	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
9-11	ADDRESS 0 - ADDRESS 2	A0-A2	These three inputs select the register to receive/transmit data on D0-D7.
12-19	DATA 7 - DATA 0	D7-D0	Eight bit bidirectional bus used for transfer of commands, status, and data.
20	GROUND	V_{SS}	Ground.
21	WRITE DATA	WD	This output contains the MFM clock and data pulses to be written on the disk.
23, 22	LATE, EARLY	$\overline{LATE}$, $\overline{EARLY}$	Precompensation outputs used to delay the WD pulses externally.
24	WRITE GATE	WG	This output is set to a logic high before writing is to be performed on the disk.
25	WRITE CLOCK	WC	4.34 or 5.0 Mhz clock input used to derive all internal write timing.
26	DIRECTION	DIR	This output determines the direction of the stepping motor.
27	STEP PULSE	STEP	This output generates a pulse for stepping the drive motor.
28	DRIVE READY	DRDY	This input must be at a logic high in order for commands to execute.
29	INDEX PULSE	INDEX	A logic high on this input informs the WD1010 when the index hole has been encountered.
30	WRITE FAULT	WF	An error input to the WD1010 which indicates a fault condition at the drive.
31	TRACK 000	TK000	An input to the WD1010 which indicates positioning over track 000.
32	SEEK COMPLETE	SC	This input informs the WD1010 when head settling time has expired.
33	REDUCED WRITE CURRENT	RWC	This output can be programmed to reduce write current on a selected starting cylinder.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
34	DATA RUN	DRUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
35	BUFFER READY	BRDY	This input is used to inform the controller that the sector buffer is full or empty.
36	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the sector buffer.
37	READ DATA	RD	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
38	READ GATE	RG	This output is set to a logic high when data is being inspected from the disk.
39	READ CLOCK	RC	A nominal square wave clock input derived from the external data recovery circuits.
40	+5 VOLT	V_{CC}	+5V ±5% Power supply input.

See page 481 for ordering information.

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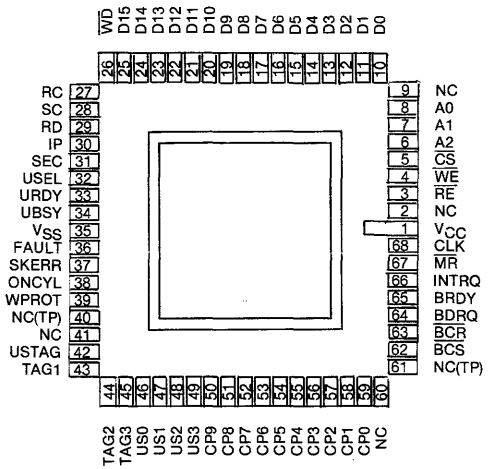
PRELIMINARY

WD1050 SMD Controller/Formatter

FEATURES

- 16 BIT HOST INTERFACE
- 9.677 MBITS/SEC DATA RATE
- SINGLE/MULTIPLE SECTOR TRANSFERS
- FIXED SECTOR FORMAT
- TTL COMPATIBLE INPUT/OUTPUTS
- SINGLE 5V SUPPLY
- 68 PIN JEDEC TYPE C CHIP CARRIER PACKAGE
- COMPATIBLE WITH SMD, MMD, FHT, LMD, AND CMD FAMILIES
- SINGLE +5V SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1050 SMD controller/formatter is a MOS/LSI device designed to interface an SMD compatible rigid disk drive to a host processor. The device is compatible with all rigid disk drives adhering to Control Data Corporation's flat cable interface for SMD, MMD, FHT, FMD, LMD and CMD families (CDC specification 64712400 Rev H). It is TTL compatible on all inputs and outputs, with interface capability for 8 or 16 bit data busses.

The WD1050 contains a powerful set of macro-commands for read/write and control functions. An internal 16 bit task file is used to process a selected command based upon parameter information in the file.

The WD1050 operates from a single +5V supply and is available in a 68 pin JEDEC Type C chip-carrier package.

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
1	V_{CC}	V_{CC}	+5V ±5% power supply input
2	NO CONNECTION	NC	
3	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	Tri-state bidirectional line, used as an input when reading the task file and an output when the WD1050 is reading from the buffer.
4	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	Tri-state bidirectional line used as an input when writing to the task file and an output when the WD1050 is writing to the buffer.
5	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals as inputs.
6-8	ADDRESS 0-2	A_0-A_2	These three inputs select a task file register to receive/transmit data.
9	NO CONNECTION	NC	
10-25	DATA BUS 0-15	D_0-D_{15}	Sixteen bit bidirectional bus used for transfer of commands, status, and data.
26	$\overline{\text{WRITE DATA}}$	$\overline{WD}$	Open drain, NRZ data output which is synchronized to the Servo Clock input.
27	READ CLOCK	RCLK	Input clock from the drive which is synchronized with the Read Data Input.
28	SERVO CLOCK	SCLK	A nominal 9.677 MHz clock input from the drive. This clock must be valid when Unit Ready (Pin 31) is active and Fault (Pin 34) is inactive.
29	READ DATA	RD	NRZ data input from the drive which must be synchronized to the Read Clock (Pin 25) input.
30	INDEX PULSE	IP	Active high input used to monitor the Index signal from the drive.
31	SECTOR	SEC	Active high input used to monitor sector pulses from the drive.
32	UNIT SELECTED	USEL	Active high input used to verify the selected drive.
33	UNIT READY	URDY	Active high input used to inform the WD1050 of a ready condition on a selected drive. If this line is made inactive during any command (except RTZ or FAULT CLEAR), command execution is terminated.
34	UNIT BUSY	UBSY	Active high input used to monitor drive status during a unit selection. If the unit had previously been selected and/ or reserved prior to issuing a USTAG, the UBSY must be made active within one microsecond of the USTAG selection. This signal is used for dual-channel access applications and should be tied to ground when not used.
35	GROUND	V_{SS}	Ground.
36	FAULT	FAULT	Active high input used to detect a fault condition at the drive. Command execution is terminated if Fault is made active during any command. Only the FAULT CLEAR command may be issued while this line is asserted.

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
37	SEEK ERROR	SKERR	Active high input used to detect a seek error at the drive.
38	ON CYLINDER	ONCYL	Active high input used to inform the WD1050 when the heads are settled and positioned over a cylinder.
39	WRITE PROTECT	WPROT	Active high input used to monitor the Write Protect signal from the drive.
40	NO CONNECTION	NC(TP)	Test point.
41	NO CONNECTION	NC	
42	UNIT SELECT TAG	USTAG	Active high output used for selection of a unit on US0-US3 lines.
43-45	TAG1-TAG3	TAG1-TAG3	Active high outputs used to strobe specific data out on the Control Port Lines. Tag definitions are: TAG1 — Cylinder address TAG2 — Head/Volume select TAG3 — Control Tag
46-49	UNIT SELECT 0-3	US0-US3	These four outputs reflect the contents of the unit address field of the task file and are used to select one of 16 drives.
50-59	CONTROL PORT BITS 9-0	CP9-CP0	Ten bit output bus used to issue tag parameters to the selected drive.
60	NO CONNECTION	NC	
61	NO CONNECTION	NC(TP)	Test point.
62	$\overline{\text{BUFFER CHIP SELECT}}$	$\overline{\text{BCS}}$	Active low output used to enable reading or writing to the external buffer by the WD1050.
63	$\overline{\text{BUFFER COUNTER RESET}}$	$\overline{\text{BCR}}$	Active low output that is strobed prior to read/write commands. Used to clear an external buffer counter.
64	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the external buffer.
65	BUFFER READY	BRDY	This input informs the WD1050 that the buffer is either full or empty.
66	INTERRUPT REQUEST	INTRQ	Active high output which is set at the completion of any command, providing the 'I' bit is also set in the command word. INTRQ is reset subsequent to a Status register read.
67	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	Active low input used to initialize the WD1050, usually after a power-up condition.
68	CLOCK	CLK	2 MHz Master Clock is input.

FUNCTION DESCRIPTION

The WD1050 SMD Winchester Controller performs the necessary link between an 8 or 16 bit processor and an SMD compatible drive. The internal architecture of the WD1050 is shown in Figure 1. The major functional blocks are:

Control Unit

This section decodes commands, implements command execution sequencing, monitors the comparator and CRC logic, monitors status and issues control to the Host and Drive Interfaces. It also writes appropriate information to the Status register during command execution.

Data I/O Buffers

A 16-bit bi-directional three-state bus (D15-D0) for data transfers between the host CPU or data buffer and the HDC. (The higher order 8-bits of this bus [D15-D8] may be used for 8-bit data bus transfers between the host CPU and the HDC).

Host/Buffer Control

This section allows HDC register selection and communication by the CPU, issues interrupt requests, and provides Direct Buffer Access (DBA) transfers between the disk drive and the data buffer.

Status Register

A 16-bit register reflecting operational status of the HDC and disk drive. This is a read-only register.

Command Register

A 16-bit field containing command information that dictates operational control sequencing of the Host and Drive Interfaces by the HDC. This is a write-only register.

Data Register

A 16-bit field used to assemble/disassemble words/bytes during data transfers. This register is internally interfaced to the HDC's Data I/O Buffers ('D' bus) and the HDC's Read Data Holding (RDH) register or Write Data Holding (WDH) register (as appropriate) during host/drive data transfers. The contents of this register are compared to the appropriate Task File field as required by command execution.

CRC Logic

This logic is used to generate or check the 16-bit Cyclic Redundancy Check (CRC). The polynominal is:

$$G(x) = X^{16} + X^{12} + X^5 + 1$$

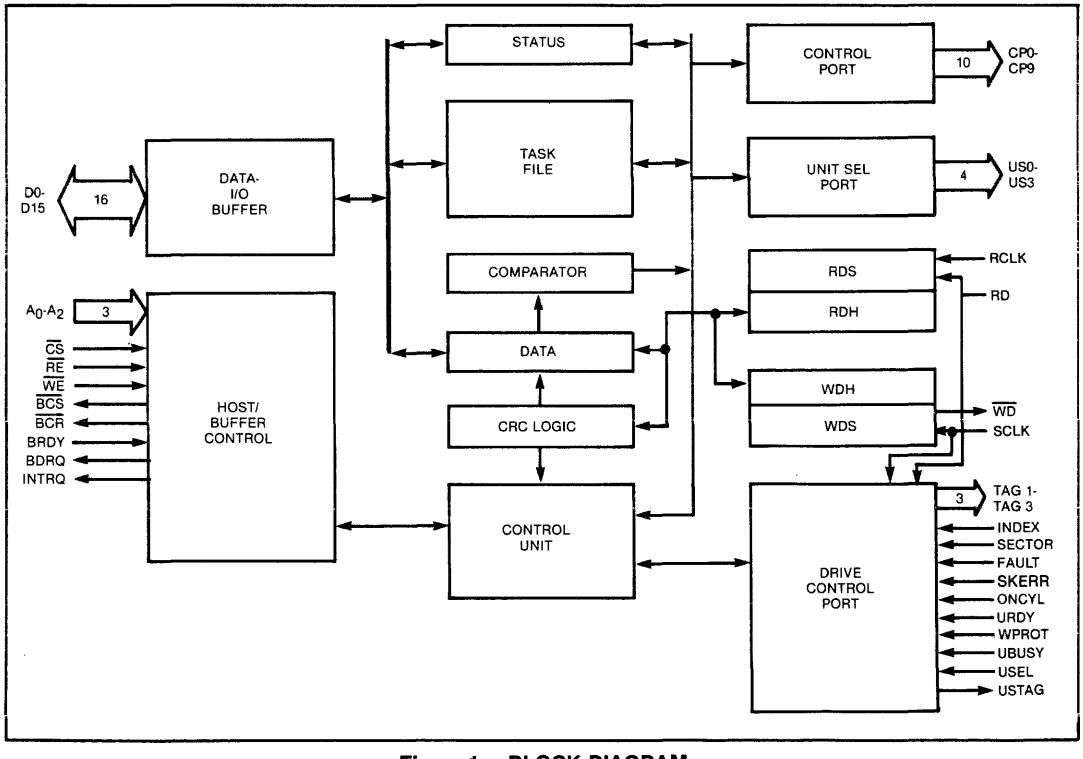


Figure 1. BLOCK DIAGRAM

The CRC includes all information beginning with the Sync character and ending with the CRC word. The CRC is preset to ones prior to a data transmission.

The CRC is implemented in parallel eight bits at a time as data is transferred between the HDC's Data register and the HDC's Read or Write Data Holding registers. The CRC word is transferred to the HDC's Data register and appended to the ID Field and Data Field (if enabled) during Format Sector or Write Data Commands.

Comparator

A 16-bit comparator used to compare the appropriate HDC's Task File field with the respective byte(s) read from the disk.

Read Data Shift Register (RDS)

This 8-bit register shifts data read from Read Data (RD) input via the drives Read Clock (HDC's RCLK input).

Read Data Holding Register (RDH)

This 8-bit holding register assembles bytes from the Read Data Shift register and transfers them to the Data register.

Write Data Holding Register (WDH)

This 8-bit holding register receives bytes from the Data register and provides an eight bit parallel input to the HDC's Write Data Shift register (WDS).

Write Data Shift Register (WDS)

This 8-bit shift register converts the eight bit parallel input from the Write Data Holding register (WDH) into a serial bit stream issued to the HDC's Write Data ($\overline{WD}$) output via the drive's Servo Clock (HDC's SCLK input).

Drive Control

This section monitors drive status, synchronizes the byte boundries generated by the Serve Clock to the sync character read from the disk or the drive's Index or Sector pulse as appropriate, and issues control tags to the drive.

Control Port (CP0-9)

This 10 bit output port is used to provide the drive with volume/head #, cylinder address, and control information in conjunction with outputs Tag 1 (cylinder address), Tag 2 (volume/head #), and Tag 3 (control). The contents of the appropriate HDC register or signals generated from the Control Unit are gated to the Control Port during command execution.

Unit Select Port (US0-3)

This 4-bit output port reflects the contents of the Unit Address register, respectively. The Unit Select Tag output selects the desired disk drive unit.

HOST INTERFACE

The primary interface between the Host processor and the WD1050 is through a 16-bit bi-directional bus. This bus is used to transfer status, parameter, and command information between the WD1050 and the host, as well as data between the WD1050 and sector buffer. The external sector buffer is constructed with either FIFO memory or a RAM and binary counter. Since the WD1050 will make this bus active when accessing the sector buffer, a transceiver must be used to isolate this bus from the host. Figure 2 shows a typical Host Interface using a RAM and Binary counter. The sector buffer may be one or more sectors in length, depending upon system requirements.

Whenever the WD1050 is not using the sector buffer, the Buffer Chip Select ($\overline{BCS}$) is high (disabled). This allows the Host to access the WD1050's Task File, read status, and issue commands. It also allows the host to access data within the sector buffer. A separate RAM select line from the host is used to access the data in memory. With each $\overline{RE}$ or $\overline{WE}$ strobe from the host, the address counter is incremented on the trailing edge of $\overline{RE}$ or $\overline{WE}$, pointing to the next sequential memory location. Whenever the WD1050 changes the state of $\overline{BCS}$, the Buffer Counter Reset ($\overline{BCR}$) Line is strobed, causing the address counter to be reset to zero. The $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1050 to allow access to the buffer only when $\overline{BCS}$ is low. Although 8-bit programming is allowed via the use of Address Line 0, the data path to and from the WD1050 must be 16 bits wide.

TASK FILE

The WD1050 contains five 16-bit registers called the Task File. These registers are used to set up parameter information prior to issuing a command. These registers are:

A2	A1	A0	15 REGISTER 0
0	0	0	HEAD/SECTOR ADDRESS
0	1	0	SECTOR COUNT/LENGTH & UNIT ADDRESS
1	0	0	CYLINDER REGISTER
1	1	0	COMMAND REGISTER (WRITE ONLY)
1	1	0	STATUS REGISTER (READ ONLY)

Each register in the Task File is accessed by selecting the proper address while $\overline{CS}$ (pin 4) is low, then strobing the $\overline{WE}$ or $\overline{RE}$ lines. All registers in the Task File are Read/Write except for the Command/Status register. The Command register can only be written to, while the Status register is a read-only register. But the command and status registers have the same address.

An 8-bit mode can also be used for accessing the Task File. Data is read/written on the most significant

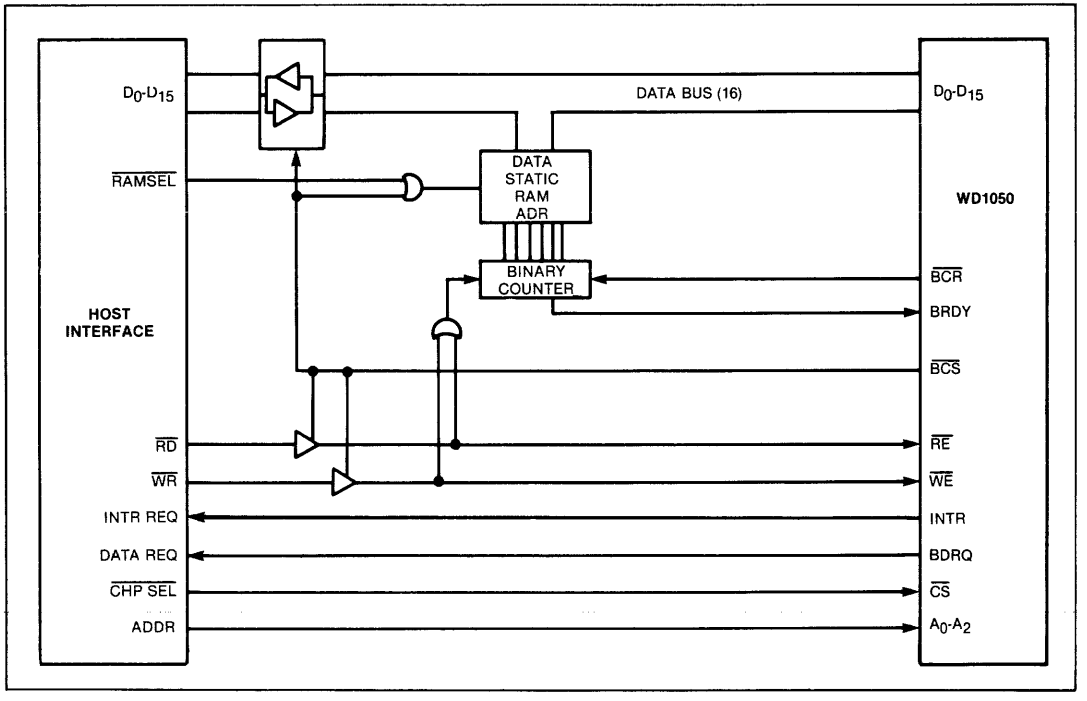
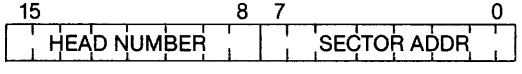


Figure 2.

8-bits of the Data bus (D15-D8). The upper byte is accessed when A_0 (pin 7) is high, and the lower byte is accessed when A_0 is low. The upper byte ($A_0 = 1$) must be accessed first, followed by the lower byte. This insures that data is transferred to the internal 16 bit bus properly, and that a command will execute when the full 16 bit word is written.

Head/Sector Address

This register holds the Head number and sector address fields:



The Sector Address byte (bits 7-0) holds the logical sector number used for comparison when searching for the specified ID field. The Head number byte (bits 15-8) hold the logical head number, and volume flag (where applicable). This 8 bit field is sent to the drive via the Control Port (CP7-0) when Tag 2 is issued. Note that all 8 bits of each byte are written into the ID field during formats and are compared during other commands.

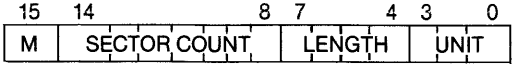
Cylinder Register

This Register holds the 16 bit cylinder number:

The least significant 10 bits of this register (bits 9-0) are transferred to the Control Port (CP9-0) when Tag 1 is issued. All sixteen bits of this register are written to the ID field during formats and are compared during other commands.

Sector Count/Length & Unit Address

This register holds the sector count, sector length and unit address fields:



The four bit unit address field (bits 3-0) contains the physical unit address and is reflected at the drive via the Unit Select Port (US3-0). This port is used in conjunction with the Unit Select Tag (USTAG) output to select the desired drive.

The four bit sector length field is used to determine the number of bytes to be read/written from the disk. The allowable sector lengths are:

BITS 7	6	5	4	# OF BYTES IN DATA FIELD
1	0	0	0	128
0	1	0	0	256
0	0	1	0	512
0	0	0	1	1024

If the CE bit (CRC Enable) in the command word is zero, an additional 8 bytes are added to the above sector lengths (and the CRC bytes are not appended to the data field). These bytes can be used to append ECC codes to each sector.

The Sector Count Field, seven bits of which (bits 14-8) are used to control single/multiple record operation for commands where the LS (Logical Sector) Flag is set, is decremented by one for each sector encountered after the desired sector has been located on the disk. The Op Code command is repeated until the contents of this field (bits 14-8) are equal to zero. For single sector operation, this field (bits 14-8) must equal "0000000." (This field [bits 14-8] is ignored for the Fault Clear command).

For the Format Sector, Verify Sector, and commands where the LS flag is not set, the Sector Count Field (bits 14-8) must contain the desired physical sector location (i.e., the Sector Count number of sector pulses from the Index pulse = physical sector location). This register is counted down to zero to determine the physical sector location for these commands. For physical sectored commands, bit 15 is used as a one bit field controlling single/multiple record operation. For bit 15 equal to '0', a single sector command is executed. For bit 15 equal to '1', these commands are repeated until the Index pulse is re-encountered, allowing multiple sector operations.

For logical sectoring, bit 15 of this register should equal '0.'

Command Register

This "write-only" register is used to load in the desired command:

The command register may be loaded whenever the Command-In-Process (CIP) status bit is reset.

Status Register

This "read-only" register is used to monitor status and error conditions as the result of command execution. Its format is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCS	CIP	UBSY	USEL	WPRT	URDY	OCYL	SKER	BCS	FLT	BDRQ	—	DFCE	DFNF	IDCE	IDNF

BIT	NAME	DESCRIPTION
0	ID Field Not Found (ID/NF)	Set if the sync character preceding the ID Field or ID Field contents read from the disk do not match the respective Task File contents.
1	ID CRC Error (IDCE)	Set if the CRC calculation on the ID Field read from the disk is in error.
2	Data Field Not Found (DFNF)	Set if the Data Field sync pattern following the ID Field does not match the sync character.
3	Data Field CRC Error (DFCE)	Set if the CRC Calculation on the Data Field read from the disk is in error.
4	Not Used	This bit is not used; it is forced to a zero.
5	Buffer Data Request (BDRQ)	Reflects the Buffer Data Request output.
6	Fault (FLT)	Reflects the status of the Fault (Flt) input.
7	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output.
8	Seek Error (SKER)	Reflects the status of the Seek Error (Sk Er) input.
9	On Cylinder (OCYL)	Reflects the status of the On Cylinder (On Cyl) input.
10	Unit Ready (URDY)	Reflects the status of the Unit Ready (U Rdy) input.
11	Write Protect (WPRT)	Reflects the status of the Write Protect (WPRT).
12	Unit Selected (USEL)	Reflects the status of the Unit Selected (U Sel) input.
13	Unit Busy (U Bsy)	Reflects the status of the Unit Busy (U Bsy) input.
14	CIP	Set when a command is in progress.
15	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output. This bit also appears in STATUS Bit 7.

INSTRUCTION SET

The WD1050 will execute eight commands. Prior to issuing a command, the Host must first setup the Task File with parameter information. A command can only be accepted if the CIP bit in the status register is reset.

COMMAND	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
	COMMAND REGISTER BITS															
Fault Clear	1	0	0	0	0	0	0	I	0	0	0	0	U	S	E	D
Return to Zero	1	0	0	1	0	0	0	I	0	0	0	M	U	S	E	D
Seek Cylinder	1	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	D
Read ID Field	1	0	1	1	R	L	O	I	Z	C	H	M	U	S	E	D
Read Sector	1	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	D
Write Sector	1	1	0	1	R	L	O	I	Z	C	H	0	U	S	E	D
Format	1	1	1	0	R	P	O	I	Z	C	H	0	U	S	E	D
Verify	1	1	1	1	R	P	O	I	Z	C	H	M	U	S	E	D

FLAG SUMMARY

V	= Verify	I	= Interrupt Enable
R	= CRC Enable	Z	= Volume/Head Change
L	= Logical Sectoring	C	= Cylinder Addr
P	= Programmable Sectors	H	= Head Selection
O	= On Cylinder	M	= Marginal Data Recovery
E	= Priority Release/Early	U	= Unit Sel/Servo Minus
D	= Unit Deselect/Late	S	= Priority Sel/Servo Plus

COMMAND FLAG DESCRIPTION

FLAG	NAME	DESCRIPTION
V	Verify	Compare the Head number and Cylinder Address word of the ID field with the appropriate Task File field when On Cylinder becomes active. The Sector Address byte in the ID Field is not compared, although the CRC is checked. This flag is valid only for the Seek Cylinder command.
R	Data Field CRC Enable	Data Field CRC is enabled. If the flag is **not** set, the condition of the DFCRC Status bit will not affect command execution; the data field is extended by four words (8 bytes), and the CRC bytes are not appended.
L	Logical Sectoring	Locate sector by matching the ID Field bytes read from the disk to the appropriate field in the HDC Task File. The Sector Count register in the Task File is used to indicate the additional number of sectors to be transferred for multiple sector commands. If L is **not** set, physical sectoring is implemented. The Task File Sector Count register is decremented to locate the desired physical sector from the Index pulse. ID Field compares are made, but do not affect command execution.
P	Programmable Sectors	The Head Number/Sector Address register is read from the buffer as each sector is encountered per command execution. (This allows an entire track to be formatted/verified with interleave sectors in one revolution of the disk). This flag is valid only for the Format Sector or Verify Sector commands.
O	On Cylinder	For the Seek Cylinder command, command completion requires activation of On Cylinder or Seek Error inputs. For other commands, On Cylinder is required before a read or write can occur.
I	Interrupt Enable	Enable the interrupt output (INTRQ) for activation upon completion or termination of command execution.

COMMAND FLAG DESCRIPTION

FLAG	NAME	DESCRIPTION
Z	Volume/Head	Issue Tag 2 as required for volume/head change.
C	Cylinder	Issue Tag 1 as required for cylinder address selection. (Tag 1 will follow Tag 2 if the Z and C flags are both set).
H	Head	Issue Tag 2 as required for head selection. (Tag 2 will follow Tag 1 if the C and H flags are both set).
M	Marginal Data	Attempt a marginal data recovery. (Marginal data recovery may be attempted only where a command requires reading from the drive).
		This bit controls the function of bits 3-0 (U, S, E, D). (See Note 1).
U	Unit Select/Servo Offset Minus	For M = 0 (or not applicable), set Unit Select Tag as required for unit selection. Unit Selected must become active for command execution to continue.
		For M = 1, issue servo offset minus control for marginal data recovery attempt.
S	Priority Select/ Servo Offset Plus	For M = 0, issue priority select control as required to reserve the unit. (See Note 2).
		For M = 1, issue servo offset plus control for marginal data recovery attempt.
E	Priority Release/ Data Strobe Early	For M = 0, issue priority release control as required to release reserve of the unit. (See Note 2).
		For M = 1, issue data strobe early control for marginal data recovery attempt.
D	Unit Deselect/Data Strobe Late	For M = 0, reset Unit Select Tag at completion of this command.
		For M = 1, issue data strobe late control for marginal data recovery attempt.

Note 1: Certain marginnal data recovery features are not applicable depending on the particular drive type under control. (Refer to CDC Interface Specification 64712400).

Note 2: Priority select and release features are applicable only for dual channel drive applications.

COMMAND EXECUTION

Command word architecture has been designed to provide comprehensive control of the drive unit via programmable micro-level commands. For example, unit selections, cylinder seek, head selection, Op Code execution (of multiple records if desired), and unit deselection can be performed with a single command.

Command execution follows the following sequence (for 'M' flag = 0):

1. If the U flag is set, the Unit Select (US) Tag is activated. (The drive should select the unit specified by the Unit Select bus [US0-3] when the US Tag is activated.)

   If the S flag is also set, CP9 will be active when the US Tag is activated (exclusively reserving the unit to that channel until released).

2. The following conditions must be met and maintained for command execution to continue:
   Unit Ready input active
   Unit Selected input active
   Unit Busy input not active

   If these conditions are not met, command execution is terminated with the appropriate bit set in the Status register.

   For all commands except the Fault Clear command, the Fault input must also be inactive and remain inactive for command execution to continue.

3. For the Write Data and Format Commands, the Write Protect Status bit is checked; if true command execution is terminated.

4. For the Write Data command, and the Format and Verify command with the P (programmable sector) flag set, the HDC activates BDRQ requesting the host to provide the required data to the buffer.

5. If the Z flag is set (indicating a volume change), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed. (Applies only for drives with volume select.)

6. If the C flag is set (indicating a cylinder address seek), the Cylinder Address field of the Task File is issued to the Control Port (bits 9-0 respectively), and Tag 1 is pulsed.

NOTE:
For the Seek Cylinder command, and for other commands where the On Cylinder flag is set, the On Cylinder input must be active before Tag 1 will be issued. (If the Seek Error input is active or becomes active before On Cylinder is active, execution is terminated with the Seek Error status recorded in the Status register.

7. If the H flag is set (indicating a head selection), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed.
8. For commands other than Seek Cylinder, O flag operation is as follows:

   If O is set, execution is suspended pending an active On Cylinder input.

   If O is not set, the command is executed regardless of the condition of On Cylinder.

   NOTE:
   Data transfer to/from the drive with On Cylinder inactive is allowed only under certain circumstances on specific drives. For example, on a drive with both fixed and moveable heads, it is possible to execute a Seek Cylinder command with the C flag not set to the moveable heads (On Cylinder will drop). The fixed heads may then be given a Read Data command with the O flag not set. The fixed head can then be read regardless of the condition of On Cylinder. (This is an overlap seek within a given unit between the fixed and moveable media). For valid read/write operation without an active On Cylinder, refer to the appropriate drive operating specification.

   For commands with C set and Seek Error received instead of On Cylinder, command execution is terminated.
9. For the Write Data command, and the Format and Verify commands with the P flag set, the BRDY input is inspected. Command execution is suspended pending reception of a low to high transition on the BRDY input.

   NOTE:
   For commands where M is set, marginal data recovery control as described in the chart below is issued to the control port prior to the activation of Tag 3. Note that unit selection, channel reserve control, and unit deselection must be accomplished with a non-marginal data recovery command since the U, S, E, and D flags assume marginal data recovery control significance.

MARGINAL DATA RECOVERY OPERATION

COMMAND FLAG IF MD IS SET	FEATURE	CONTROL PORT BIT ACTIVATED
U	Servo Offset Plus	2
S	Servo Offset Minus	3
E	Data Strobe Early	7
D	Data Strobe Late	8

Location of the appropriate sector within the cylinder is common to all commands except Fault Clear and RTZ. One of two methods is used: logical sector search (for commands where the L flag is set) and physical sector locating (for the Format and Verify commands and commands where the L bit is not set).

Logical sector search consists of reading the first encountered ID Field, comparing these bytes to the appropriate fields in the HDC's Task File, (including the sync byte) and checking the ID Field CRC bytes. When a valid compare with correct CRC are found, execution continues. If a valid compare with correct CRC are not found before four Index pulses are detected, the appropriate Status bits are set (IDNF and/or IDCE) and command execution is complete. For multiple sector commands, the Sector Address field of the Task File is incremented between sectors and the Sector Count field is used to indicate the number of additional sectors for which the command is to be executed. A single sector command is executed for Sector Count = '00 . . . 00'.

Physical sector locating is accomplished by decrementing the Sector Count field of the Task File by one for each Sector pulse encountered after the Index pulse is located until the Sector Count field = '0000000'. For Sector Count = '0000000', the command will be executed to the sector immediately following the Index pulse). The ID Field compares and the IDCE check are still made and the appropriate bit set in the Status register (if applicable), but command execution is not affected by an error condition. A single sector command is executed if bit 15 of the Sector Count/Sector Length/Unit Address register of the Task File is zero. If bit 15 is one, command execution is repeated until the Index pulse is re-encountered. Note that Status register error bits are not cleared between sectors (one's catching).

Tag 3 (Control Select) is activated for all commands except Seek Cylinder with the V flag not set.

When the appropriate Sector pulse is encountered, CPI (Read Gate) is activated and the HDC synchronizes to the first low to high transition on the Read Data (RD) input. This initiates the following three compares: the sync byte FE preceded by eight zeros, the upper and lower Cylinder Address, and the Head number and Sector Address. (The Sector Address compare is suppressed on the RTZ and Seek Cylinder commands). The ID FIELD CRC is then checked. CPI is deactivated and command execution follows.

FAULT CLEAR

CP4 (Fault Clear) is pulsed and this completes execution. This command is intended to clear the Fault output of the drive. The condition causing the fault within the drive should no longer exist when this command is issued.

RTZ (RETURN TO ZERO)

CP6 (RTZ) is pulsed and the Cylinder Address, Head

number, and Sector Address fields of the Task File are all set to zero. This completes execution.

SEEK CYLINDER

Execution of this command is controlled completely by the command flags. If O is set, execution is suspended until On Cylinder (or Seek Error) is received. If the V flag is not set, receipt of On Cylinder completes execution. If C and V are both set, and On Cylinder is received, CPI (Read Data) is issued and the ID Field is inspected. The Sector Address compare is not made for this command.

NOTE:
If L is set (logical sectoring), execution is complete when ID Field is successfully found or when the 4th Index pulse is encountered. There is no multiple sector operation when L is set for this command. If L is not set (physical sectoring), the IDNF and IDCE Status bit are one's catching. (The entire track may be verified with multiple sector operation).

The V flag is ignored if the O flag is not set.

If the C flag is not set, this command may be used for Unit Select only functions.

READ ID FIELD

The Read ID Field command is provided to allow transfer of the ID Field formatted on the disk to the data buffer (ie., $\overline{BCS}$ • D15-D0 • $\overline{WE}$ pulses). The Sector Address field is not compared in this command.

If the L flag is set, the first encountered ID Field is transferred to the buffer. The following bytes are transferred: 00FE, Upper and Lower Cylinder Address, Head number, Sector Address, and the two CRC bytes. Thus four $\overline{WE}$ pulses are issued.

If the L flag is not set, the physical sector is located and the corresponding ID Field is transferred to the buffer.

There are no retries with this command if ID Field compare errors result.

CP1 is then reactivated, and the first low to high transition on the RD input causes a compare for the Data Field sync character. If the compare does not match, the Data Field Not Found (DFNF) Status bit is set. The Data Field CRC (DFCE) Status bit is set if an error is detected. CP1 is then deactivated.

Note that the Data Field is not transferred with this command.

For multiple sector operation, the Sector Address Field of the Task File is automatically incremented. The BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (ie., buffer not full) execution is then repeated. If a low to high transition has occurred, (ie., buffer is full) $\overline{BCS}$ is deactivated, $\overline{BCR}$ is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition of BRDY (ie., buffer empty). $\overline{BCR}$ is then pulsed, and execution is repeated. If a Data Field CRC is detected, the command will not terminate.

READ DATA

After the appropriate sector has been located, Data Field operation is as described under the Read ID Field Command, except that the Data Field is transferred to the buffer. Note that only the Data Field data bytes are transferred with this command.

This completes execution for single sector commands and for multiple sector commands where the L and R flags are set. If a Data Field sync error (DFNF) or a Data Field CRC (DFCE) error has occurred, the command will also be terminated.

For multiple sector command where the C flag and/or L flag is not set, and for multiple sector commands where no Data Field error has occurred, execution is repeated.

Note that if the R flag and/or the L flag is not set, the DFNF and DFCE Status bits are one's catching.

WRITE DATA

After the appropriate sector has been located, CP0 (Write Gate) is activated. Thirteen bytes of zeros (two Write Splice bytes and eleven PL0 Sync bytes) are written followed by the sync character. The Data Field is then written to the disk from the data buffer (ie., $\overline{BCS}$ • D15-D0 • $\overline{RE}$ pulses). The CRC bytes and two bytes of zeros (End of Record) are appended to the Data Field and written to the disk.

For multiple sector operation, the BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (ie., buffer not empty), execution is then repeated. If a low to high transition has occurred (ie., buffer empty), $\overline{BCS}$ is deactivated, $\overline{BCR}$ is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition on BRDY (ie., buffer full). $\overline{BCR}$ is then pulsed, and execution is repeated.

FORMAT SECTOR

Physical sectoring only applies to the Format Sector command. Upon reception of the appropriate Sector pulse, CP0 (Write Gate) is activated. Twenty seven bytes of zeros (16 Head Scatter bytes and eleven PL0 Sync bytes), and the sync character are written to the disk. The four ID Field bytes are written to the disk from the HDC's Task File, and the resultant CRC is appended. Thriteen bytes of zeros are written (two Write Splice bytes and eleven PL0 sync bytes) followed by the sync character. The Data Field (Format Character E5 repeated) is then written. If the R bit is set, then the two CRC bytes are appended; if R is not set eight additional E5's are added to the data field. Zeros are written until the next Sector or Index pulse is encountered.

For single sector operations CP0 is then deactivated.

For multiple sector operation, CP0 remains active, and execution is repeated until the Index pulse is again encountered.

If the P flag is set, the HDC will fetch the Head number/Sector Address from the data buffer prior to encountering each ID Field. Thus, by filling the data buffer with the desired Head Number/Sector Address information, the HDC can format an entire track with any given programmed sector interleave in one revolution.

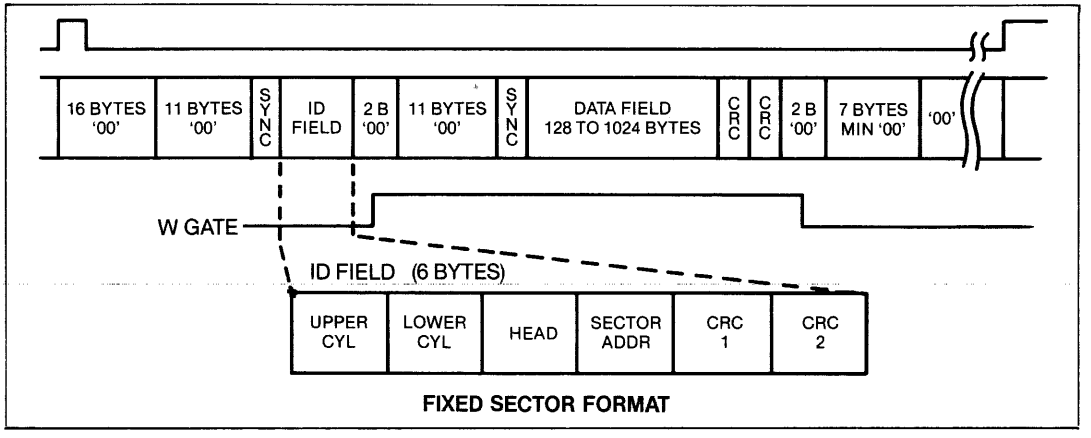
If the P flag is not set, the contents of the Sector Address field of the Task File will be incremented by one between sectors.

The $\overline{BCS}$ output will remain active for the duration of this command.

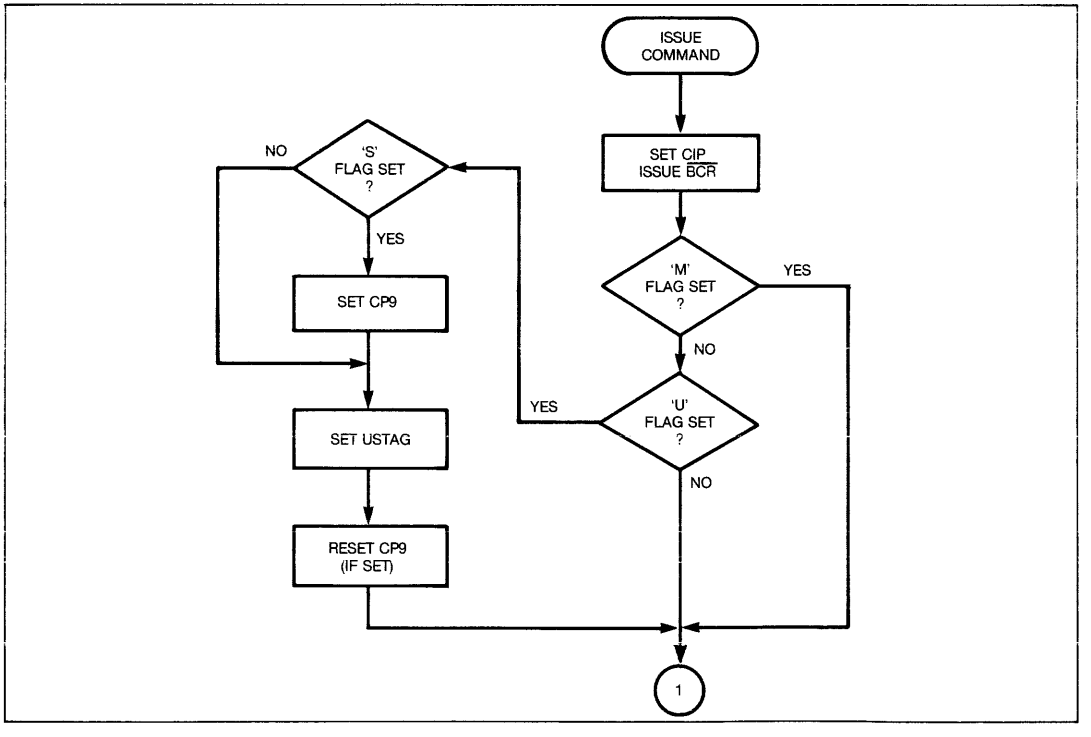
VERIFY SECTOR

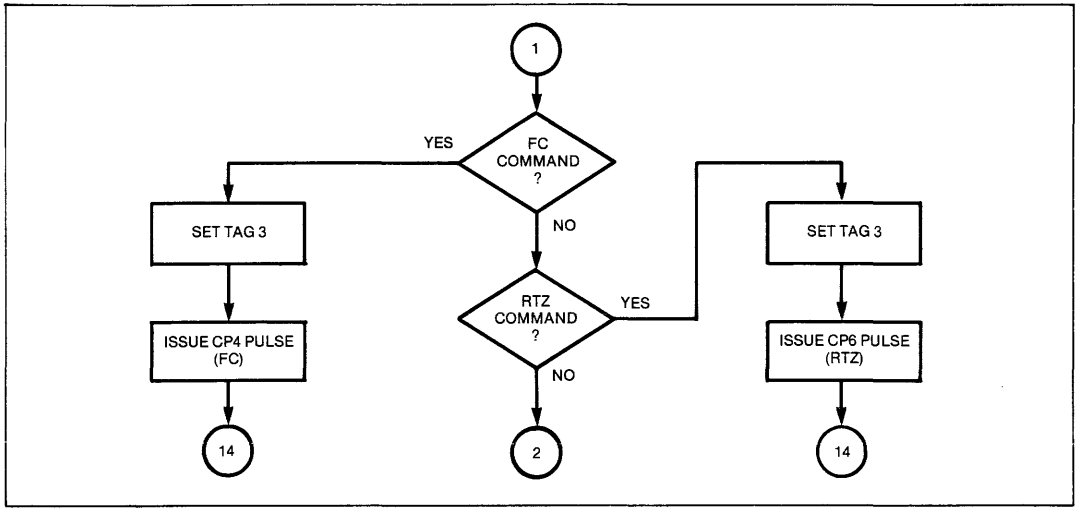
This command allows verification of sector format without transfer of data. Sector addressing is identical to that described for the Format Sector command. The IDNF, IDCE, DFNF and DFCE bits are set if errors are found (all bits are one's catching for multiple sector operation). With multiple sector operation, an entire track can be verified in a single revolution.

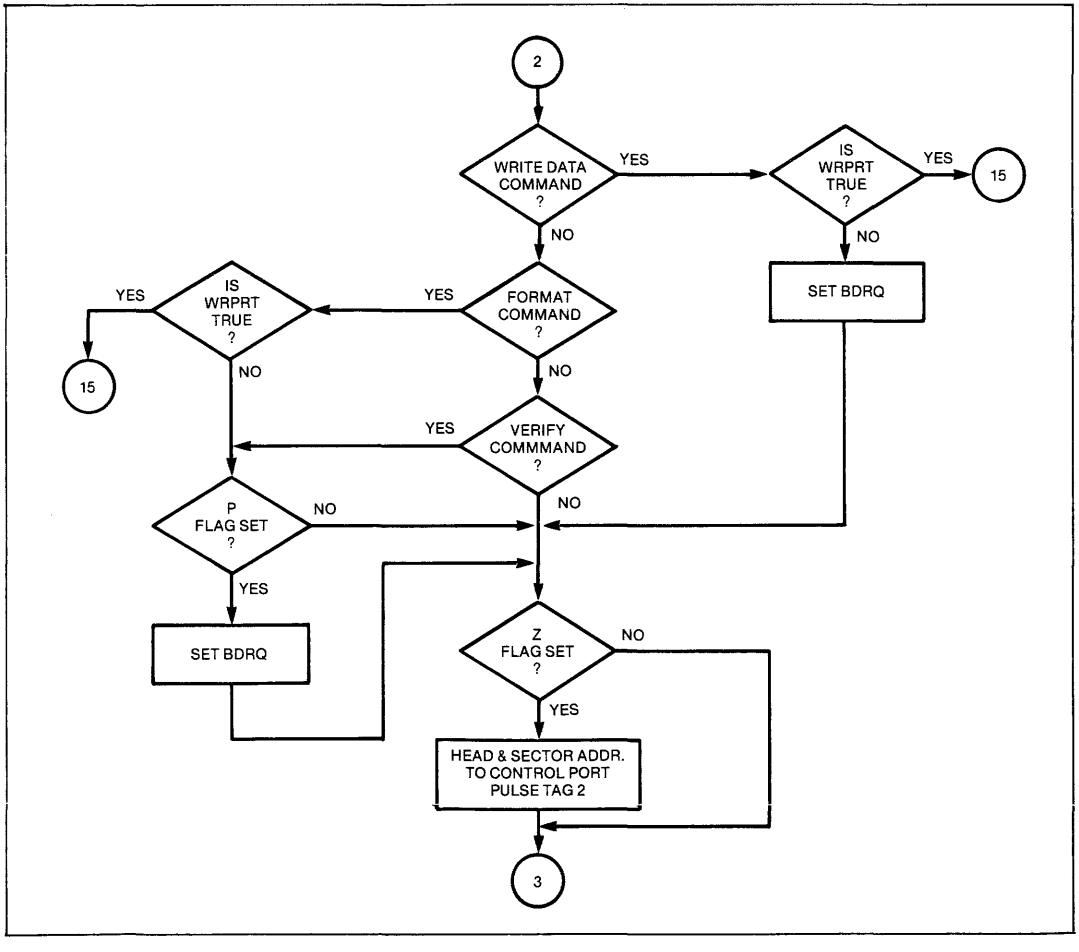
NOTE:
When used with the Lark drive, the validity of the DFCE bit is not guaranteed with this command if it immediately follows a FORMAT of the sector.

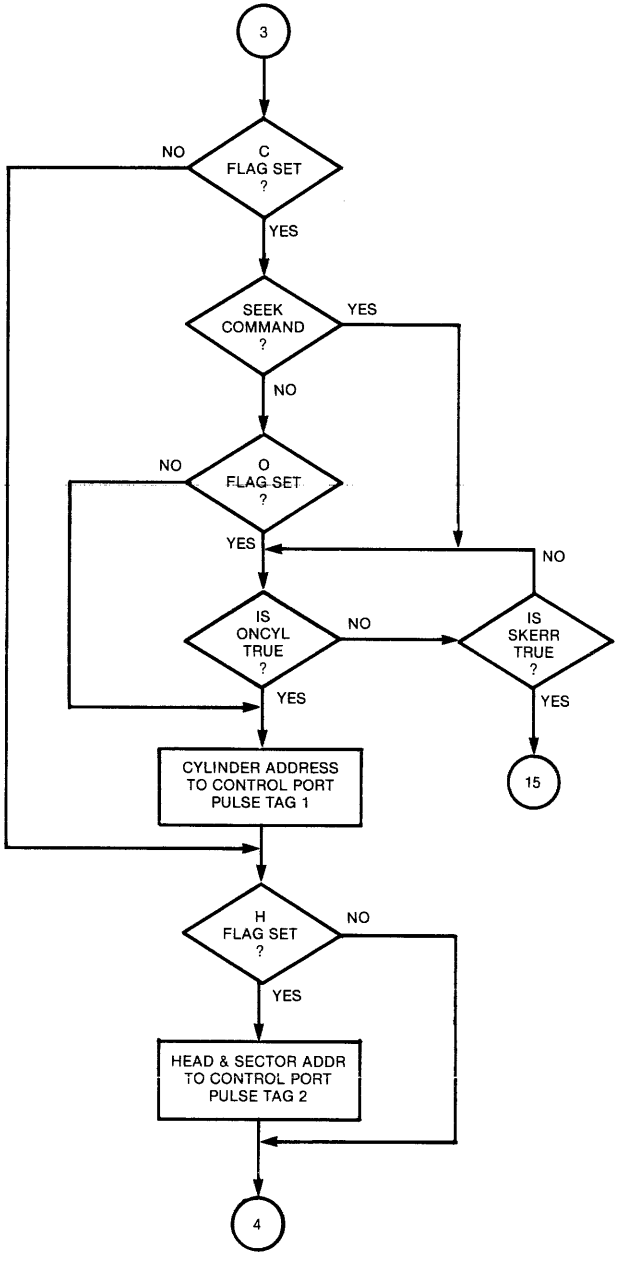


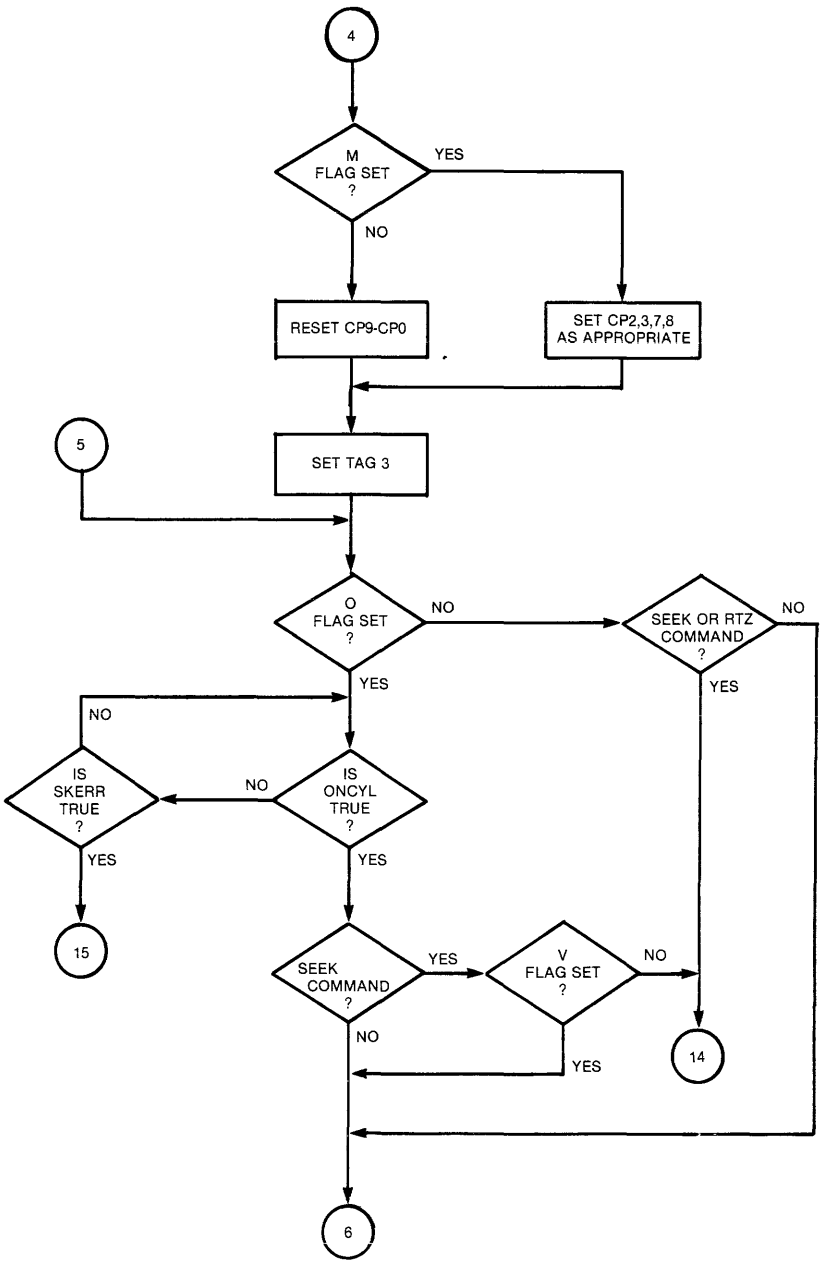
FIXED SECTOR FORMAT

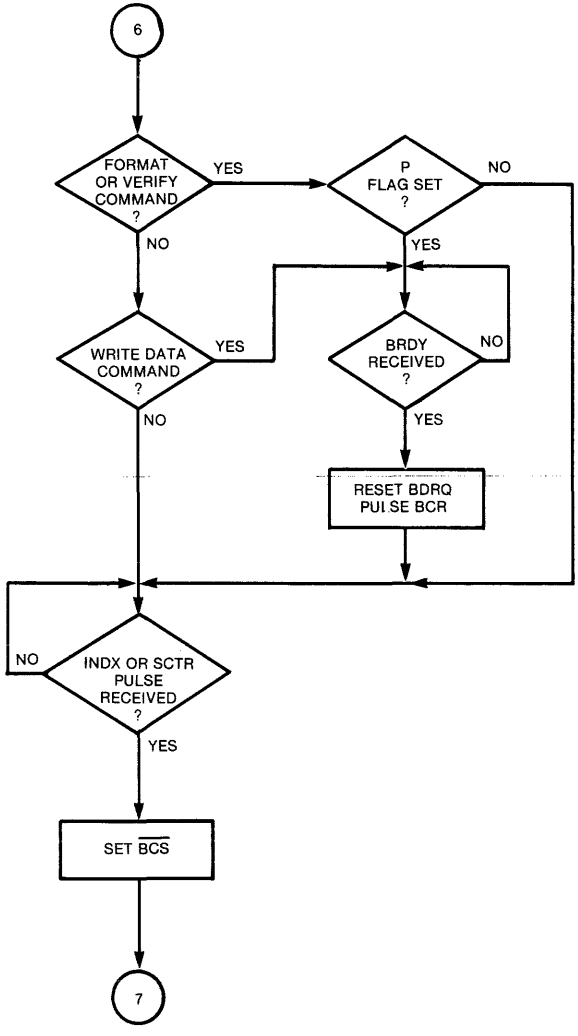


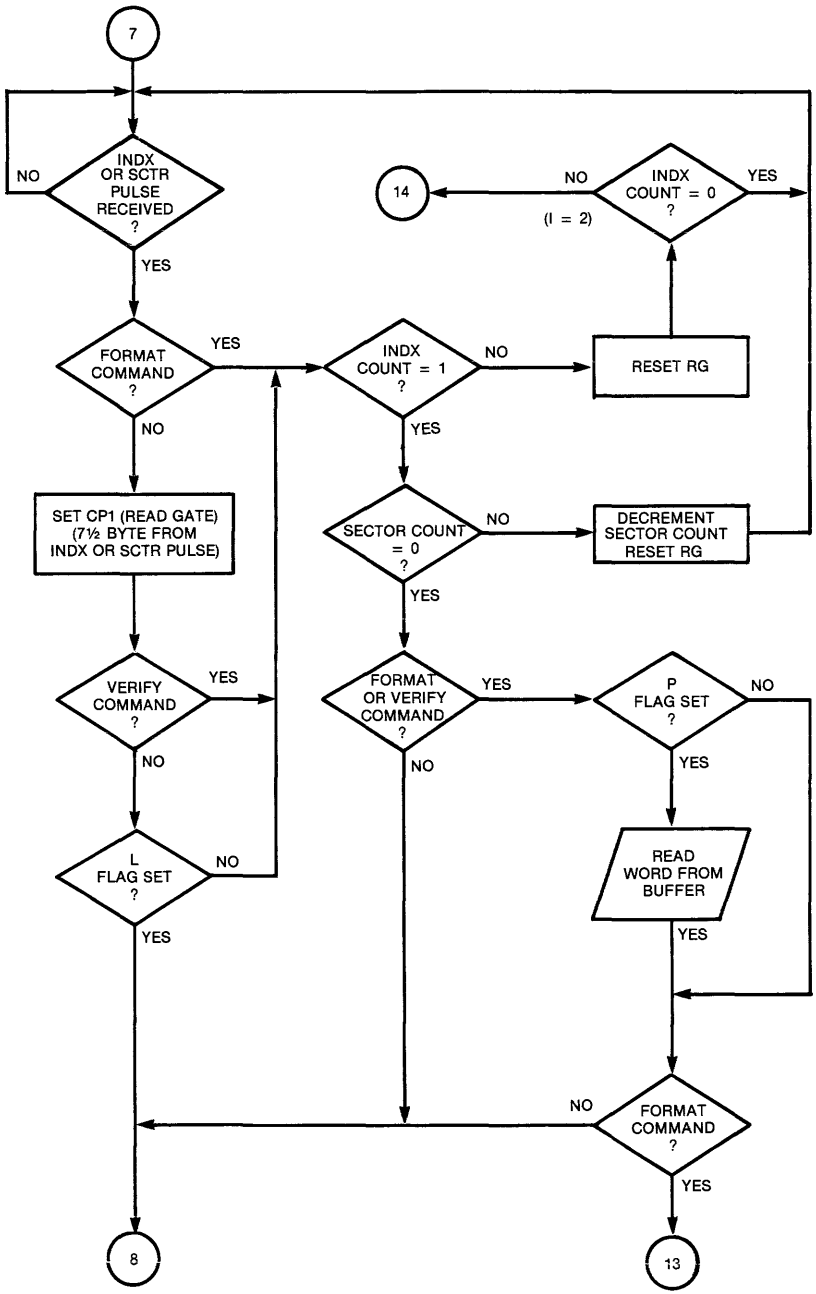

1
FC COMMAND ?
YES
NO
SET TAG 3
ISSUE CP4 PULSE (FC)
14
RTZ COMMAND ?
YES
NO
2
SET TAG 3
ISSUE CP6 PULSE (RTZ)
14

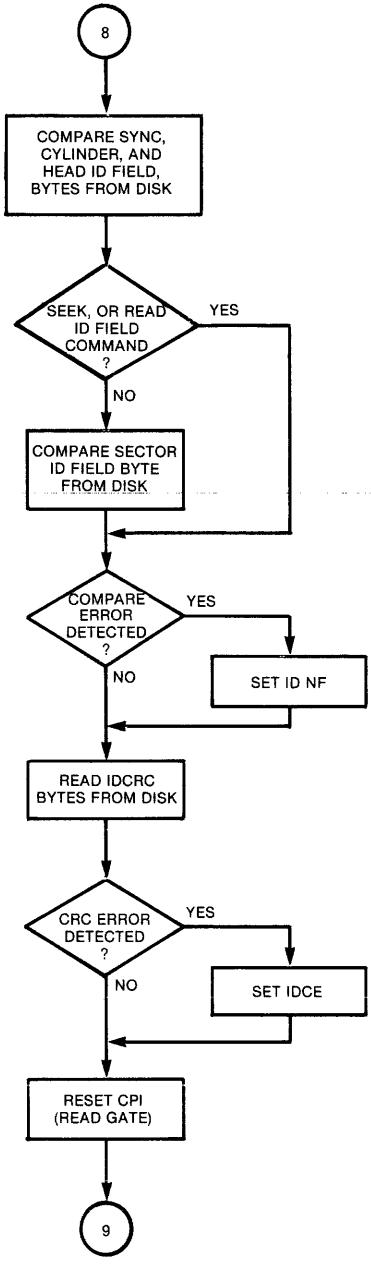

2
WRITE DATA COMMAND ?
YES
NO
IS WRPRT TRUE ?
YES
NO
15
SET BDRQ
FORMAT COMMAND ?
YES
NO
IS WRPRT TRUE ?
YES
NO
15
VERIFY COMMMAND ?
YES
NO
P FLAG SET ?
NO
YES
SET BDRQ
Z FLAG SET ?
NO
YES
HEAD & SECTOR ADDR. TO CONTROL PORT PULSE TAG 2
3

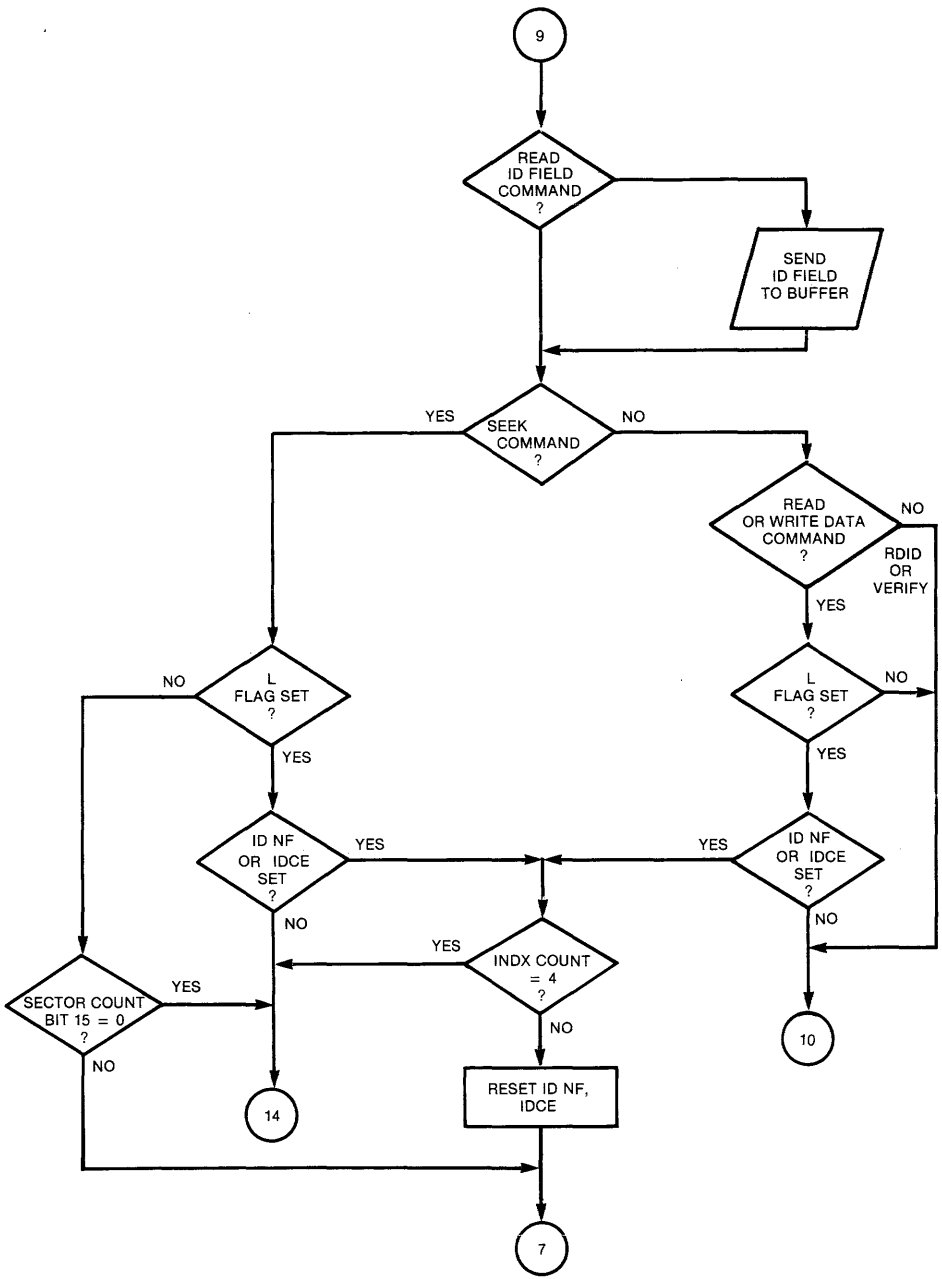

3
C FLAG SET ?
NO
YES
SEEK COMMAND ?
YES
NO
O FLAG SET ?
NO
YES
NO
IS ONCYL TRUE ?
NO
IS SKERR TRUE ?
YES
YES
CYLINDER ADDRESS TO CONTROL PORT PULSE TAG 1
15
H FLAG SET ?
NO
YES
HEAD & SECTOR ADDR TO CONTROL PORT PULSE TAG 2
4

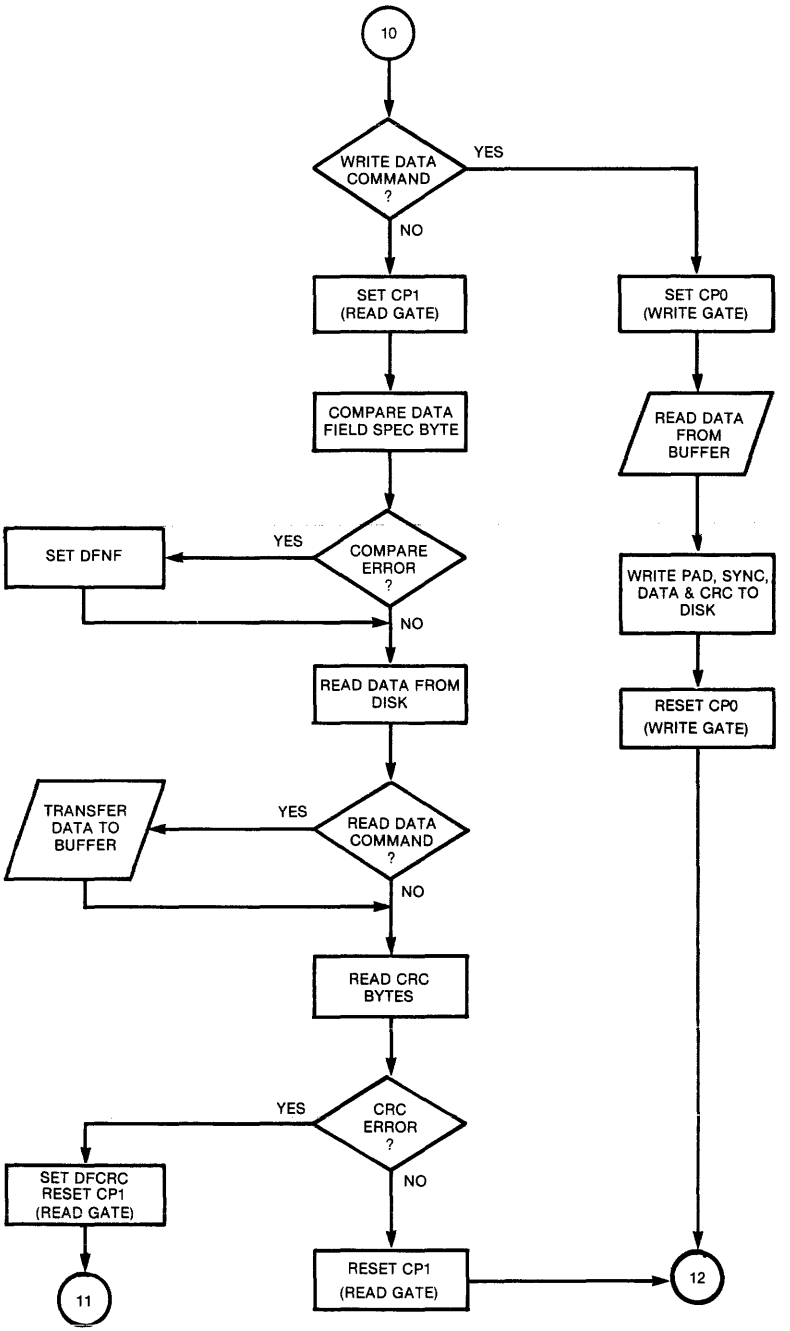

4
M FLAG SET ?
YES
NO
RESET CP9-CP0
SET CP2,3,7,8 AS APPROPRIATE
5
SET TAG 3
O FLAG SET ?
NO
SEEK OR RTZ COMMAND ?
NO
YES
YES
NO
IS SKERR TRUE ?
NO
IS ONCYL TRUE ?
YES
YES
15
SEEK COMMAND ?
YES
V FLAG SET ?
NO
NO
YES
14
6

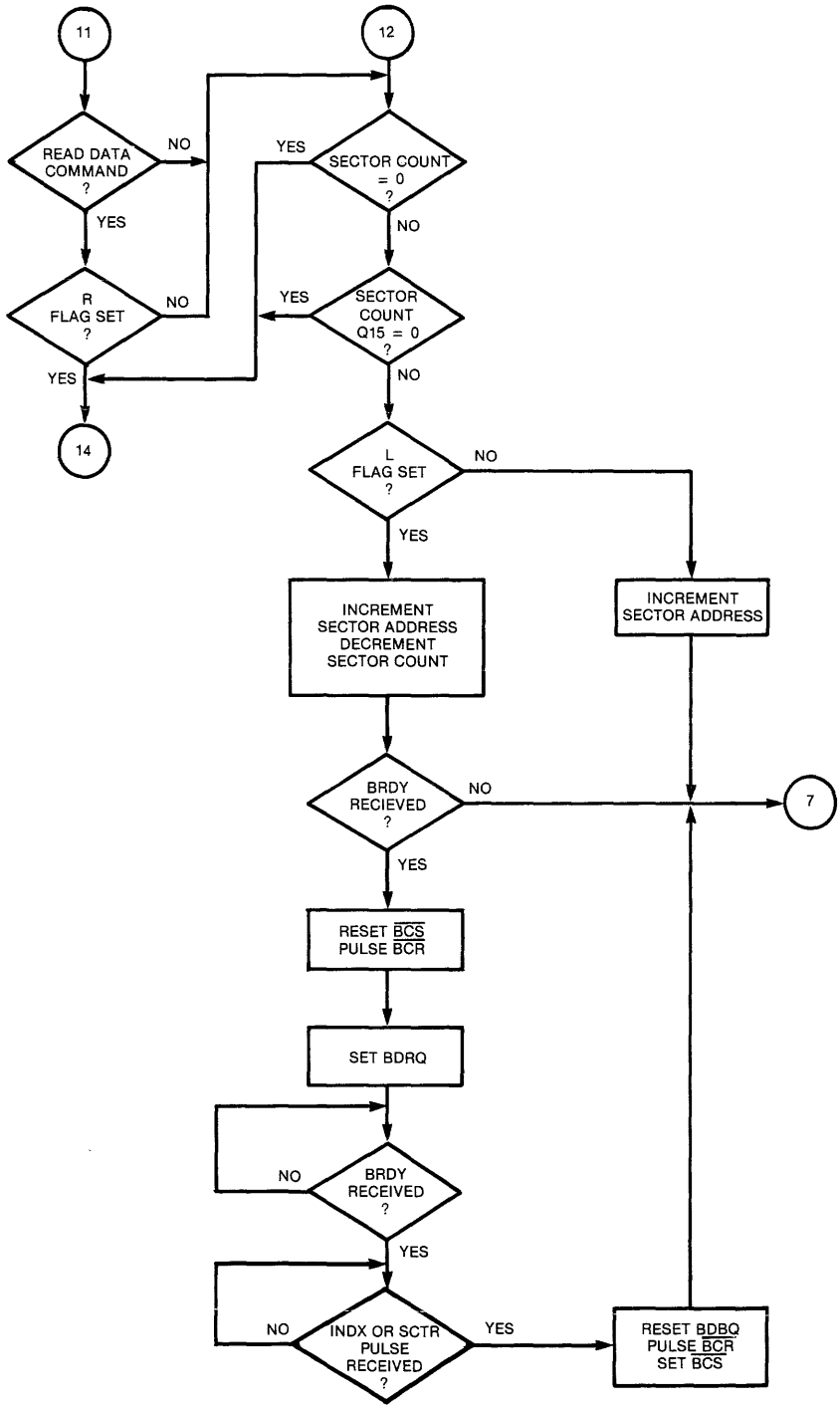

6
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
WRITE DATA COMMAND ?
YES
NO
BRDY RECEIVED ?
NO
YES
RESET BDRQ PULSE BCR
NO
INDX OR SCTR PULSE RECEIVED ?
YES
SET BCS
7

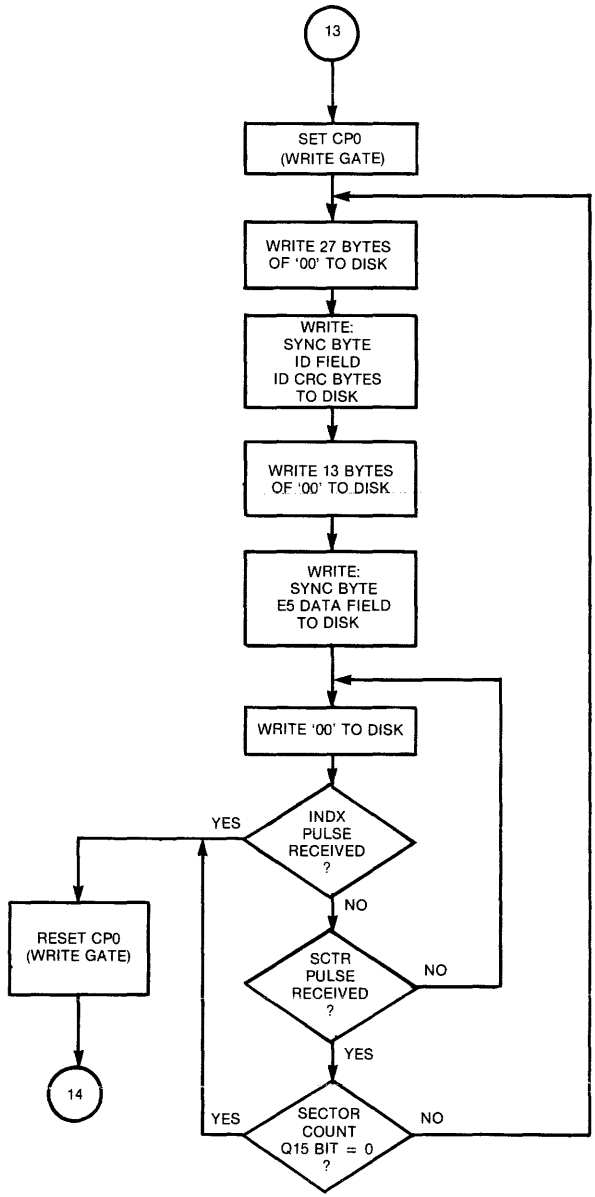

7
INDX OR SCTR PULSE RECEIVED ?
NO
YES
FORMAT COMMAND ?
YES
NO
INDX COUNT = 1 ?
NO
YES
RESET RG
14
NO
INDX COUNT = 0 ?
YES
(I = 2)
SET CP1 (READ GATE) (7½ BYTE FROM INDX OR SCTR PULSE)
SECTOR COUNT = 0 ?
NO
YES
DECREMENT SECTOR COUNT RESET RG
VERIFY COMMAND ?
YES
NO
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
L FLAG SET ?
NO
YES
READ WORD FROM BUFFER
YES
NO
FORMAT COMMAND ?
YES
8
13

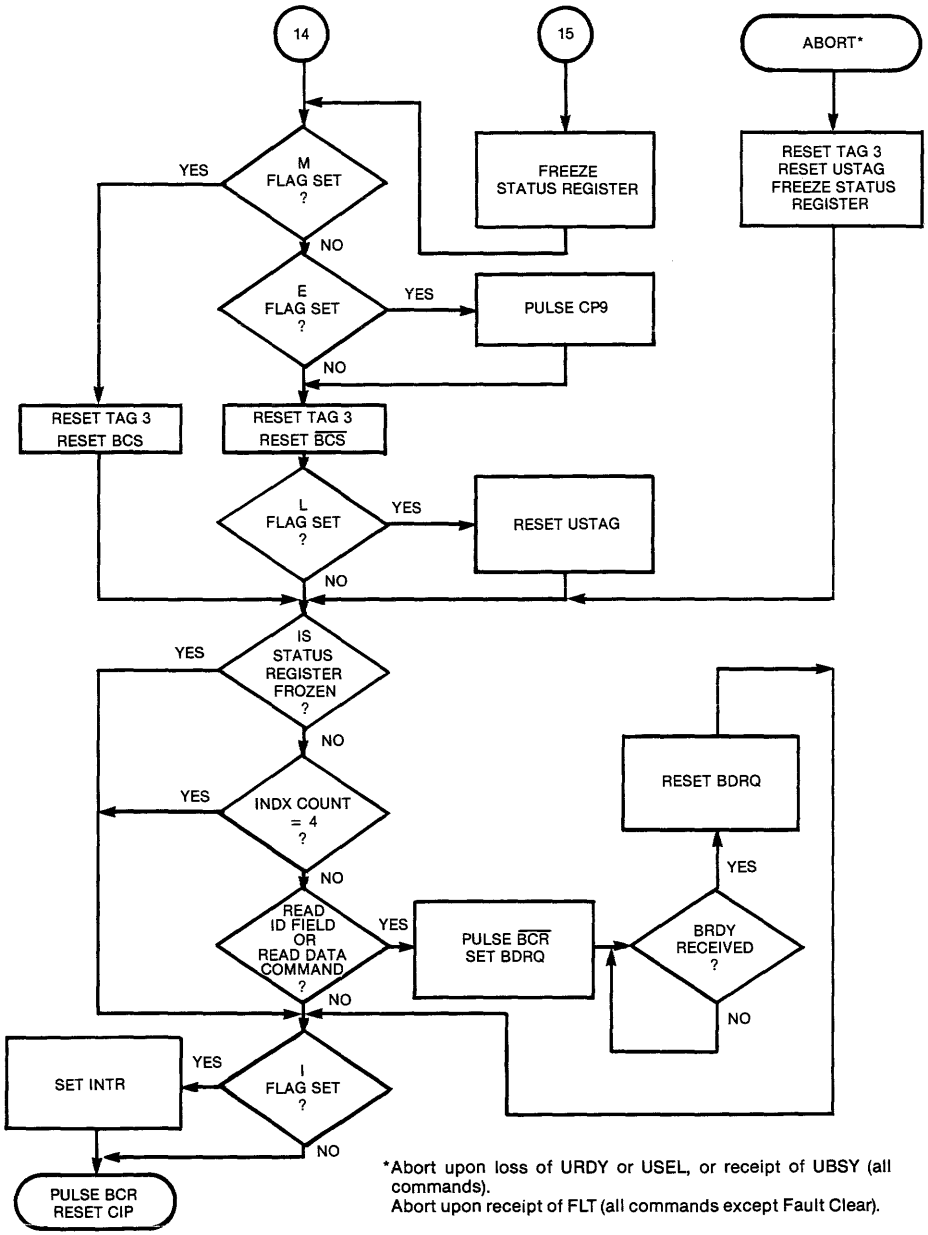

8
COMPARE SYNC, CYLINDER, AND HEAD ID FIELD, BYTES FROM DISK
SEEK, OR READ ID FIELD COMMAND ?
YES
NO
COMPARE SECTOR ID FIELD BYTE FROM DISK
COMPARE ERROR DETECTED ?
YES
NO
SET ID NF
READ IDCRC BYTES FROM DISK
CRC ERROR DETECTED ?
YES
NO
SET IDCE
RESET CPI (READ GATE)
9


9
READ ID FIELD COMMAND ?
SEND ID FIELD TO BUFFER
YES
SEEK COMMAND ?
NO
READ OR WRITE DATA COMMAND ?
NO
RDID OR VERIFY
YES
NO
L FLAG SET ?
YES
L FLAG SET ?
NO
YES
ID NF OR IDCE SET ?
YES
YES
ID NF OR IDCE SET ?
NO
NO
YES
INDX COUNT = 4 ?
SECTOR COUNT BIT 15 = 0 ?
YES
NO
NO
10
14
RESET ID NF, IDCE
7


10
WRITE DATA COMMAND ?
YES
NO
SET CP1 (READ GATE)
SET CP0 (WRITE GATE)
COMPARE DATA FIELD SPEC BYTE
READ DATA FROM BUFFER
SET DFNF
YES
COMPARE ERROR ?
WRITE PAD, SYNC, DATA & CRC TO DISK
NO
READ DATA FROM DISK
RESET CP0 (WRITE GATE)
TRANSFER DATA TO BUFFER
YES
READ DATA COMMAND ?
NO
READ CRC BYTES
YES
CRC ERROR ?
SET DFCRC RESET CP1 (READ GATE)
NO
RESET CP1 (READ GATE)
11
12


11
12
READ DATA COMMAND ?
NO
YES
SECTOR COUNT = 0 ?
YES
NO
R FLAG SET ?
NO
YES
SECTOR COUNT Q15 = 0 ?
YES
NO
YES
14
L FLAG SET ?
NO
YES
INCREMENT SECTOR ADDRESS DECREMENT SECTOR COUNT
INCREMENT SECTOR ADDRESS
BRDY RECIEVED ?
NO
7
YES
RESET BCS PULSE BCR
SET BDRQ
NO
BRDY RECEIVED ?
YES
NO
INDX OR SCTR PULSE RECEIVED ?
YES
RESET BDBQ PULSE BCR SET BCS


13
SET CP0
(WRITE GATE)
WRITE 27 BYTES
OF '00' TO DISK
WRITE:
SYNC BYTE
ID FIELD
ID CRC BYTES
TO DISK
WRITE 13 BYTES
OF '00' TO DISK
WRITE:
SYNC BYTE
E5 DATA FIELD
TO DISK
WRITE '00' TO DISK
INDX
PULSE
RECEIVED
?
YES
NO
RESET CP0
(WRITE GATE)
SCTR
PULSE
RECEIVED
?
NO
YES
14
SECTOR
COUNT
Q15 BIT = 0
?
YES
NO



*Abort upon loss of URDY or USEL, or receipt of UBSY (all commands).
Abort upon receipt of FLT (all commands except Fault Clear).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with
respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

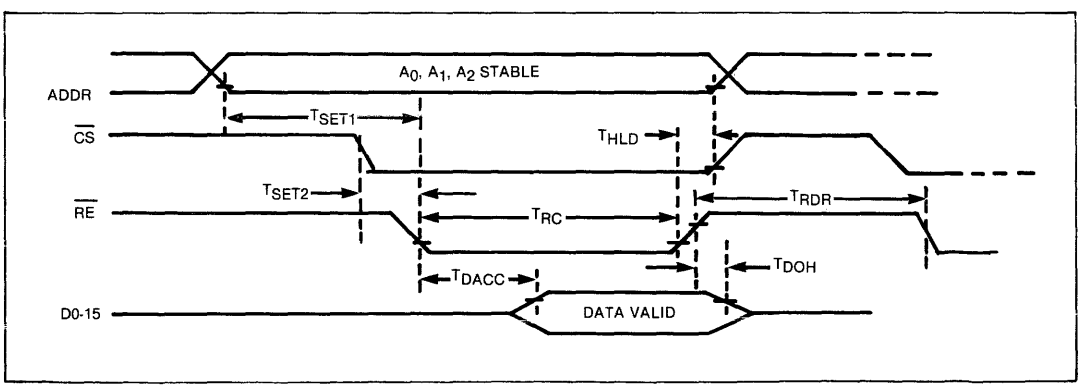
DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	FOR PINS 25, 26, 27:				See Note 1
V_{IH}	Input High Voltage	V_{CC}		V	
V_{IL}	Input Low Voltage		V_{SS} + ≤0.4 V	V	

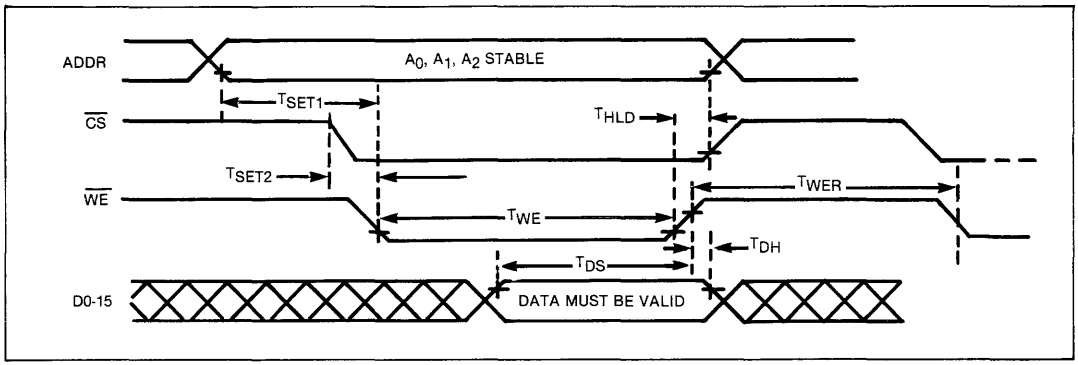
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ±.25V

HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SET1}	ADDR, Set up to $\overline{RE}$	80		nsec	
T_{SET2}	$\overline{CS}$ Set up to $\overline{RE}$	0		nsec	
T_{DACC}	Data Valid from $\overline{RE}$		375	nsec	C_L = 100 pF
T_{RC}	Read Enable Pulse Width	.375	5.0	μsec	
T_{DOH}	Data Hold from $\overline{RE}$		150	nsec	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		nsec	
T_{RDR}	Read Recovery Time	500		nsec	



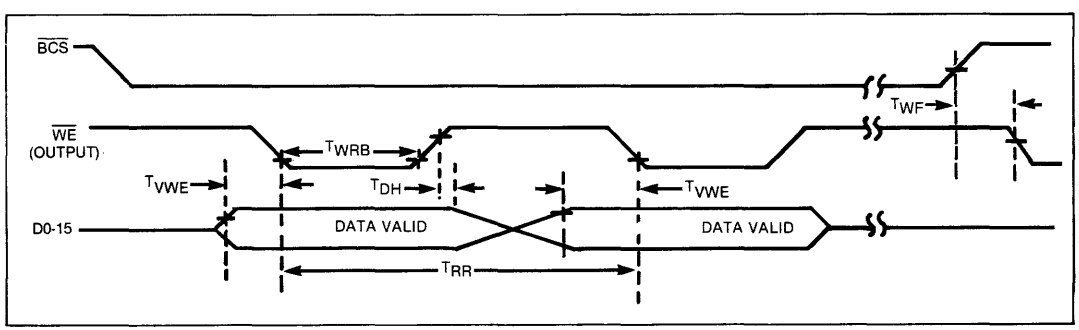
HOST READ TIMING



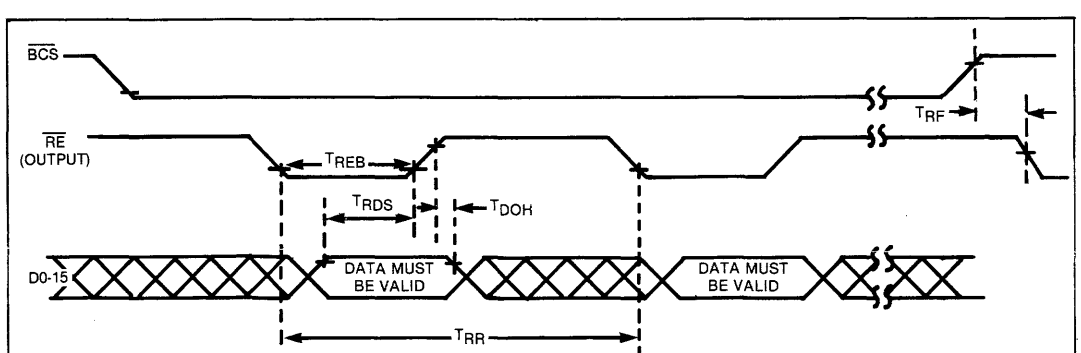
HOST WRITE TIMING

HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SET1}	ADDR, Set up to $\overline{WE}$	80		nsec	
T_{SET2}	$\overline{CS}$ Set up to $\overline{WE}$	0		nsec	
T_{DS}	Data Bus Setup to $\overline{WE}$	100		nsec	
T_{WE}	Write Enable Pulse Width	200		nsec	
T_{DH}	Data Bus Hold from $\overline{WE}$	80		nsec	
T_{HLD}	ADDR, $\overline{CS}$ Hold from $\overline{WE}$	0		nsec	
T_{WER}	Write Recovery Time	1.0		μsec	



BUFFER WRITE TIMING



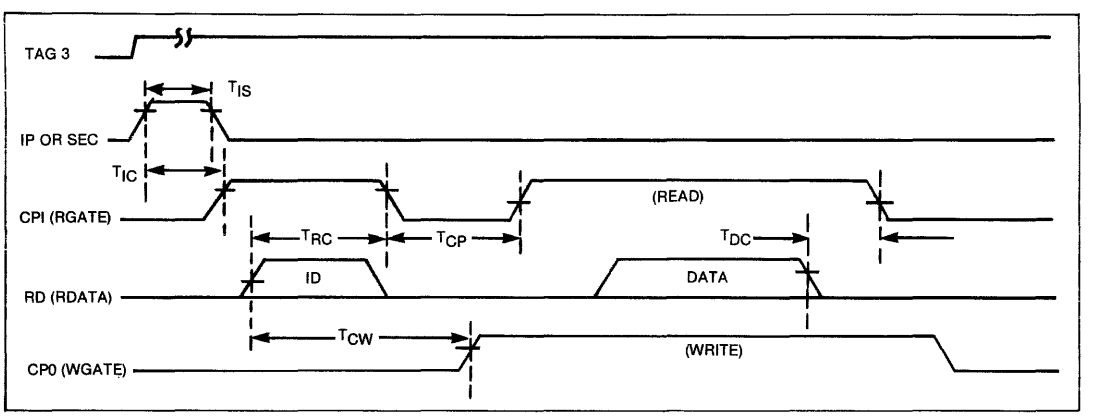
BUFFER READ TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

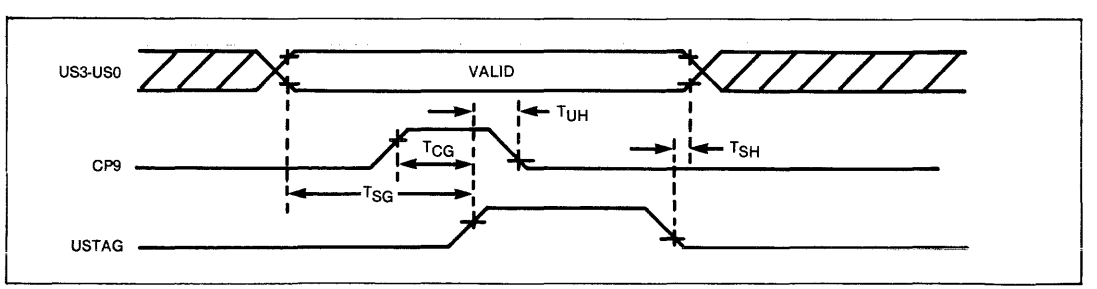
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WRB}	$\overline{WE}$ Output Pulse Width		4		SC	See Note 2
T_{VWE}	Data Set up to $\overline{WE}$		4		SC	See Note 2
T_{DH}	Data Hold from $\overline{WE}$		4		SC	See Note 2
T_{RR}	$\overline{WE}$ Repetition Rate		16		SC	See Note 2
T_{WF}	$\overline{WE}$ Float from $\overline{BCS}$			0	nsec	

BUFFER READ TIMING (WRITE SECTOR CMD)

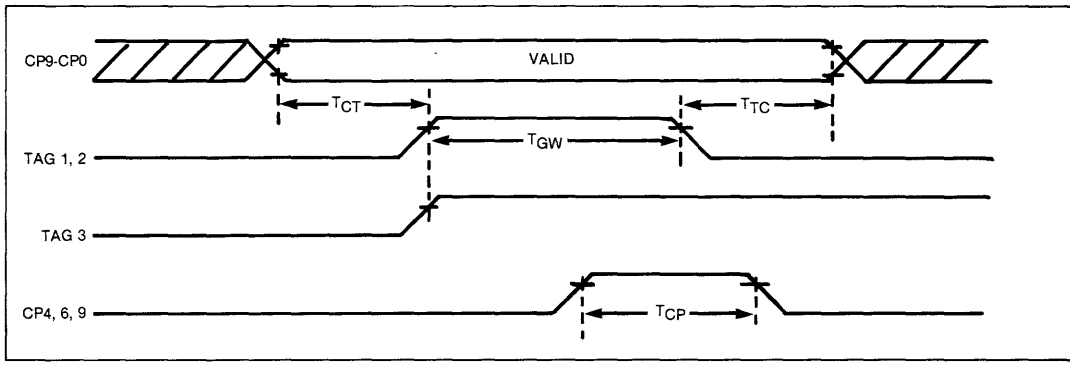
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REB}	$\overline{RE}$ Output Pulse Width		4		SC	See Note 2
T_{RDS}	Data Setup to $\overline{RE}$	100			nsec	
T_{RR}	$\overline{RE}$ Repetition Rate		16		SC	See Note 2
T_{DOH}	Data Hold from $\overline{RE}$	80			nsec	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			0	nsec	



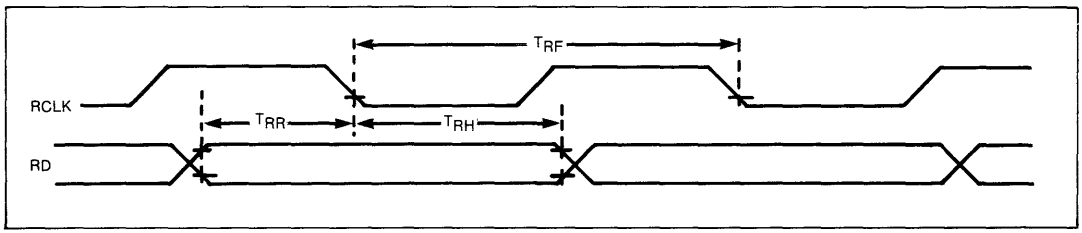
DISK R/W CONTROL TIMING



UNIT SELECT TIMING



CP TAG TIMING



READ DATA TIMING

DISK R/W CONTROL TIMING (SCLK = 9.677 MHZ)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{IS}	Index/Sector Pulse Width	.2	1.25	3.0	μsec	
T_{IC}	Index/Sector to CP1 High		60		SC	See Note 3
T_{RC}	CP1 Low from Read Data		56		SC	See Note 3
T_{CP}	CP1 Low to CP1 High			12	SC	See Note 3
T_{DC}	Last Read Data to CP1 Low		16		SC	See Note 3
T_{CW}	CP0 High from Read Data		60		SC	See Note 3

UNIT SELECT TIMING (SCLK = 9.677 MHZ)

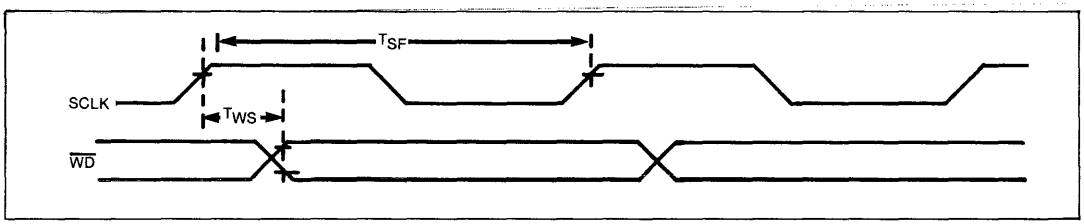
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{SG}	US3-US0 Setup to USTAG	2.0			μsec	
T_{CG}	CP9 Setup to USTAG		4		CLK	See Note 4
T_{UH}	CP9 Hold Time from USTAG		4		CLK	See Note 4
T_{SH}	US3-US0 Hold Time from USTAG	2.0			μsec	

CP TAG TIMING (SCLK = 9.677 MHZ)

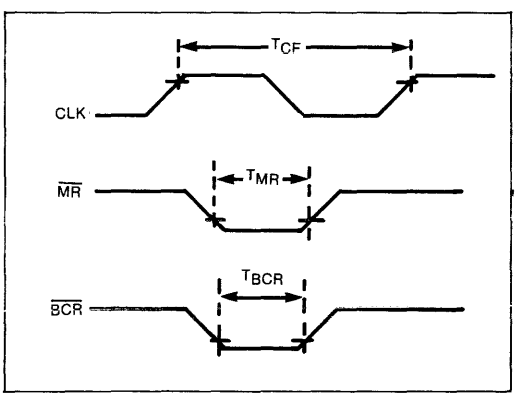
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{CT}	CP9-CP0 Setup to TAGS 1, 2, or 3		5		CLK	See Note 4
T_{GW}	TAGS 1 & 2 Pulse Width		4		CLK	See Note 4
T_{TC}	CP9-CP0 Hold Time from TAG 1, 2 Low		2		CLK	See Note 4
T_{CP}	CP4, 6, 9 Pulse Width During TAG 3 True		4		CLK	See Note 4

READ DATA TIMING

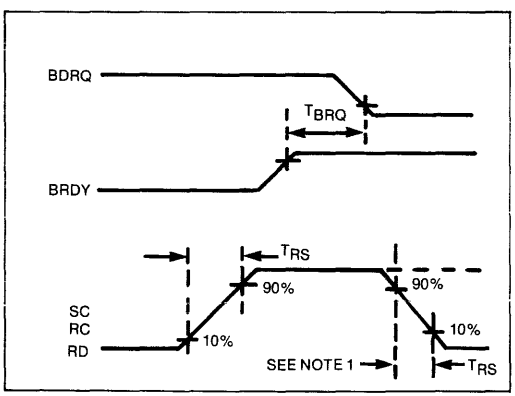
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RF}	RCLK Frequency	1.0	9.677	10.1	MHZ	
T_{RR}	Read Data Setup to RCLK Low	35			nsec	
T_{RH}	Read Data Hold Time from RCLK Low	0			nsec	



WRITE DATA TIMING



MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{SF}	Servo Clock Frequency	1.0	9.677	10.1	MHZ	
T_{WS}	$\overline{WD}$ Valid from Servo Clock High			85	nsec	C_L = 15 pf. See Note 5

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{CF}	Master Clock Frequency		2.0	2.5	MHZ	50% Duty Cycle
T_{MR}	Master Reset Pulse Width	12			μsec	CLK Active
T_{BCR}	$\overline{BCR}$ Pulse Width		4		CLK	See Note 4
T_{BRQ}	BDRQ Reset from BRDY	50		600	nsec	
T_{RS}	Rise or Fall Time			15	nsec	See Note 1

NOTES:
1. It is recommended to buffer the line receiver stage with a TTL or Schottky TTL stage on pins 25, 26 and 27. A current sink capability of 48 mA with a 100 ohm pull-up resistor will provide both the required rise and fall times and also the required voltage swing. It is recommended to locate these buffers physically near the WD1050 to minimize inductive ringing.
2. Timing is a function of the Servo Clock (SCLK) frequency. The number of SCLK periods is specified. (Disregard "TYP" in this case.)
3. Timing is a function of the Servo Clock (SCLK) frequency. The number of negative SCLK transitions plus 400 nsec. max. is specified. (Disregard the "TYP" in this case.)
4. Timing is a function of the Master Clock (CLK) frequency. The number of CLK periods is specified. (Disregard the "TYP" in this case.)
5. $\overline{WD}$ is an open drain output and requires an external 1K ohm pull-up to V_{CC}. This pin is inverted relative to the SMD interface cable. It is recommended that this output go to the 'D' input of a 74S74 flip-flop that is clocked by the SCLK buffer described in Note 1. The 74S74 $\overline{Q}$ output may then connect to the interface line driver. It is recommended that the 74S74 be located physically near the WD1050.
6. All AC timing is measured at V_{OL} = 0.8 V, V_{OH} = 2.0 V.

See page 481 for ordering information.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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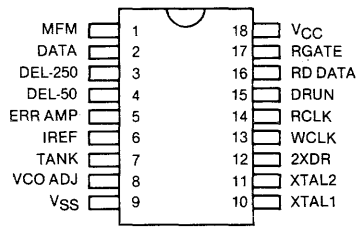
ADVANCED INFORMATION

WD1011 Winchester Data Separator Device

FEATURES

- 4.34 OR 5.0 MBIT/SEC DATA RATE
- SINGLE +5V SUPPLY
- FM OR MFM OPERATION
- COMPATIBLE WITH THE WD1010
- WRITE CLOCK GENERATOR
- HIGH FREQUENCY DETECTION



PIN DESIGNATION

DESCRIPTION

The WD1011 Winchester Data Separator has been designed to replace the complex analog/digital circuitry required for data recovery by Winchester disk drives. Directly interfacing to the WD1010 Winchester Controller device, the WD1011 allows operation of 4.34 Mbit/sec or 5.0 Mbit/sec transfer rates. In addition to data recovery, the device provides Write Clock signals for the WD1010 as well as high frequency detection for pre-amble search. Output levels on data pins swing close to the supply rails for increased noise immunity and to minimize layout restrictions.

The WD1011 operates from a single +5 volt supply and is available in an 18 pin plastic or ceramic Dual-in-Line package.

2.0.2 PIN DESIGNATIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	MFM	MFM	MFM read data input from the disk.
2	DATA	DATA	Output which extends width of disk pulse externally connected to input of delay element.
3	DELAY-250nSEC	DEL-250	Input to DRUN — externally connected to 250ns output of delay element.
4	DELAY-50nSEC	DEL-50	Input to phase detector and DRUN — externally connected to 50ns output of delay element.
5	ERROR AMPLIFIER	ERR AMP	Output from error amplifier — externally connected to input of low pass filter.
6	INPUT CURRENT REFERENCE	IREF	Input current reference used to stabilize error amplifier.
7	TANK	TANK	Variable capacitor is connected to this pin to adjust the open loop frequency of the VCO.
8	VCO ADJUSTMENT	VCO ADJ	Input to VCO TANK — externally connected to output of low pass filter.
9	V_{SS}	V_{SS}	Ground.
10	XTAL1	XTAL1	Crystal oscillator connection, or connection to TTL driver.
11	XTAL2	XTAL2	Crystal oscillator connection, or no connection if external TTL driver is used.
12	DATA REFERENCE CLOCK	2XDR	Data Reference clock.
13	WRITE CLOCK	WCLK	Write Clock output. (Frequency = RCLK)
14	READ CLOCK	RCLK	Read Clock synchronous with MFM data read from the disk.
15	DRUN	DRUN	DRUN output signal that is true whenever there is a continuous stream of either MFM ones or zeros.
16	READ DATA	RDDATA	Output of disk pulse extended MFM bits — externally connected to WD2183.
17	READ GATE	RGATE	Read Gate input from the WD2183 used to multiplex the reference clock or MFM to the phase comparator: If RGATE = 0 reference is enabled If RGATE = 1 MFM is enabled
18	V_{CC}	V_{CC}	+5V ± 5% Substrate.

See page 481 for ordering information.

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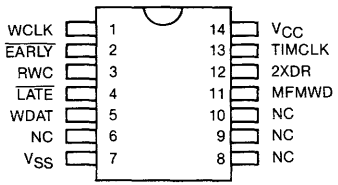
ADVANCED INFORMATION

WD1012 Write Precompensation Device

FEATURES

- INTERNAL DELAY LINE
- COMPATIBLE WITH THE WD1010
- INTERFACES DIRECTLY WITH TTL LOGIC
- CMOS TECHNOLOGY
- SINGLE +5VDC SUPPLY
- USED WITH SHUGART SA1000, SEAGATE TECHNOLOGY ST506, AND OTHER COMPATIBLE DRIVES



PIN DESIGNATION

DESCRIPTION

The WD1012 Write Precompensation Logic Device has been designed to replace a complexity of logic circuitry as well as several TTL packages. By designing the Write Precomp delay line into the package, an additional device is replaced reducing on-board space and design requirements and minimizing layout restrictions.

The WD1012 is designed to be used with the WD1010 for Winchester disk operation. The WD1012 operates from a single +5VDC supply and is manufactured using CMOS technology. The device is available in a 14 pin, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	SIGNAL	SIGNAL NAME	DESCRIPTION
1	WCLK	WRITE CLOCK	Write Clock input required to generate TIMCLK output.
2	$\overline{\text{EARLY}}$	$\overline{\text{EARLY}}$	Input from WD1010 used to gate internal Time Delay (EP) to WDAT output.
3	RWC	REDUCE WRITE CURRENT	Reduce Write Current input from the WD1010. When RWC is low, NOMINAL is high. If RWC is high and either EARLY or LATE is enabled to the WDAT multiplexer then NOMINAL is disabled, otherwise it is high. Both EARLY and LATE cannot be active at the same time.
4	$\overline{\text{LATE}}$	$\overline{\text{LATE}}$	Input from WD1010 used to gate internal time delay (LD) to WDAT output.
5	WDAT	WRITE DATA	This output line to the disk is multiplexed to the internal delay line taps (ED, ND, LD) using gated signals $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$ respectively.
6	NC	NO CONNECTION	
7	V_{SS}	GROUND	Ground.
8-10	NC	NO CONNECTION	
11	MFMWD	MFM WRITE DATA	MFM Write Data input from the WD1010. This signal is latched with 2XDR internally and transmitted to the external delay line on DOUT.
12	2XDR	2X DATA REFERENCE	This input reference clock latches MFMWD internally.
13	TIMCLK	TIMING CLOCK	Timing Clock output used by the SA1000 drives as a stepping rate reference in the stepper control circuitry. WCLK is divided down by 16 to produce TIMCLK.
14	V_{CC}	+5VDC	+5VDC input supply.

See page 481 for ordering information.

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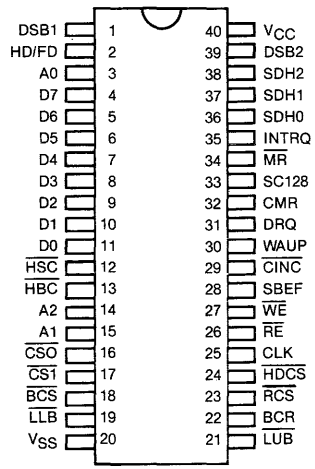
PRELIMINARY

WD1014 Error Detection/Support Logic Device

FEATURES

- 32 BIT ECC POLYNOMINAL
- BURST CORRECTION TO 5 BITS
- MULTIPLE ERROR BURST DETECTION
- DATA TRANSFER RATE OF 5 M BITS/SECOND
- PROCESSES CHECK/SYNDROME BITS IN 2-BIT SERIAL FASHION
- SECTOR SIZES = 128, 256, 512, & 1024 BYTE DATA FIELDS
- SUPPORT READ/WRITE SHORT/LONG FEATURES
- ON-CHIP STORAGE OF SYNDROME/CHECK BYTES
- 8-BIT I/O DATA BUS
- SOFTWARE ADDRESSABLE REGISTERS & LATCHES
- ON-CHIP LOGIC FOR EXTERNAL BUFFER CONTROL
- 40-PIN, DUAL-IN-LINE, N-MOS DEVICE
- TTL, MOS COMPATABILITY
- SINGLE SOURCE +5 VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1014 EDS logic chip provides the WD1002-05 Winchester Floppy Disk Controller (WFC) board with ECC and support logic. The EDS chip is a single chip device specifically designed to add error correction capabilities to a 5.25" Winchester disk drive. It also contains three 8-bit registers, three counters, and several latches that enhance the capability of the WFC on-board Control Processor (CP) chip WD1015) for control functions in real time operation. The EDS 40-pin device replaces approximately 35 standard TTL packages consisting of shift registers, flip-flops, and logic gates.

The ECC polynomial selected is the same as the one implemented in the WD1100-06 ECC/CRC logic except that the current design is a 2-bit serial implementation of the polynomial for faster operation. The ECC polynomial selected is a computer generated code optimized for sector sizes of 128, 256, 512, and 1024 byte data fields. The four ECC bytes appended by this chip enable correction of a single burst of up to 5 bits. It can also a single burst of up to 20 bits and a double burst of up to 4 bits. The computer generated code has been selected over a comparable fire code since fire codes suffer from a pattern sensitivity problem.

The WD1014 EDS device is fabricated using N-channel silicone gate technology, and is available in a 40-pin, ceramic, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1 39	DRIVE SELECT BIT 2 DRIVE SELECT BIT 2	DSB1 DSB2	These two output lines are encoded to select one of three Winchester Drives or one of four floppy drives depending upon the state of HD/$\overline{FD}$.
2	HARD OR FLOPPY DISK SELECT	HD/$\overline{FD}$	When high hard disk drives are selected and when low floppy disk drives are selected.
3 14 15	ADDRESS BIT 0 ADDRESS BIT 2 ADDRESS BIT 1	A0 A2 A1	These 3 input lines along with $\overline{CS0}$, $\overline{CS1}$, are used to address the interim registers.
16 17	CHIP SELECT BIT 0 CHIP SELECT BIT 1	$\overline{CS0}$ $\overline{CS1}$	One of these 2 lines should be low to select the registers as shown under task files.
4-11	DATA BUS	D7-D0	8 bit bidirectional data bus. Data is output only when the check/syndrome register or the command register is read.
12	HOST STATUS CONTROL	$\overline{HSC}$	This output when low, enables the WFC status onto the data lines available to the host processor.
13	HOST BUS CONTROL	$\overline{HBC}$	This output when low, enables the host to communicate to the WFC and set up all task files.
18	BUFFER CHIP SELECT	$\overline{BCS}$	This input line indicates that an external device wants to access the buffer. The ECC check/syndrome computation is also enabled at this time.
19	LOAD LOWER BYTE	$\overline{LLB}$	The rising edge of this output line is used to load the lower byte of address into the external buffer counter.
20	GROUND	V_{SS}	Ground.
21	LOAD UPPER BYTE	$\overline{LUB}$	The rising edge of this output line is used to load the upper byte of address into the external buffer counter.
22	BUFFER COUNTER RST.	BCR	This input indicates that an external device wants to reset the external buffer counters. The internal overflow counters are also cleared.
23	RAM CHIP SELECT	$\overline{RCS}$	This output line is used to select external RAM when $\overline{BCS}$ is active low or when the CP or the host is accessing the RAM.
24	HARD DISK CHIP SELECT	$\overline{HDCS}$	This output line is used to enable the WD1010 when the host is accessing its task files except the Error, Status and Command registers.
25	CLOCK	CLK	The rising edge of CLK is used to shift the ECC polynominal and the falling edge is used to count exactly 4 shifts.
26 27	READ ENABLE WRITE ENABLE	$\overline{RE}$ $\overline{WE}$	Strobes used in conjunction with $\overline{CS0}$, $\overline{CS1}$, AS-A0 to access registers.
28	SECTOR BUFFER EMPTY OR FULL	SBEF	Output signal used to indicate the sector buffer has been filled or emptied.
29	COUNTER INCREMENT	$\overline{CINC}$	The rising edge of this output signal increments an external address counter.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
30	WAKE UP	WAUP	This output signal is used to indicate that a command is being executed by the CP of the WFC board. The host cannot communicate with the WFC at this time until after the command has been completed.
31	DATA REQUEST	DRQ	The data request line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the sector buffer has been filled or emptied.
32	COUNTER MASTER RESET	CMR	This output signal resets the external address counters whenever a $\overline{MR}$ or a command has been issued by the host.
33	SECTOR COUNT OF 128 BYTES	SC128	This input signal is used in conjunction with the SDH register to indicate that the buffer has overflowed.
34	MASTER RESET	$\overline{MR}$	Used to initialize internal logic. All internal buffer overflow counters are reset, the DRQ and INTRQ flip-flops are cleared and BUSY is set.
35	INTERRUPT REQUEST	INTRQ	This output line is activated whenever a command has been completed. It is reset to the inactive state when the status register is read, or a new command is loaded via the DAL lines, or $\overline{MR}$ is asserted.
36 37 38	SECTOR SIZE DRIVE SELECT, AND HEAD SELECT BITS	SDH0 SDH1 SDH2	The least 3 significant bits of the internal SDH register are available as outputs. The SDH register is updated whenever the host writes to it.
40	+5 V	V_{CC}	+5 V input supply.

TASK FILES

WAKE UP, CS1, CS0, A2-A0, $\overline{RE}$ and $\overline{WE}$ are used to select various registers as shown below:

BUSY	CS1 –	CS0 –	A2-A0	EFFECT
X	1	1	X	Idle — Nothing selected.
0	1	0	X	Host to WFC and WD1010 files.
1	1	0	X	CP to WD1010 + RAM access.
1	0	1	X	CP to EDS registers.
X	0	0	X	Illegal condition.

			WD1010 REGISTERS		EDS REGISTERS	
A2	A1	A0	$\overline{RE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WD}$
0	0	0	RAM	RAM	0 + CHECK/SYN bytes	0 + CHECK bytes
0	0	1	Error Req.	Write Precomp		Set ECC
0	1	0	Sector Count	Sector Count	SLEEP	0 + LLB
0	1	1	Sector Number	Sector Number	Clear OVF/CNTRS	0 + LUB
1	0	0	Cylinder Low	Cylinder Low		Set DRQ
1	0	1	Cylinder High	Cylinder High		Set Read Latch
1	1	0	S.D.H.	S.D.H.	Clear Mult Mode	Set Mult Mode
1	1	1	Status Reg.	Command Reg.	0 + Command	0 + Error Reg.

COMMAND CODES

For the implementation of parts of the controls, the following command codes are pertinent:

COMMAND	BITS 7	6	5	4	3	2	1	0
READ	0	0	1	0	D	M	L	0
WRITE	0	0	1	1	0	M	L	0
FORMAT	0	1	0	1	0	0	0	0

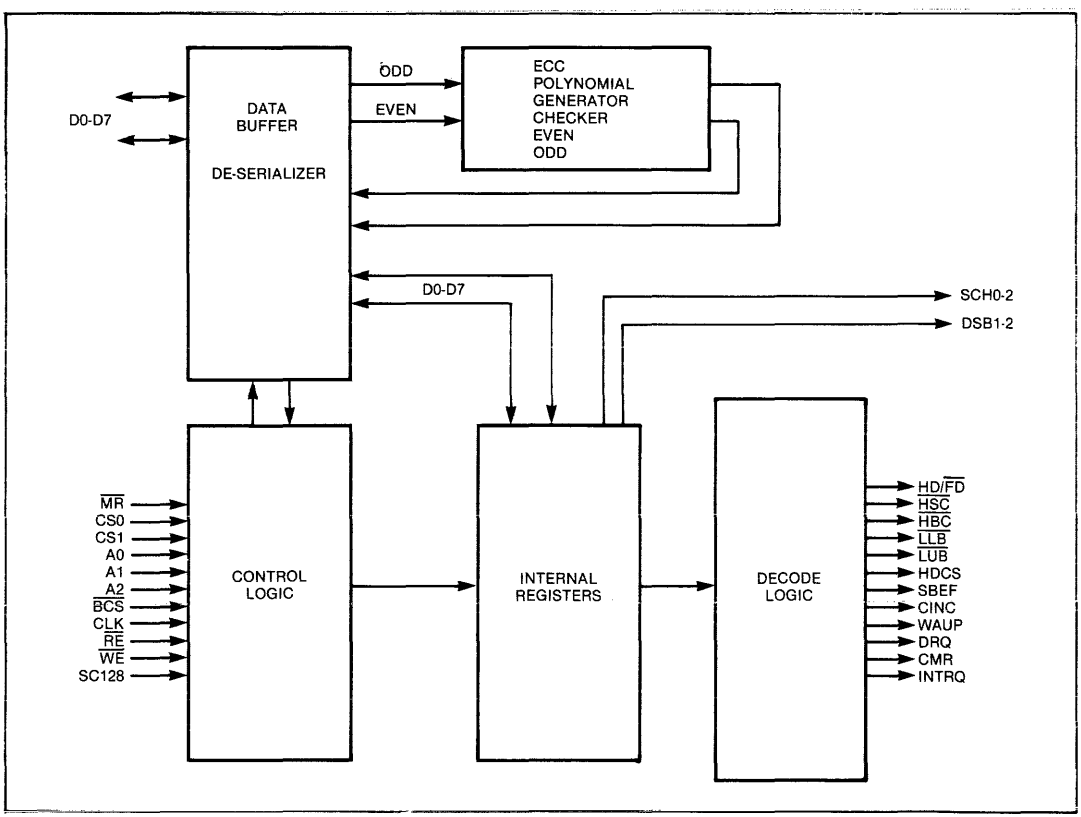
The control logic only decodes bits 7-4 and uses bit 1 (long bit) in its internal logic. The rest of the command codes and bits are not used by the EDS.

For a complete description of the commands or the task files refer to the WD1002-05 WFC data sheet.

WD1014 ARCHITECTURE

The WD1014 chip was specifically designed for the WFC board to extend the capabilities of the Control Processor (WD1015) to handle real time functions. As designed, the WD1014 is not a stand alone general purpose device unless, of course, almost all of the protocol described can be used in any new designs.

The WD1014 consists of a 2 bit serial polynomial generator (that produces 4 bytes of check/syndrome) an 8 bit data buffer and deserializer, two 8 bit latches, namely a Command/Error register and a SDH latch, and control logic consisting of 3 counters, 6 latches, and a host of combinatorial logic. The addressable registers and latches are accessed as shown in the block diagram below.



WD1014 BLOCK DIAGRAM

Each major functional block will be described essentially independent of one another. Some overlap and references to the WFC board are unavoidable and, in fact, they aid in presenting a clearer picture of the device.

THE ECC POLYNOMIAL GENERATOR

The 4 byte check/syndrome generator consists of two 16 bit shift registers each of which has 8 feedback terms implemented with XOR gates, and control gates for the feedback and data paths.

ECC computations are made whenever the external sector buffer is being accessed. The data present on the system data bus is accepted by the input data buffer and processed along with the gated data from the last stages of the shift register strings. The direction of shift within the ECC polynomial is from the L.S.B. to the M.S.B. After the last byte of data has been accessed from the sector buffer, the internal counter overflow register is set. This in turn sets a feedback inhibit register after the last byte has been processed by the ECC polynomial. At this point, the feedback terms are forced to zero and only the data path to the L.S.B. is enabled. This feature is convenient to store the 4 check/syndrome bytes internally so that RLONG and WLONG commands can be supported without the use of an external buffer.

During a write operation, the input data stream is divided by the polynomial and the 32 bit remainder obtained after buffer overflow is used as the 4 check bytes. The 4 check bytes are gated out of the WD1014 even though $\overline{RCS}$ = 1 since the internal $\overline{RBCS}$ is still active. In a READ operation, the check bytes are recomputed and compared to the recorded check bytes to generate the 4 syndrome bytes. The syndrome bytes are stored internally in the shift registers until the CP is ready to use them. Otherwise, the non-zero syndrome is used by the software algorithm to compute the displacement and the error vector within the bad sector.

To support RLONG and WLONG (L = 1) features of the WD1002-05, shift register strings are used as storage elements. After the last byte of data, the host can write or read the 4 additional bytes which serve as check bytes for the data transmitted to the buffer. In this mode the feedback terms and the outputs from M.S.B. of the shift registers are disabled so that only data is accepted and stored. This enables the user to alter the check bits/or data to verify the operation of the Error detection logic.

SDH REGISTER

This register can be written into by either the host or the CP. Bits 6 and 5 (sector size selection) are decoded as follows:

SDH6	SDH5	SECTOR SIZE IN BYTES
1	1	128
0	0	256
0	1	512
1	0	1024

The decoded bits are used in conjunction with a 3 bit counter which has SC128 as its clock. The falling edge of this input is used to set a counter overflow latch for sector sizes 256, 512 and 1024. The rising edge of this input sets counter overflow latch when the sector size is 128. The counter overflow is available on the output as SBEF and is used internally to set the buffer overflow latch and various other control logic as required by system operation. This counter and associated logic is cleared upon $\overline{MR}$, any new command, or can be directly cleared by CLROVF.

Bits 1-4 are encoded as follows:

$\overline{FD}$ = $\overline{SDH4}$. $\overline{SDH3}$
HD = $\overline{SDH4}$. $\overline{SDH3}$ = $\overline{SDH4}$ + $\overline{SDH3}$

	DSB2	DSB1
$\overline{FD}$/HD = 1	$\overline{SDH4}$	$\overline{SDH3}$
$\overline{FD}$/HD = 0	SDH2	SDH1

In addition, the latched bits 0, 1 and 2 are directly available as outputs.

COMMAND/ERROR REGISTER

This 8 bit register intercepts and holds the command issued by the host. When a command is issued:

(a) the sector counter and associated overflow latches are cleared

(b) the external counters are cleared via CMR

(c) the read command latch is cleared

(d) INTRQ is reset

(e) bit 1 (the long bit) is used by the ECC polynomial to implement the READLONG and WRITE LONG command. The CP can also read this latch so that it can execute the command.

(f) WAKEUP is set immediately if the command is a RESTORE, SEEK, or READ. For a WRITE or a FORMAT command, WAUP is set after counter overflow (COVF) occurs or an additional four RAM accesses have occured (SYN4), depending upon the long bit L = 0 or L = 1.

At the completion of a command, this register is re-used to hold error information that can be read by the host. This is necessary since error information from 2 sources has to be manipulated by the CP and reported to the host in real time when requested to do so.

ERROR DETECTION LOGIC

The error detection logic consists of an input data buffer and deserializer, two 16 bit shift registers to generate the ECC bytes, and associated control logic consisting of two 3 bit counters and integrated logic.

INPUT DATA BUFFER AND DESERIALIZER

This section is designed to accept a byte of data on the rising edge of $\overline{RE}$ or $\overline{WE}$ under the following conditions:

1. The ECC polynomial is selected as implied by SDH7 = 1.
2. A valid $\overline{RBCS}$ is generated regardless of the counter overflow
3. If the syndrome is to be read by the C.P. after an overflow condition has occurred (i.e., the syndrome is not saved after it has been read by the C.P.).

Valid data presented to the WD1014 device is accepted by the data buffer and the ECC shift registers on the rising edge of RE or We input strobes. These strobes are synchronized internally by the falling edge of the input clock so that shifting can begin on the rising edge of the clock. Data is serialized and shifted in a 2 bit parallel mode until the internal bit counter reaches the count of 3. This process is repeated for every byte of data until the counter overflow occurs plus an additional 4 bytes have been processed. Under the worst case conditions, a byte of data will be processed within 4 clock cycles after the $\overline{RE}$ or $\overline{WE}$ strobes are terminated.

MULTIPLEXER

The multiplexer is used to channel data to the I/O pins D7-D0 when one of the following conditions occur.

1. The command register is read
2. The error register is read
3. The check bytes are read
4. The syndrome bytes are read

CONTROL LOGIC

This section will cover the rest of the control logic required for system operation not described as part of the other sections, in terms of the output signals.

WAKEUP

This signal alerts the external CP that a command has been received and is internally referred to as the busy signal.

This line is set high whenever $\overline{MR}$ is asserted or a command has been received unless it is a WRITE or a FORMAT command. In that case, WAUP is not set until SBEF = 1 (COVF) if L = 0, or until an additional 4 bytes have been accepted by the EDS if L = 1.

For proper operation, the READ command latch must be set by the CP whenever that command has been received. Also the Multiple Mode latch is set by the CP in order to execute the same command a multiple number of times. This latch must be reset if executing a READ or a WRITE command only once, or if the last sector of a multiple sector transfer is being processed.

WAKEUP can only be reset by asserting SLEEP.

DATA REQUEST

The true condition of the DRQ latch can only be sampled by external circuitry if WAUP = 0.

This latch can be set by either the CP, or whenever a WRITE or FORMAT command is written into the WD1014. It is reset by COVF = 1 (SBEF) if L = 0, or until an additional 4 bytes have been accepted by the EDS if L = 1.

INTERRUPT REQUEST

Two latches are provided to handle interrupts. The programmed I/O interrupt (PINT) latch is set whenever an interrupt is desired at the start of data transmission to the host. The DMA interrupt (DINT) latch is set whenever an interrupt is desired at the end of data transmission to the host.

Both latches are reset when:

1. A $\overline{MR}$ occurs
2. Any command is transmitted
3. The output signal $\overline{HCS}$ is activated.

As in the case of DRQ, the true condition of INTRQ can only be sampled by external circuitry if WAUP = 0.

MISCELLANEOUS CONTROL SIGNALS

The rest of the output signals are purely combinatorial in nature and are best described by Boolean expressions. Refer to Section 3 for a description of these signals.

1. $\overline{HSC} = \overline{BUSY} \cdot \overline{CSO} \cdot A2 \cdot A1 \cdot A0 \cdot \overline{RE}$
2. $\overline{HBC} = \overline{BUSY} \cdot \overline{CSO} \cdot HSC$
3. $\overline{LUB} = \overline{CS1} \cdot \overline{A2} \cdot A1 \cdot A0 \cdot \overline{WE}$
4. $\overline{LLB} = \overline{CS1} \cdot \overline{A2} \cdot A1 \cdot \overline{A0} \cdot \overline{WE}$
5. $\overline{RCS} = \overline{COVF}\,(\overline{CSO} \cdot \overline{A2} \cdot \overline{A1} \cdot \overline{A0} + \overline{BCS})$
6. $\overline{HDCS} = (\overline{BUSY} \cdot A2 \cdot A1 \cdot A0 \cdot + \overline{BUSY} \cdot \overline{A2} \cdot \overline{A1} \cdot \overline{RE} + \overline{CSO}) -$

In words, $\overline{HDCS}$ is active only if the host is not accessing the error, status or the command registers of the WD1010 device, and $\overline{CSO}$ is aserted.

7. $\overline{CINC} = \overline{COVF} \cdot \overline{RSC}\,(\overline{WE} + \overline{RE})$
8. CMR = $\overline{MR}$ + CST where
   CST = $\overline{BUSY}.\overline{CSO}.A2.A1.A0.\overline{WE}$ (Any cmd written)
9. SBEF = COVF

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin
with respect to V_{SS} ..... −0.2V to +7.0V
Power dissipation ..... 1.5 Watt

STORAGE TEMPERATURE

Plastic ..... −55°C to +125°C
Ceramic ..... −55°C to +150°C

NOTE 4:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

TIMING DIAGRAMS

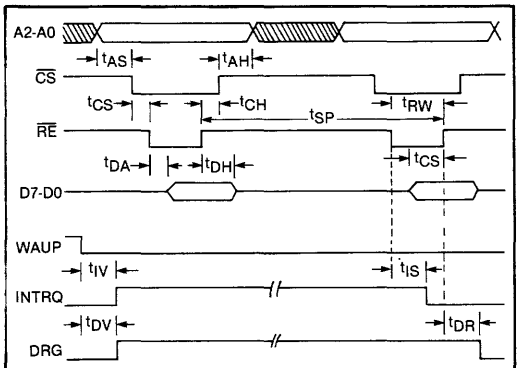


Figure 1. DATA READ CYCLE

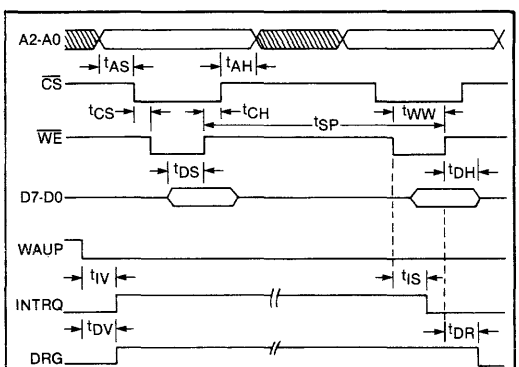


Figure 2. DATA WRITE CYCLE

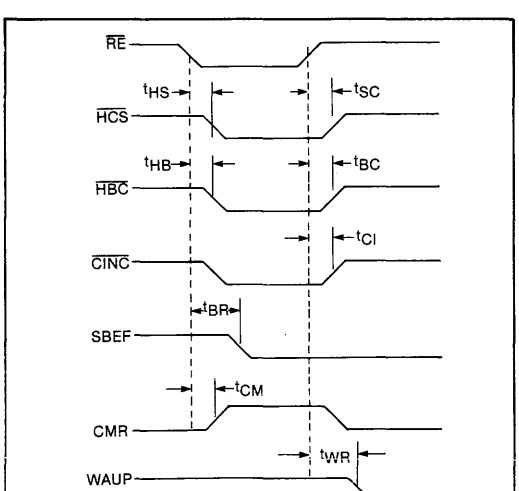


Figure 3. OUTPUT SIGNALS W.R.T. RE

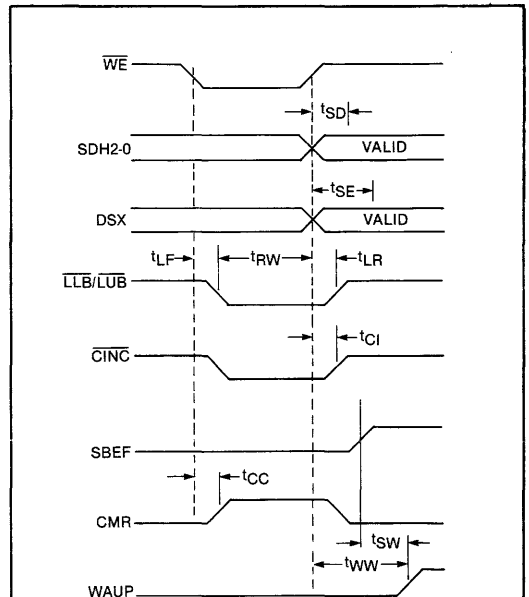


Figure 4. OUTPUT SIGNALS W.R.T. WE

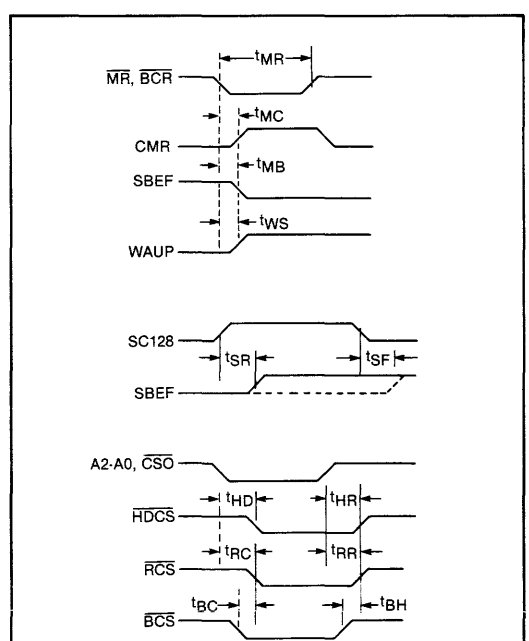


Figure 5. MISCELLANEOUS TIMINGS

See page 481 for ordering information.

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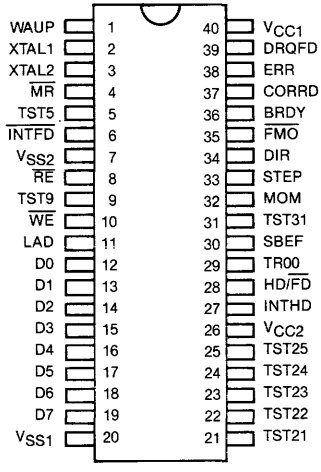
ADVANCED INFORMATION

WD1015 Buffer Manager Control Processor

FEATURES

- SINGLE +5V POWER SUPPLY
- COMPLETE BUFFER MANAGER
- PROGRAMMABLE SECTOR SIZES — 128, 256, 512, OR 1024 BYTES
- ECC BURST ERROR CORRECTION UP TO 5 BITS ON HARD DISK DATA
- 8 BIT MULTIPLEXED ADDRESS/DATA I/O BUS
- FLOPPY DISK COMMAND TRANSLATION
- SUPPORTS MOTOR ON OR HEAD LOAD DRIVES
- SUPPORTS 250 OR 500 KBS FLOPPIES
- BUFFERED SEEKS WITH FLOPPIES AND WINCHESTERS
- 16 POPULAR STEPPING RATES AVAILABLE
- AUTOMATIC RETRIES ON ALL ERRORS WITH SIMULATED COMPLETION
- POWER-ON DIAGNOSTICS INCLUDED
- 10 MHZ CLOCK RATE
- 40 PIN DIP PACKAGE



PIN DESIGNATION

DESCRIPTION

The WD1015 is a complete Control Processor (CP) that is used to handle all aspects of buffer management, in conjunction with the EDS (WD1014) device, for the Winchester/Floppy Controller board (WD1002-05). It executes all of the commands used by the WD1002-05 and does all of the control required except for real time processing, which is done by the WD1014. Throughout this specification this device will be referred to as the WD1015, or BMAC (buffer manager and controller), or simply as the CP (control processor). The WD1015 is programmed to control the transfer of information within the WFC and it maintains the necessary copies of the task files (TSF) found on both drives. Host access to the WFC causes the CP to access task file information in the TSF after a command is issued. Depending on the command, the CP will make the buffer accessible to the host or the WD1010 or 2797 controllers. The CP also controls the operation of the Error Correcting logic. During the transfer of data from the host to the WD1010, the EDS monitors the data bus, if so enabled, to compute a 4 byte ECC which is appended to the end of data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the host the CP uses the ECC to validate the data. If data is corrupted the CP envokes recovery techniques such as retries and correction. A maximum of 8 retries are attempted if two consecutive syndromes do not match. Correction is attempted only if two consecutive syndromes match. If the error is uncorrectable, the operation is terminated. The CP is also used to handle data transfers from/to the SF for the floppy disk controller, which only uses CRC check bytes for its data fields. Two commands, RESTORE and SEEK, are directly executed by the CP rather than the WD2797 floppy disk controller. During status reads by the host, the CP consolidates the normal completion status from the WD1010, the WD2797 and the current EDS status into a form consistant with established WD1010 error reporting. This consolidated status is then presented to the host. The WD1015 is fabricated using HMOS technology and is available in a 40 pin DIP package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAKE-UP	WAUP	This input is used by the BMAC to poll a command from the host. The BUSY status bit is set immediately except in case of a WRITE/ FORMAT command. In that case, WAUP and BUSY, are set only after the sector buffer has been filled by the host. WAUP is reset when the command has been executed.
2	CRYSTAL 1	XTAL1	One side of crystal input for internal oscillator. Also input for external source.
3	CRYSTAL 2	XTAL2	Other side of crystal/external source input. Frequency should be 10 MHz.
4	MASTER RESET	$\overline{MR}$	This input is used to initialize the internal logic of the processor.
5	TEST 5	TST5	This input is to be left open by the user. Internal pullup — 300K ohm.
6	FLOPPY DISK INTERRUPT	$\overline{INTFD}$	Initiates an interrupt if interrupt is enabled; disabled on reset.
7	V_{SS2}	V_{SS2}	This input is to be left open by the user. Internal pullup — 10M ohm.
8	READ ENABLE	$\overline{RE}$	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
9	TEST 9	$\overline{TST9}$	This output is left open by the user.
10	WRITE	$\overline{WE}$	Output strobe during a BUS write. Used as write strobe to an external device. Signifies that valid data has been put on the BUS.
11	ADDRESS LATCH	LAD	This output signal occurs once during each instruction cycle. The negative edge of LAD strobes address into an external latch, used to communicate to the WD1010, WD2797, and the WD1014 chips.
12-19	DATA BUS	D7-D0	True I/O bidirectional BUS which can be written to or read synchronously using $\overline{RE}$, $\overline{WE}$, strobes. Also contains the address and data during an external acess to/from port devices, under control of LAD, $\overline{RE}$, and $\overline{WE}$.
20	GROUND	V_{SS1}	Ground.
21-25	TEST 21-25	TST21-25	Unused pins to be left open by the user.
26	V_{CC2}	V_{CC2}	+5V during operation.
27	HARD DISK INTERRUPT	INTHD	This input is polled to sense an interrupt from the WD1010, indicating completion of command issued to it by the BMAC.
28	HARD DISK/FLOPPY DISK	HD/$\overline{FD}$	This input is used to sense hard disk operation when high, and floppy disk operation when low.
29	TRACK 00	TR00	This input indicates that the R/$\overline{W}$ heads of the selected floppy drive are positioned over the outermost cylinder.
30	SECTOR BUFFER EMPTY/FULL	SBEF	This input to the BMAC is set high whenever a sector of data has been written to or read from the sector buffer.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	TEST 31	TST31	Normally left open by the user.
32	MOTOR MODE	MOM	Input used to select motor-on or head load timings for floppies. This line should be left open for motor-on type drives such as the mini floppies. A delay of 1 second will be observed before $\overline{FMO}$ is activated. For head load type drives like the standard floppies, this input should be grounded. A delay of 40 mS, will be observed before $\overline{FMO}$ is activated, thereby improving the overall performance when accessing the floppies.
33	STEP	STEP	The STEP output is pulsed once for each cylinder to be stepped on the floppies. The step pulse period is normally determined by the stepping rate selected. On a RESTORE for the floppies, however, a stepping rate of 8 mS, is used if the specified stepping rate is faster than 8 mS.
34	DIRECTION	DIR	This output is used by the floppy drive to determine the direction of a seek operation. A low defines direction as out and a high specifies direction as in.
35	FLOPPY MOTOR-ON	$\overline{FMO}$	This output is used to turn the motor on, on all floppy drives supported by the WD1002 WFC board. The drives must be configured such that the heads are loaded when this signal is activated. When the floppies are being accessed for the first time, a delay as determined by MOM, is observed before activating $\overline{FMO}$. Motor on is turned off after — 3 seconds, if no further floppy accesses are made.
36	BUFFER READY	BRDY	This output signal indicates the sector buffer is ready to be accessed by an external device such as the WD1010.
37	CORRECTED DATA	CORRD	This output status indicates to the host that the BMAC has successfully corrected a data error in the data buffer, at least once. To determine if more than one correction has taken place during a multisector read, each sector specified must be reread by the host on an individual basis.
38	ERROR	ERR	Output status bit indicates that the BMAC encountered an error during the execution of a command. The error reg, on the WFC board must be read by the host to determine the type of error that occurred.
39	DATA REQUEST	DRQFD	This input indicates to the BMAC that the WD2797 has a byte of data available to be read from the disk, or requires a byte of data to be written to the floppy disk.
40	V_{CC1}	V_{CC1}	Main power supply. +5V +/−5%

See page 481 for ordering information.

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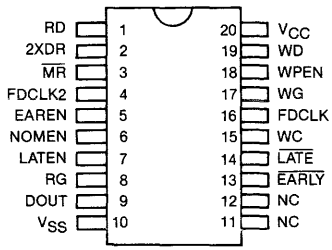
WESTERN DIGITAL
CORPORATION

WD1100-10
Write Precomp/Data Separator Support Chip

FEATURES

- COMPATIBLE WITH THE WD1010 WINCHESTER DISK CONTROLLER
- 1MHZ AND 2MHZ CLOCK OUTPUT FOR OPTIONAL FLOPPY DISK CONTROL
- EARLY/LATE/NOMINAL SIGNALS TO WRITE PRE-COMPENSATION CIRCUITRY
- SINGLE +5VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1100-10 Write Precomp/Data Separator Support Logic, when used with the WD1010 and other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester Hard Disk Write Precomp/Data Separator.

The WD1100-10 is fabricated in NMOS Silicon Gate Technology and is available in a 20 pin plastic or ceramic package.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1	RD	READ DATA	This AH input is combined data and clock pulses from disk drive. (MFM)
2	2XDR	2 TIMES DATA RATE	This AH input is a 2 TIMES DATA RATE SIGNAL used to generate WC, FDCLK1 and FDCLK2.
3	$\overline{MR}$	$\overline{MASTER\ RESET}$	MR resets the clock generator.
4	FDCLK2	FLOPPY DISK CLOCK 2	This output supplies a nominal 2 MHz clock for a floppy disc controller.
5	EAREN	EARLY ENABLE	This AH output signifies the write data should be shifted early before writing.
6	NOMEN	NOMINAL ENABLE	This AH output signifies the write data should be shifted nominal before writing.
7	LATEN	LATE ENABLE	This AH output signifies the write data should be shifted late before writing.
8	RG	READ GATE	This AH input from the WD1010 or other source signifies that data is to be read from the disk.
9	DOUT	DATA OUT	This AH output data line may be 2XDR, RD, or WD depending upon the states of RG and WG.
10	V_{SS}	GROUND	Ground.
11	NC	NC	
12	NC	NC	
13	$\overline{EARLY}$	$\overline{EARLY}$	This AL input is used with $\overline{LATE}$ to derive NOMEN, EAREN and LATEN.
14	$\overline{LATE}$	$\overline{LATE}$	This AL input is used with $\overline{EARLY}$ to derive NOMEN, EAREN and LATEN.
15	WC	WRITE CLOCK	This output runs at the data rate and is 1/2 2XDR Nominal 5.0 MHz.
16	FDCLK1	FLOPPY DISK CLOCK 1	This output supplies a nominal 1 MHz clock for a floppy disk controller.
17	WG	WRITE GATE	This AH input goes high when data is to be written to the disk. Normally comes from the WD1010.
18	WPEN	WRITE PRECOMP ENABLE	This AH input enables EAREN and LATEN to be active during a write operation.
19	WD	WRITE DATA	This AH input is the WRITE DATA signal which can be gated onto DOUT.
20	V_{CC}	V_{CC}	+5 V ± 10% power supply input.

AH = ACTIVE HIGH
AL = ACTIVE LOW

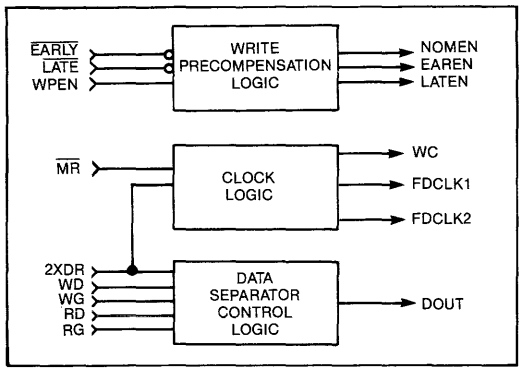


Figure 1.
WD1100-10 BLOCK DIAGRAM

DEVICE DESCRIPTION

The WD1100-10 is divided into four sections, each section will be described separately.

WRITE PRECOMPENSATION LOGIC

The $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$ and WPEN input signal from the WD1010 are decoded and latched to form NOMEN, EAREN and LATEN. These three output signals are used by external circuitry to delay the write data.

CLOCK GENERATION LOGIC

The 2XDR input signal is divided to produce the output signals WC (5 MHz), FDCLK1 and FDCLK2. Both signals are symmetrical and suitable for driving WD1010 and WD279X controllers. WC is a simple divider by-two of 2XDR. FDCLK2 is derived from a symmetrical divide-by-five counter chain driven by 2XDR and FDCLK1 is derived from FDCLK2.

DATA SEPARATOR CONTROL LOGIC

The Data Separator Control Logic provides three separate operational modes by selecting one of three input sources.

IDLE MODE RG = 0, WG = 0

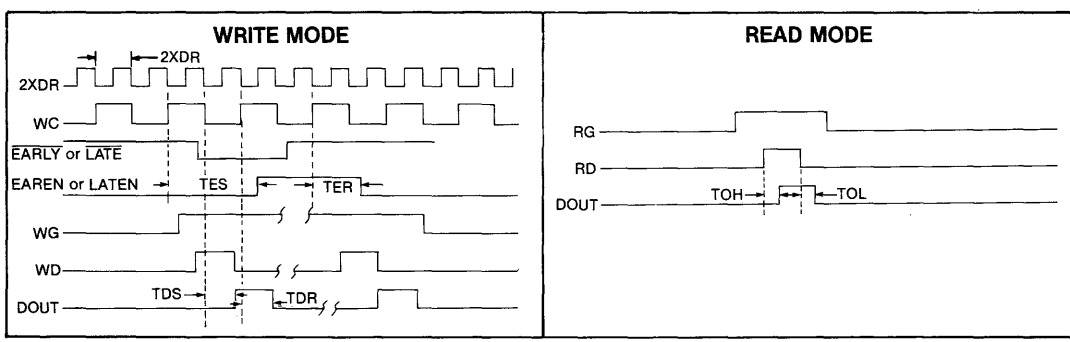
In this mode, the VCO is held locked to 2XDR. This prevents the VCO from drifting far off of the data rate when RD is not being read.

READ DATA MODE RG = 1, WG = 0

In this mode, the VCO is locked to actual data from the disk. RD is locked to the falling edge of $\overline{\text{OSC}}$. Dividing $\overline{\text{OSC}}$ with an external F/F produces RCLK. RD and RCLK are of the proper relationship to be read by the WD1010.

WRITE DATA MODE RG = X, WG = 1

In this mode, the dealy line is used to provide Write Precomp delays and at the same time the VCO is locked to WD. This accomplishes essentially the same result as locking the VCO to $\overline{\text{2XDR}}$ in the idle mode.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COND
TES	2XDR ↓ TO EAREN ↑			2NDR + 150	NS	$\overline{\text{EARLY}}$ = 0
TER	2XDR ↓ TO EAREN ↑			2XDR + 150	NS	$\overline{\text{EARLY}}$ = 1
TDS	2XDR ↓ TO DOUT ↑			165	NS	WD = 1 WG = 1
TDR	2XDR ↓ TO DOUT ↑			165	NS	WD = 0 WG = 1
TOH	RD ↑ TO DOUT ↑			70	NS	RG = 1
TOL	RD ↓ TO DOUT ↓			70	NS	RG = 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with
respect to V_{SS} . . . . . −0.2 V to +7.0 V
Power Dissipation . . . . . 1 Watt
Storage Temperature
Plastic . . . . . −55°C to +125°C
Ceramic . . . . . −55°C to +150°C

DC Electrical Characteristics TA = 0°C to 50°C; V_{CC} = +5 V +10% V_{SS} = 0 V

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	2.4			V	IOH = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

See page 481 for ordering information.

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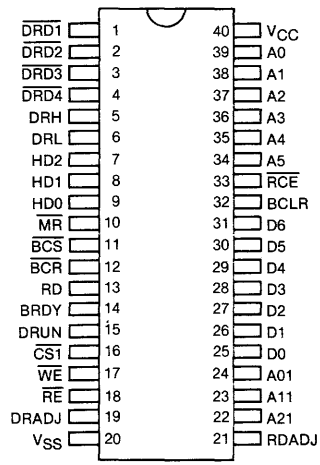
ADVANCED INFORMATION

WD1100-11 Buffer Manager Support Chip

FEATURES

- DRUN PULSE GENERATION
- RD PULSE GENERATION
- BUFFER MEMORY CONTROL
- HEAD SELECT GENERATION
- DRIVE SELECT GENERATION
- 40 PIN DUAL-IN-LINE PACKAGE
- SINGLE +5VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1100-11 Buffer Manager Support Chip controls the operation of the external buffer memory when used with the WD1010 Winchester Disk Controller. The WD1100-11 provides a means for programming the Head Select and Drive Select by latching onto the SDH information when it is available on the Data Bus. The WD1100-11 also converts the serial data from the selected drive and shapes the Read Data and DRUN pulses appropriately for the WD1010.

The WD1100-11 is designed using NMOS technology and is manufactured in a 40 pin DIP package. The WD1100-11 requires only a single +5VDC supply.

PIN DESCRIPTION

PIN NUMBER	SIGNAL	SIGNAL NAME	DESCRIPTION
1 2 3 4	$\overline{DRD1}$ $\overline{DRD2}$ $\overline{DRD3}$ $\overline{DRD4}$	$\overline{DRIVE\ DATA\ BITS}$ 1-4	Serial data from four drives.
5 6	DRH DRL	DRIVE SELECT BITS	Selects drives 1-4 depending upon bit configuration.
7 8 9	HD2 HD1 HD0	HEAD SELECT BITS 0-2	Selects heads 1-8 depending upon bit configuration.
10	$\overline{MR}$	$\overline{MASTER\ RESET}$	Master reset.
11	$\overline{BCS}$	$\overline{BUFFER\ CHIP\ SELECT}$	WD1010 to RAM chip select.
12	$\overline{BCR}$	$\overline{BUFFER\ COUNTER\ RESET}$	Resets the external buffer counter.
13	RD	READ DATA	Strobe for reading data from the disk.
14	BRDY	BUFFER READY	This line indicates the RAM buffer is ready to read or write data.
15	DRUN	DRUN	This line informs the WD1010 when a field of 0's or 1's have been detected.
16	$\overline{CS1}$	$\overline{CHIP\ SELECT\ 1}$	Host to WD1100-11 chip select.
17	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	Write Enable strobe latches SDH value on bus and increments Sector Buffer Address Counter for write operations.
18	$\overline{RE}$	$\overline{READ\ ENABLE}$	Read Enable strobe increments Sector Buffer Address Counter for read operations.
19	DRADJ	DRUN ADJUST	DRUN pulse adjustment.
20	V_{SS}	GROUND	
21	RDADJ	RD ADJUST	RD pulse adjustment.
22 23 24	A21 A11 A01	HEAD/DRIVE SDH REGISTER SELECT BITS A21, A11, A01	These bits select the SDH register in the WD1100-11 for head and drive select programming and also select the data register during R/W sector commands.
25 26 27 28 29 30 31	D0 D1 D2 D3 D4 D5 D6	DATA BIT 0-6 ACCESS LINES	7-bit data access lines.
32	BCLR	BUFFER CLEAR	This line clears the RAM buffer.
33	$\overline{RCE}$	$\overline{RAM\ CHIP\ ENABLE}$	WD1100-11 to RAM chip enable.
34 35 36 37 38 39	A5 A4 A3 A2 A1 A0	RAM ADDRESS LINES 0-5	Address lines for accessing the external RAM buffer.
40	V_{CC}	+5VDC	

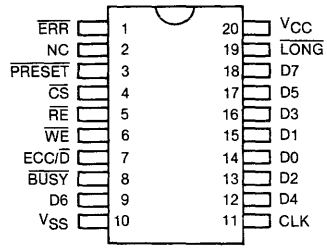
See page 481 for ordering information.

ADVANCED INFORMATION

WD1100-13 ECC Logic Device

FEATURES

- 32 BIT COMPUTER SELECTED POLYNOMIAL
- MAXIMUM BURST DETECTION SPAN-11 BITS
- PARALLEL INPUT/OUTPUT
- DATA TRANSFER RATES UP TO 5 MBITS/SEC
- RECORD LENGTH UP TO 1038 BYTES INCLUDING CHECK BYTES
- TTL, MOS COMPATIBLE
- 20 PIN, NMOS TECHNOLOGY DIP PACKAGE
- SINGLE +5VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1100-13 is designed to provide ECC capabilities for Winchester Disk Controllers and will accommodate data transfer rates of up to 5 Mbits/sec. Data is transferred into and out of the WD1100-13 via an 8 bit bidirectional parallel data port.

The WD1100-13 performs several operations including, check byte generation, error detection, and error syndrome generation. Additionally, the WD1100-13 supports user diagnostics by allowing transparent check byte transfers between the host and disk medium.

The WD1100-13 uses NMOS technology and is provided in a 20 pin DIP package configuration. Only a single +5VDC supply is required.

PIN DESCRIPTION

PIN NUMBER	SIGNAL	SIGNAL NAME	I/O	SIGNAL DESCRIPTION
1	ERR	ERROR	O	When this line is low, it indicates that no error was detected in the syndrome bytes.
2	NC	NC		NO CONNECTION
3	$\overline{\text{PRESET}}$	$\overline{\text{PRESET}}$	I	This line, when low, presents the ECC accumulator to logic ones.
4	$\overline{\text{CS}}$	$\overline{\text{CHIP SELECT}}$	I	A low input on this line enables WE and RE.
5	$\overline{\text{RE}}$	$\overline{\text{READ ENABLE}}$	I	Used to write data bytes into the ECC accumulator and read data bytes from the ECC accumulator.
6	$\overline{\text{WE}}$	$\overline{\text{WRITE ENABLE}}$	I	Used to write data bytes and check bytes into the ECC accumulator.
7	ECC/$\overline{\text{D}}$	ECC/$\overline{\text{DATA}}$	I	A logic 0 indicates that user data is being strobed for check byte computation and a logic one indicates a check/syndrome byte is being strobed.
8	$\overline{\text{BUSY}}$	$\overline{\text{BUSY}}$	O	The BUSY bit is set when the WD1100-13 is performing an input or output data transfer, thus inhibiting user access.
10	V_{SS}	GND		Ground.
9	D6	DATA BITS 0-7	I/O	8 bit parallel bidirectional bus used to transfer data bytes, check bytes, and syndrome bytes.
12	D4			
13	D2			
14	D0			
15	D1			
16	D3			
17	D5			
18	D7			
11	CLK	CLOCK	I	5 MHz clock used for internal timing within the WD1100-13.
19	$\overline{\text{LONG}}$	$\overline{\text{LONG}}$	I	When this signal is a logic one, normal mode is selected. When this signal is low, long mode is selected and PRESET is inhibited.
20	V_{CC}	+5VDC		+5VDC +10%

See page 481 for ordering information.

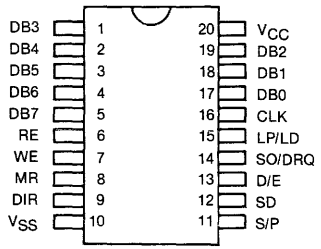
Printed in U.S.A

ADVANCED INFORMATION

WD1100-14 Programmable Polynomial Generator (PPG)

FEATURES

- PERFORMS THE FUNCTION OF AN 8 BYTE BY 8 BIT (64 BITS) PROGRAMMABLE POLYNOMIAL (ERROR CORRECTION CODE) GENERATOR.
- ALL BIT POSITIONS CAN BE PROGRAMMED TO PERFORM THE FUNCTION OF ERROR CORRECTION CODE CALCULATION.
- LAST BIT IS ALWAYS SET FOR CALCULATION.
- BYTE LENGTH OF THE POLYNOMIAL IS PROGRAMMABLE FROM 1 TO 8.
- DESIRED POLYNOMIAL CAN BE ENTERED IN PARALLEL OR SERIAL.
- DATA CAN BE WRITTEN TO DEVICE IN PARALLEL OR SERIAL FORM.
- ECC'S OUTPUT IS IN PARALLEL OR SERIAL FORMAT.
- WHEN GOING FROM FUNCTION OF READING ECC TO INPUT OF DATA FOR CALCULATION, DATA REGISTER IS SET TO ALL 1'S.
- WHEN A PARALLEL OPERATION IS IN PROGRESS, DRQ & LOST DATA STATUS ARE ACTIVE.
- ANY DATA TRANSFER TO AND FROM DEVICE IS TRUE DATA.
- PARALLEL I/O BUS & SERIAL I/O PIN.
- ALL LOGIC IS IMPLEMENTED WITH STATIC CIRCUITS.
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE.
- PACKAGED IN A 20 PIN DUAL INLINE PACKAGE.
- SINGLE 5V SUPPLY.



PIN DESIGNATION

DESCRIPTION

The WD1100-14 Programmable Polynomial Generator (PPG) is an NMOS logic device designed to be programmed for 8 bit to 64 bit polynomial byte length in 8 bit steps. The WD is designed primarily for generating ECC/CRC polynomials for Winchester control. The WD1100-14 permits greater ECC/CRC range in the transfer of data to and from Winchester disks.

The WD1100-14 requires only a single + 5VDC power source and is available in a 20-pin, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
5-1, 19-17	DATA BUS	DB7-0	I/O	I/O bus line, true, DB7 = MSB.
6	READ ENABLE	$\overline{RE}$	I	When low the contents of the 8 bit output register appear on the Data Bus. Resets DRQ pin.
7	WRITE ENABLE	$\overline{WE}$	I	When low loads the input register with the contents of the Data Bus. When a $\overline{MR}$ pulse has occurred with S/P = 0 the next 8 $\overline{WE}$'s load the 8 bytes of the polynomial register from the Data Bus. Resets DRQ pin.
8	MASTER RESET	$\overline{MR}$	I	Resets the SET latch, picks parallel or serial load of polynomial from S/$\overline{P}$ pin, and sets polynomial length latch from DIR pin.
9	DIRECTION	DIR	I	After a $\overline{MR}$ pulse : DIR = 0 selects polynomial length of 8 bytes, DIR = 1 selects a programmable polynomial length. This is 1 of 3 control pins for the functions of the chip.
10	GROUND	V_{SS}	P	Device ground.
11	SERIAL/PARALLEL	S/$\overline{P}$	I	After a $\overline{MR}$ pulse : S/$\overline{P}$ = 0 selects 8 byte parallel load of polynomial register, S/$\overline{P}$ = 1 selects serial load of polynomial register through DB7. This is 1 of 3 control pins for the functions of the chip.
12	SERIAL DATA	SD	I/O	Tri-state I/O pin for serial data to and from the chip, controlled by DIR, S/$\overline{P}$, and D/$\overline{E}$.
13	DATA/ECC	D/$\overline{E}$	I	For D/$\overline{E}$ = 0 to 1 transition a set sequence is initiated to set the data register to all 1's. On any transition resets DRQ and LD pins. This is 1 of 3 control pins for the functions of the chip.
14	SERIAL OUTPUT/ DATA REQUEST	SO/DRQ	O	When S/$\overline{P}$ = 1 this is a Serial Output from the data register. When S/$\overline{P}$ = 0 this the Data Request Output.
15	LOAD POLYNOMIAL/ LOST DATA	LP/LD	I/O	When S/$\overline{P}$ = 1 this is an input pin that when pulsed high Loads the Polynomial register with the contents of the data register. When S/$\overline{P}$ = 0 this is the Lost Data output.
16	CLOCK	CLK	I	Master clock for device.
20	V_{CC}	V_{CC}	P	+ 5V power supply.

See page 481 for ordering information.

Printed in U.S.A.

PRELIMINARY

WD1000-05 Winchester Disk Controller

FEATURES

- BUILT IN DATA SEPARATOR
- BUILT IN WRITE PRECOMPENSATION LOGIC
- CONTROL FOR UP TO 4 WINCHESTER DRIVES
- CONTROL FOR UP TO 8 READ/WRITE HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- CRC GENERATION/VERIFICATION ON ID FIELDS
- AUTOMATIC FORMATTING
- 128, 256, 512, 1024 USER SELECTABLE BYTES PER SECTOR
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- MFM ENCODING RECORDING
- AUTOMATIC RETRIES ON ALL ERRORS
- PROGRAMMABLE 500 μSEC INCREMENTAL STEP PULSE RATES (35 μS TO 7.5 mS)
- AUTOMATIC RESTORE ON ALL SEEK ERRORS
- PROGRAMMABLE DISK PARAMETERS
- ERROR REPORTING (DISK/CONTROLLER)
- 8 BIT HOST INTERFACE
- SINGLE +5VDC SUPPLY

DESCRIPTION

The WD1000-05 Winchester Disk Controller is a stand alone, general purpose Winchester disk drive controller board designed to interface up to four Winchester disk drives with a host processor. The drive signals are based upon the Floppy look-alike interface available on the Seagate Technology ST506, the Quantum Q2000, and other compatible drives.

Communications to and from the host processor are made via a separate computer access port. This port consists primarily of an 8-bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on-board sector buffer allows data transfers to the host computer independant of the actual drive data transfer rate.

The WD1000-05 is based upon a proprietary chip set consisting of the WD1010, the WD1100-11, and the WD1100-10 designed specifically for Winchester drive control.

ARCHITECTURE

The WD1000-05 has seven on board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors. The drive control cable is daisy-chained to each of the four drives.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1000-05.

The host interface connector provides interface signals that are compatible with most microprocessors and mini-computers.

SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (1024 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	7.5 mS to 35 μS (0.5 mS increments)
Data Transfer Rate:	5 Mbits/sec
Write Precomp Time:	12 Nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3M) max.
Host Cable Length:	3 ft. (1 M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.)
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes

DIMENSIONS

Length:	8 in. (20.3 cm)
Width:	5.75 in. (14.5 cm)
Height:	0.75 in. (1.9 cm)

HOST INTERFACING

The WD1000-05 is designed to easily interface to most micro computers and mini-computers. All interfacing is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers.

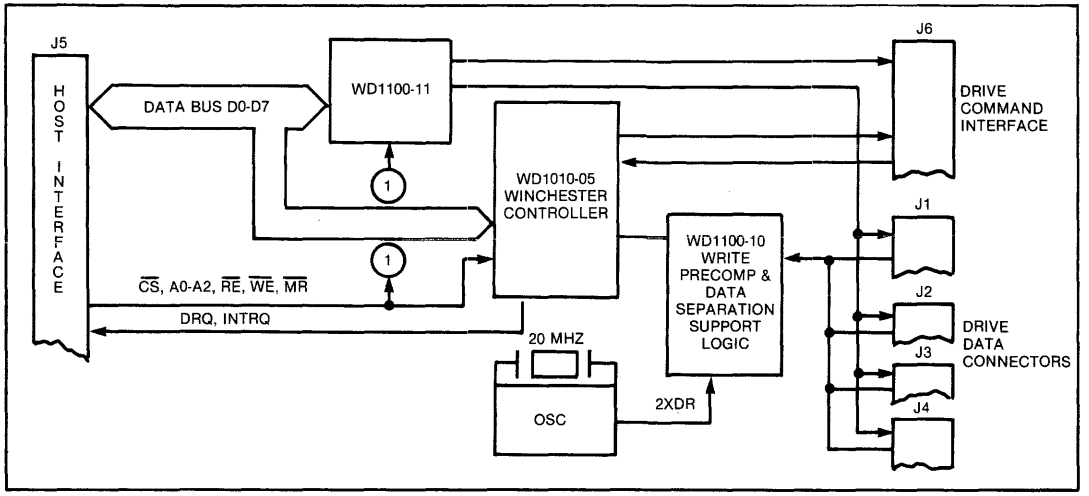


Figure 1. WD1000-05 SIMPLIFIED BLOCK DIAGRAM

Table 1. HOST INTERFACE CONNECTOR

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the CS line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When Card Select is active along with RE or WE, Data is read or written via the DAL bus. CS must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with CS, the host may write data to a selected register of the WD1000-05.
28	27	$\overline{RE}$	When Read Enable is active along with CS, the host may read data from a selected register of the WD1000-05.
30	29	PULLED UP (PUP)	
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.

Table 1. HOST INTERFACE CONNECTOR (Continued)

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exhausted or until a write or read is performed on the Cylinder Low register.
40	39	$\overline{MR}$	The Master Reset line initializes all internal logic on the logic on the WD1000-05. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset. The Drive Select register is set to 1.
	41-50	Not Connected	
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J7, pins 2 & 3.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1000-05, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Table 2:

Table 2. 34 PIN DRIVE CONTROL CONNECTOR

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6	O	$\overline{Write\ Gate}$
7	8	I	$\overline{Seek\ Complete}$
9	10	I	$\overline{TR000}$
11	12	I	$\overline{Write\ Fault}$
13	14	O	$\overline{Head\ Select\ 0}$
15	16	NC	
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24	O	$\overline{Step}$
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32	O	$\overline{Drive\ Select\ 4}$
33	34	O	$\overline{Direction\ In}$

DRIVE CONTROL SIGNAL DESCRIPTIONS

$\overline{RWC}$

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The $\overline{RWC}$ line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

$\overline{Write\ Gate}$

This output signal allows data to be written on the disk.

$\overline{Seek\ Complete}$

Informs the WD1000-05 that the head of the selected drive has reached the desired cylinder and has stabilized. $\overline{Seek\ Complete}$ is not checked after a SEEK command, thus allowing overlapped seeks.

$\overline{Track\ 000}$

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

$\overline{Write\ Fault}$

Informs the WD1000-05 that some fault has occurred on the selected drive. The WD1000-05 will not execute commands when this signal is true.

$\overline{HS0\text{-}HS2}$

Head Select lines are used by the WD1000-05 to select a specific R/W head on the selected drive.

$\overline{Index}$

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

Ready

Informs the WD1000-05 that the desired drive is selected and that its motor is up to speed. The WD1000-05 will not execute commands unless this line is true.

Step

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION IN line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

Direction In

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

DS1-DS4

These four Drive Select lines are used to select one of four possible drives.

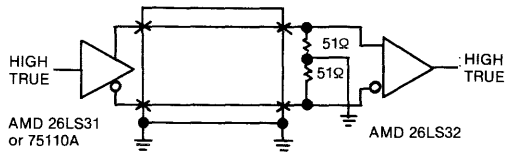
DRIVE DATA CONNECTOR

Four data connectors (J1-J4) are provided for clock signals and data between the WD1000-05 and each drive. All lines associated with the transfer of data between the drive and the WD1000-05 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

Table 3. DATA CONNECTIONS AND DESCRIPTIONS

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1		NC
4	3		NC
6	5		NC
8	7		NC
	9		NC
	10		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	− MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	− MFM Read Data
19			GND
20			GND

DIFFERENTIAL DATA DRIVER/RECEIVER



NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

$Z_X = 105\Omega$ FLAT RIBBON OR TWISTED PAIR MAX 10 FT.

POWER CONNECTOR

A four pin connector (J7) is provided for power input to the WD1000-05. See Table 4.

Table 4.

PIN	WD1001-05
1	Not Connected
2	Ground
3	Ground
4	+ 5V Regulated
Housing	Amp 1-4840429-0

TASK FILE

The Task File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addreses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE:
Registers are **not** cleared by master reset (MR).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	—	ID	—	AC	TK	DM

Bit 7 — Bad Block Detect
This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 — CRC Data Field
This bit is set when a data field CRC error has occurred or the Data Address Mark has not been found. The sector buffer may still be read but will contain errors.

Bit 5 — Reserved
Not used; forced to a zero.

Bit 4 — ID Not Found
This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occurred.

Bit 3 — Reserved
Not used; forced to a zero.

Bit 2 — Aborted Command
This bit is set if a command was issued while the DRDY (Pin 28) line is low or the WF (Pin 30) line is low. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 — TK000 Error
This bit is set only by the restore command. It indicates that the TK000 (Pin 31) line has not gone active after the issuance of 1024 stepping pulses.

Bit 0 — Data Address Mark Not Found
This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC (Pin 33) line is asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of H'01' will cause RWC to activate on cylinder 4; H'02' on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . 1020. The RWC will be asserted when the present cylinder is equal to a greater than the value in this register. For example, the ST506 requires precomp on cylinder 128 (H'80') and above. Therefore, the write precomp cylinder register should be loaded with 32 (H'20').

SECTOR COUNT

This register holds the number of sectors that are needed to be transferred to the buffer:

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER REGISTERS

Internal to the WD1000-05, is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and low registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1000-05 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

CYLINDER NUMBER LOW

This register holds the least significant 8 bits of the desired cylinder number:

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used in conjunction with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

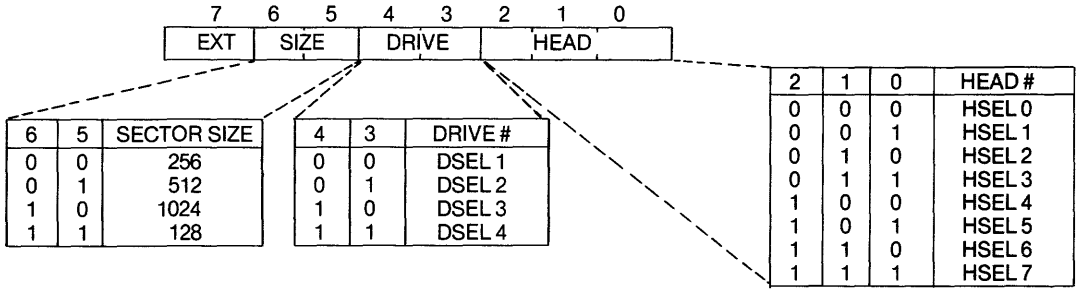
This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the end of the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extension bit. Note that the sector size bits are written to the ID during a formatting command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:



6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	—	CIP	ERR

Bit 7 — Busy
This bit is set whenever the WD1010 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled.

Bit 6 — Ready
This pin normally reflects the state of the DRDY (Pin 28) line.

Bit 5 — Write Fault
This bit reflects the state of the WF (Pin 30) line. Whenever the WF pin goes high, an interrupt will be generated.

Bit 4 — Seek Complete
This bit reflects the state of the SC (Pin 32) line. Certain commands will pause until seek complete is true.

Bit 3 — Data Request
This bit reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BDRQ signal can be used in DMA interfacing, while the DRQ bit can be used for programmed I/O transfers.

Bit 2 — Reserved
Not used. This bit is always forced to a zero.

Bit 1 — Command in Progress
When this bit is set, a command is being executed

and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host.

Bit 0 — Error
This bit is set whenever any bits in the error register are set. It is the logical 'or' of the error register and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
		C	O	M	M	A	N	D		

The commands begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ (Pin 3) line, if set, will be cleared by a write to the command register.

COMMANDS

The WD1000-05 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

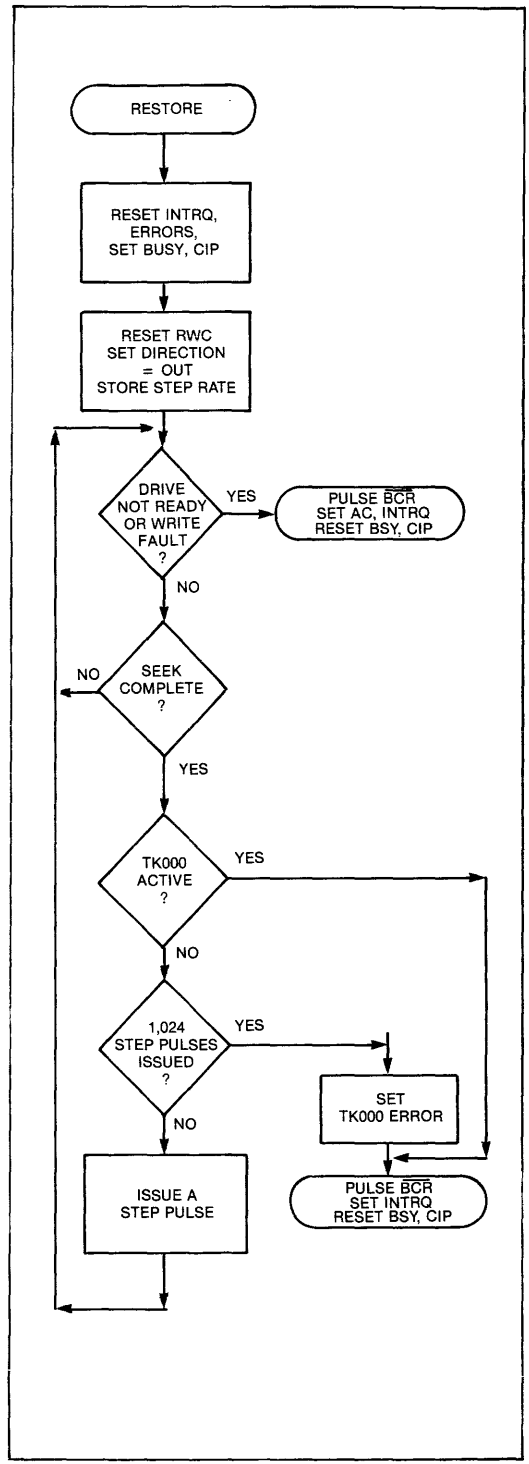
COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field

For 5 MHz WCLK:

R_3-R_0 = 0000 — ≈35 μs.
0001 — .5 ms.
0010 — 1.0 ms.
0011 — 1.5 ms.
0100 — 2.0 ms.
0101 — 2.5 ms.
0110 — 3.0 ms.
0111 — 3.5 ms.
1000 — 4.0 ms.
1001 — 4.5 ms.
1010 — 5.0 ms.
1011 — 5.5 ms.
1100 — 6.0 ms.
1101 — 6.5 ms.
1110 — 7.0 ms.
1111 — 7.5 ms.



Bit 0, ("T") Read Sector, Write Sector Commands

Should be set to 0 for WD1000-05

M = Multiple Sector Flag

M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable

I = 0, Interrupt at BDRQ time
I = 1, Interrupt at end of command

RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1000-05 waits for the Seek Complete line to go active before issuing the next pulse. If after 1,024 stepping pulses, the TK000 line does not go active, the WD1000-05 will set the TK000 error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R_3-R_0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

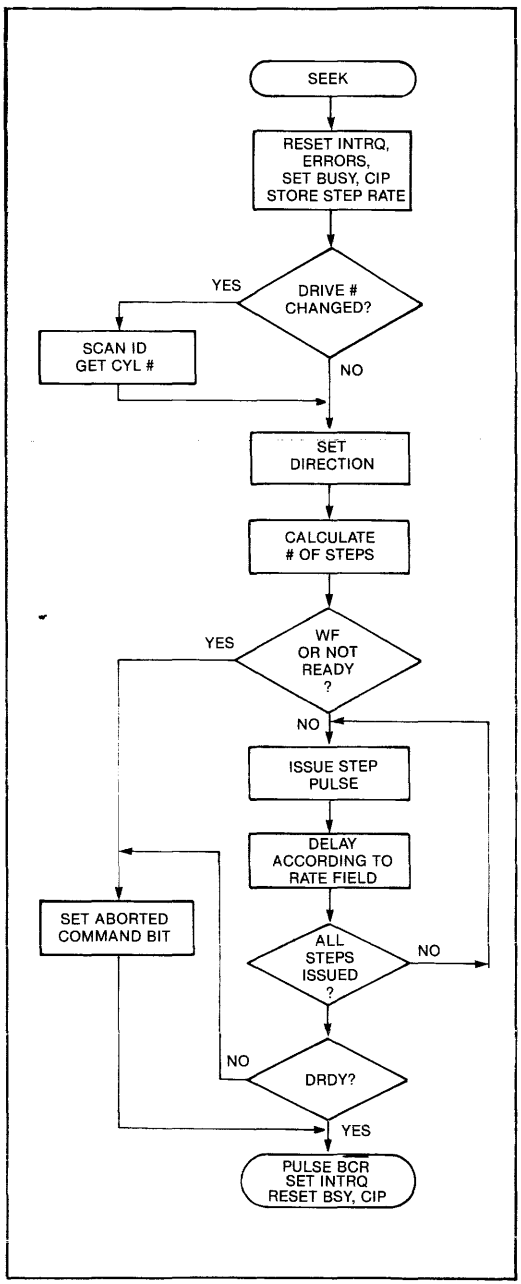
Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

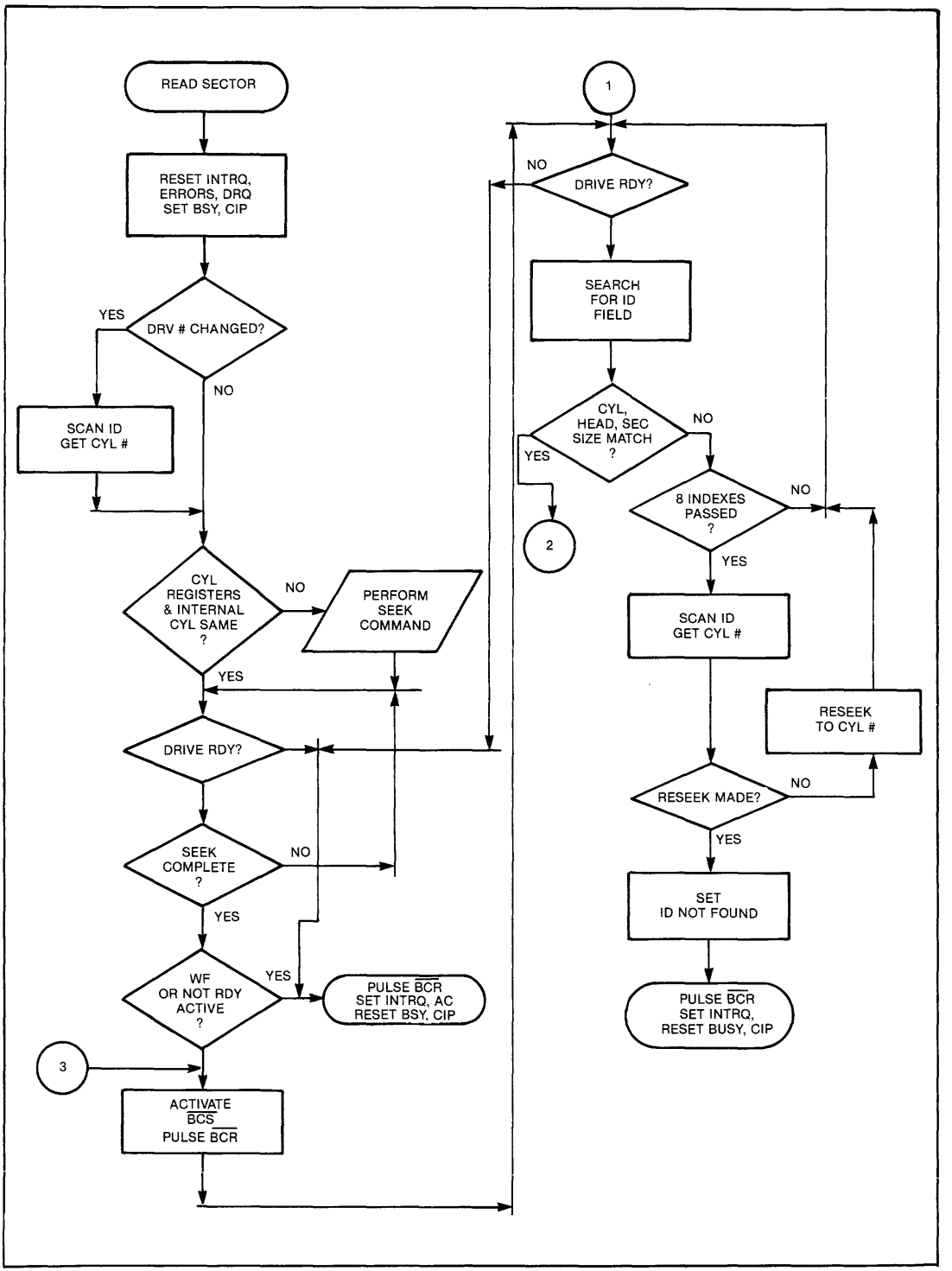
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

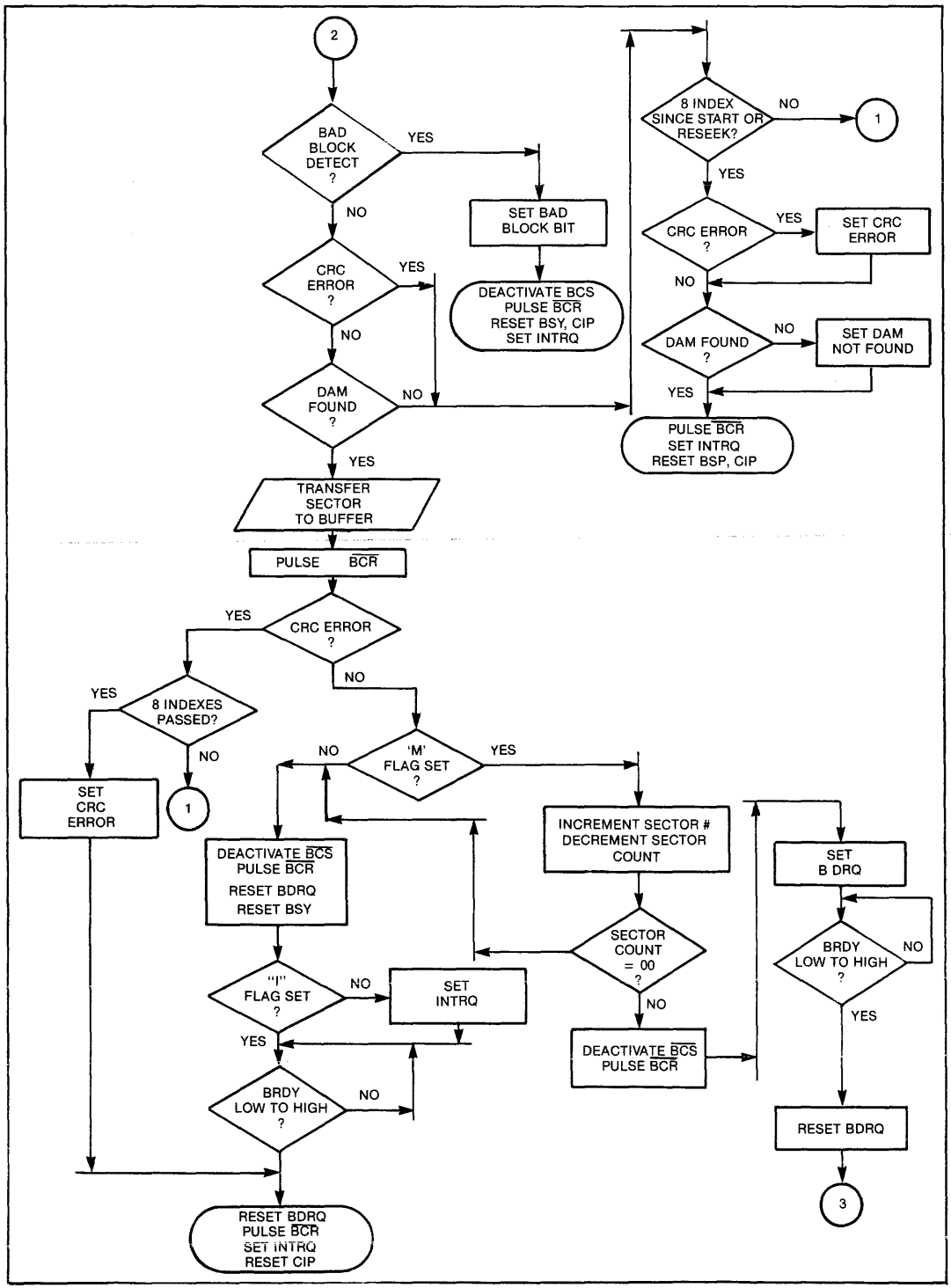
READ SECTOR

The read sector command is used to transfer one or more sectors of data to the disk. Upon receipt of this command, the WD1000-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and a seek takes place. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1000-05 must find an ID with the correct cylinder, head, sector size, and CRC within 8 revolutions or else the appropriate error bits will be set and the command terminated. If not, eight retries are performed with the ID-NOT-FOUND error bit set and the command terminated. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.




READ SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRV # CHANGED?
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL SAME ?
NO
PERFORM SEEK COMMAND
YES
DRIVE RDY?
SEEK COMPLETE ?
NO
YES
WF OR NOT RDY ACTIVE ?
YES
PULSE BCR SET INTRQ, AC RESET BSY, CIP
3
ACTIVATE BCS PULSE BCR
1
NO
DRIVE RDY?
SEARCH FOR ID FIELD
CYL, HEAD, SEC SIZE MATCH ?
NO
YES
2
8 INDEXES PASSED ?
NO
YES
SCAN ID GET CYL #
RESEEK TO CYL #
RESEEK MADE?
NO
YES
SET ID NOT FOUND
PULSE BCR SET INTRQ, RESET BUSY, CIP


2
BAD BLOCK DETECT ?
YES
SET BAD BLOCK BIT
DEACTIVATE BCS
PULSE BCR
RESET BSY, CIP
SET INTRQ
NO
CRC ERROR ?
YES
NO
DAM FOUND ?
NO
YES
TRANSFER SECTOR TO BUFFER
PULSE BCR
CRC ERROR ?
YES
NO
8 INDEXES PASSED?
YES
NO
SET CRC ERROR
1
'M' FLAG SET ?
NO
YES
DEACTIVATE BCS
PULSE BCR
RESET BDRQ
RESET BSY
"I" FLAG SET ?
NO
SET INTRQ
YES
BRDY LOW TO HIGH ?
NO
RESET BDRQ
PULSE BCR
SET INTRQ
RESET CIP
INCREMENT SECTOR #
DECREMENT SECTOR COUNT
SECTOR COUNT = 00 ?
NO
DEACTIVATE BCS
PULSE BCR
8 INDEX SINCE START OR RESEEK?
NO
1
YES
CRC ERROR ?
YES
SET CRC ERROR
NO
DAM FOUND ?
NO
SET DAM NOT FOUND
YES
PULSE BCR
SET INTRQ
RESET BSP, CIP
SET B DRQ
BRDY LOW TO HIGH ?
NO
YES
RESET BDRQ
3

When the data address mark is found, the WD1000-05 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e. after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1000-05 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero or BRDY goes inactive. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1000-05:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0 (On).
(3)	1000-05:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1000-05:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(5)	1000-05:	Sets BDRQ = 1; sets DRQ flag.
(6)	1000-05:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1000-05:	Waits for BDRY then sets INTRQ = 1; End.
(9)	1000-05:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1000-05:	Strobes $\overline{BCR}$; set $\overline{BCS}$ = 0 (On).
(3)	1000-05:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1000-05:	Decrements sector count register; increments sector number register.
(5)	1000-05:	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1 (Off).
(6)	1000-05:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1000-05:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1000-05:	Go to Step (2).
(11)	1000-05:	Activates INTRQ.

WRITE SECTOR

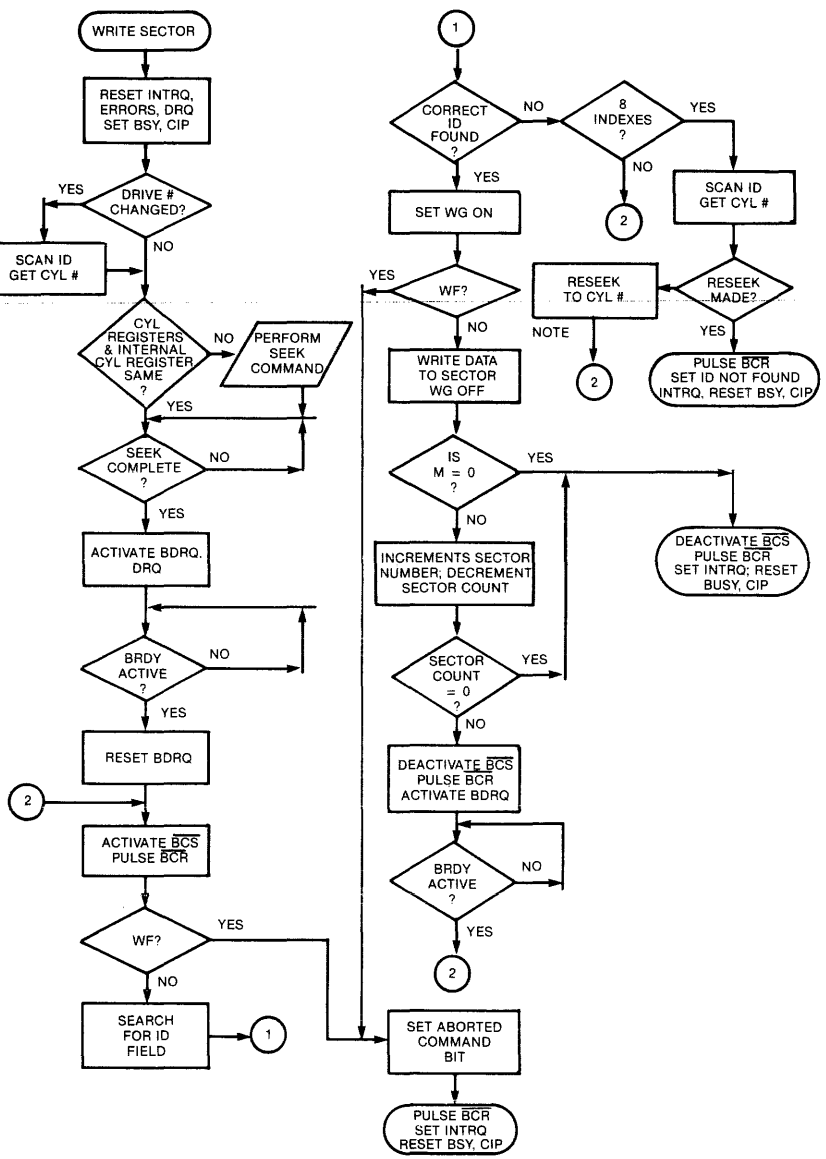
The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1000-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1000-05 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. If the ID field cannot be found within 8 revolutions, the ID not found bit is set and the command is terminated.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY line is asserted after the first sector is read out of the buffer, the WD1000-05 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1000-05 will raise BDRQ and wait for the host to place more data in the buffer.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1000-05:	Strobes $\overline{BCR}$; sets BDRQ = 1, DRQ flag = 1.
(3)	Host:	Loads buffer with data (by $\overline{WE}$ strobes).
(4)	1000-05:	Waits for BRDY = low to high.
(5)	1000-05:	Finds specified ID field, write out sector.
(6)	1000-05:	If M = 0, then interrupt; End.
(7)	1000-05:	Increments sector number, decrements sector count.
(8)	1000-05:	If sector count = 0, then interrupt; End.
(9)	1000-05:	If BRDY = inactive, then (5).
(10)	1000-05:	Go to (2).



SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

After the command is loaded, the seek complete line is sampled until true. The ready and write fault lines are also checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1000-05 will retry up to 8 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 2 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A H'00' is normal; a H'80' indicates a bad block mark for that sector. In the example of Figure 2, sector 04 will get a bad block mark recorded.

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

Figure 2. FORMAT COMMAND BUFFER CONTENTS

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1000-05 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3; for instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of H'4E' are written for Gap 1 and Gap 3.

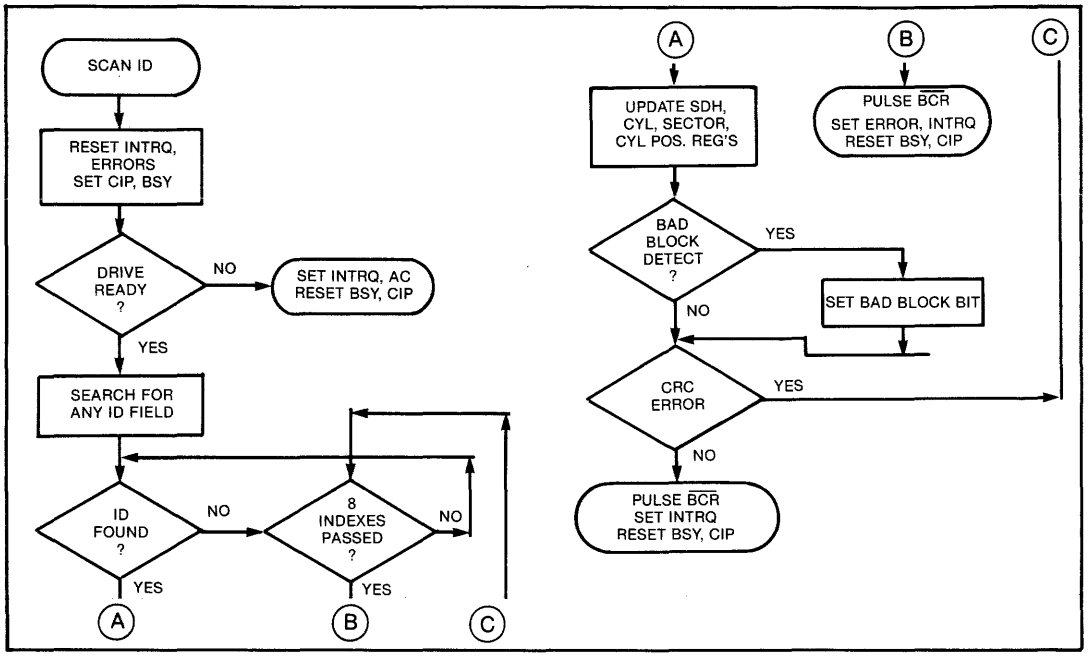
The data fields are filled with H'FF,' and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, H'4E' is filled until index. Like all commands, a write fault or drive not ready condition will terminate the command. Figure 3 shows the format that the WD1000-05 will write on the disk.

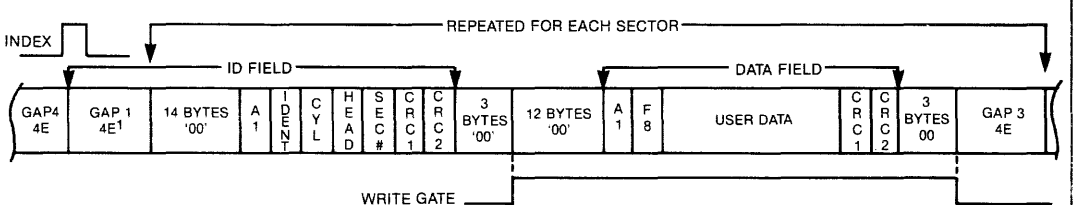
The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E

M = motor speed variation (e.g. .03 for + − 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 3 shows the format that the WD1000-05 will write on the Disk.





ID FIELD

A1 = H'A1' with H'0A' clock.

IDENT = MSB of Cylinder Number
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark

Sec # = Logical Sector Number

DATA FIELD

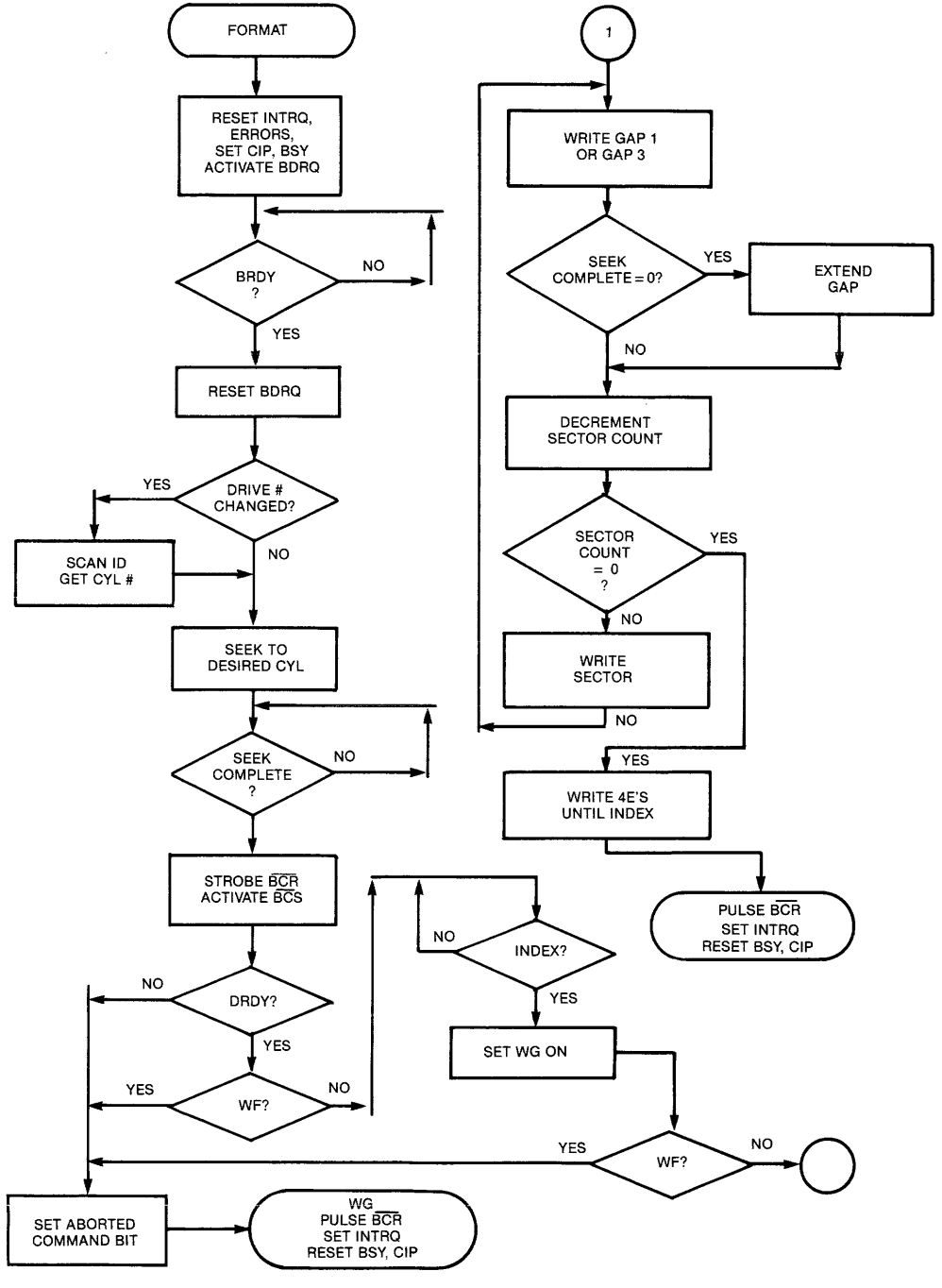
A1 = H'A1' with H'0A' Clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 128 to 1024 Bytes[2]

NOTES:
1. GAP1 and 3 length determined by sector number register contents during formatting.
2. If EXT bit in SDH register is set to 1 then an additional 7 data bytes are written, no CRC bytes are written.

Figure 3. FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY ?
NO
YES
RESET BDRQ
DRIVE # CHANGED?
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE ?
NO
STROBE BCR ACTIVATE BCS
DRDY?
NO
YES
WF?
YES
NO
SET ABORTED COMMAND BIT
WG PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0?
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0 ?
YES
NO
WRITE SECTOR
NO
YES
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP
NO
INDEX?
YES
SET WG ON
YES
WF?
NO

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

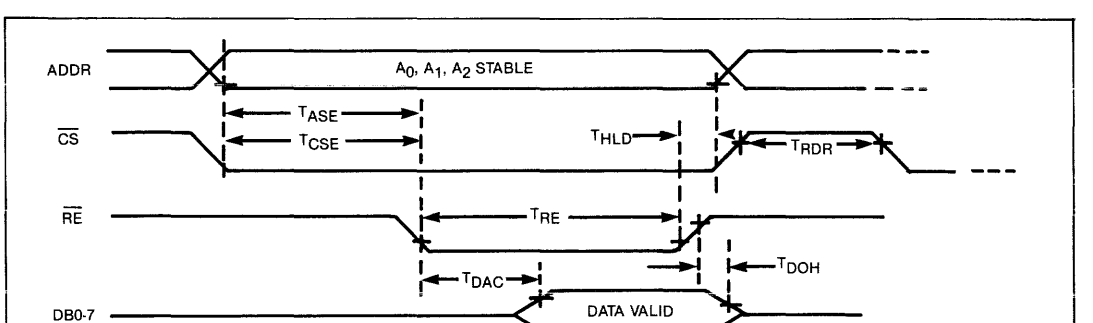
DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Draw)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = −100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	IO = 4.8 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

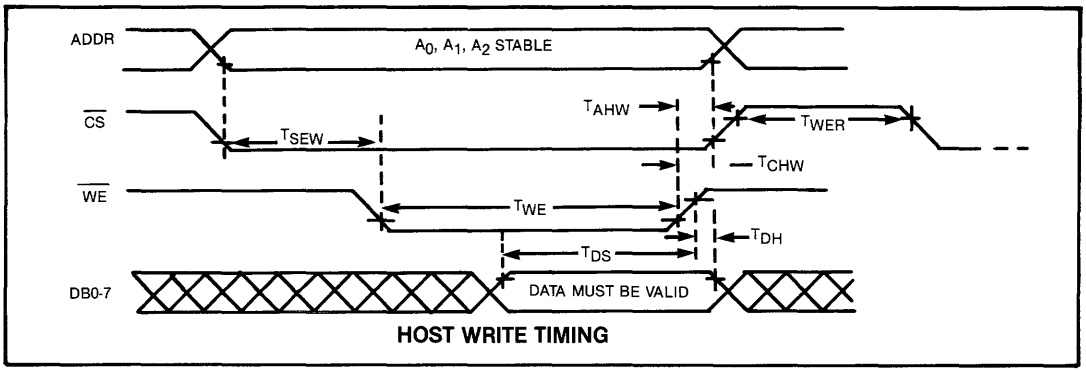
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ± .25V

HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{ASE}	ADDR Setup to $\overline{RE}$	100		ns	
T_{DAC}	Data Valid from $\overline{RE}$		375	ns	
T_{RE}	Read Enable Pulse Width	.4	10	μs	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	ns	
T_{HLD}	ADDR, CS, Hold from $\overline{RE}$	0		ns	
T_{RDR}	Read Recovery Time	300		ns	
T_{CSE}	$\overline{CS}$ Setup To	0		ns	



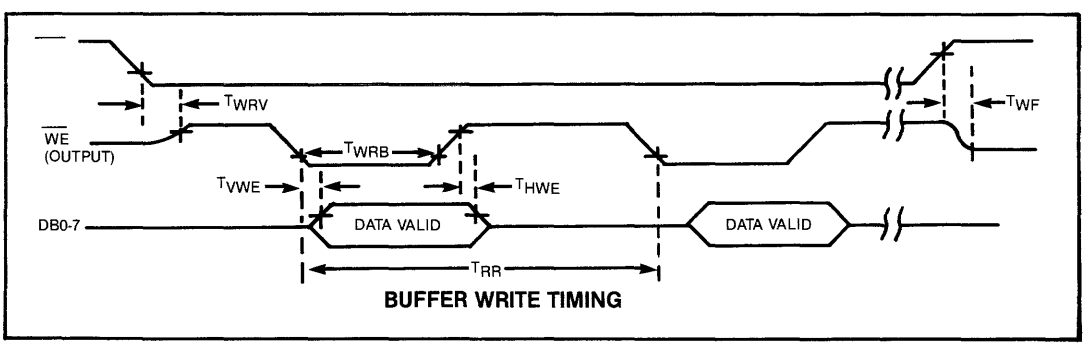
HOST READ TIMING



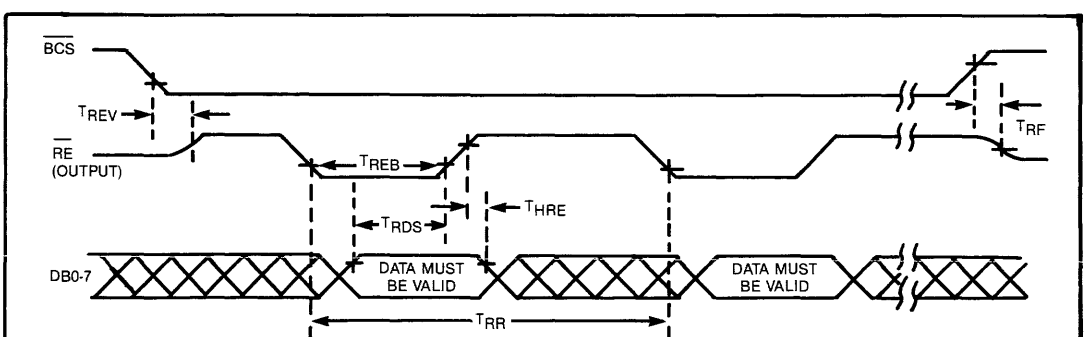
HOST WRITE TIMING

HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T_{SEW}	ADDR, CS Setup to $\overline{WE}$	0	10	µs	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	µs	
T_{WE}	Write Enable Pulse Width	.2	10	µs	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		ns	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		ns	
T_{WER}	Write Recovery Time	1.0		µs	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time	0			



BUFFER WRITE TIMING



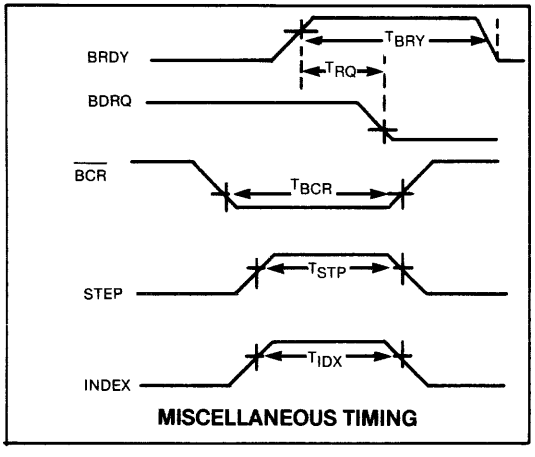
BUFFER READ TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

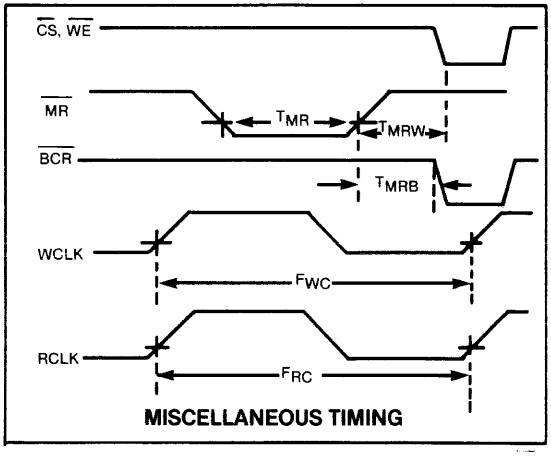
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	ns	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			110	ns	
T_{HWE}	Data Hold from $\overline{WE}$	60			ns	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{WF}	$\overline{WE}$ Float from BCS	15		100	ns	C_L = 50 pf

BUFFER READ TIMING (WRITE SECTOR CMD)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	ns	C_L = 50 pf
T_{REB}	$\overline{RE}$ Output Pulse Width	300	400	500	ns	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			ns	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	µs	See Note 2
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	ns	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			ns	



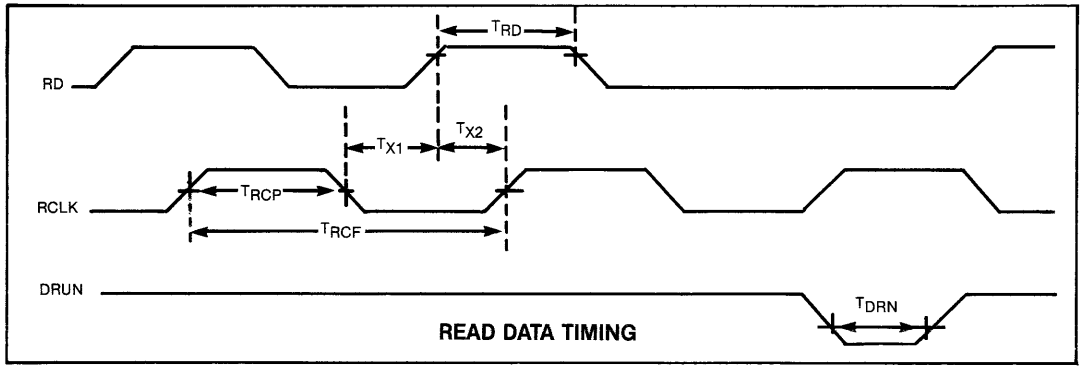
MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

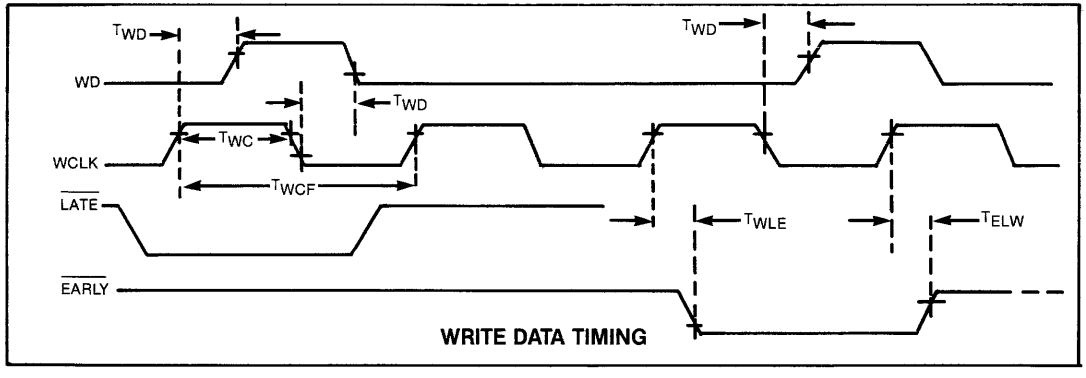
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	ns	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	µs	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	µs	See Note 2
T_{IDX}	Index Pulse Width	5		15	µs	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
F_{RC}	Read Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
T_{BRY}	BRDY Pulse Width	800			ns	See Note 5
T_{MRB}	$\overline{MR}$ Trailing To $\overline{BCR}$	1.6	3.2	6.4	µs	See Note 2
T_{MRW}	$\overline{MR}$ Trailing To Host Write	6.4			µs	See Note 2



READ DATA TIMING

READ DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	ns	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		$T_{RCP} \div 2$	ns	
T_{X2}	RD to RCLK Transition	20		$T_{RCP} \div 2$	ns	
T_{RD}	RD Pulse Width	40		T_{RCP}	ns	
T_{DRN}	DRUN Pulse Width	30			ns	
T_{RCF}	RCLK Frequency	.250		5.25	MHZ	See Note 6



WRITE DATA TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	ns	
T_{WD}	Prepagation Delay WCLK to WD	10		65	ns	
T_{WLE}	WCLK to Leading Early/Late	10		65	ns	
T_{ELW}	WCLK to Trailing Early/Late	10		65	ns	
T_{WCF}	WCLK Frequency	.250		5.25	MHZ	See Note 6

NOTES:
1. AC timing measured at $V_{OH} = 2.0V$, $V_{OL} = 0.8V$, $C_L = 50$ pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. BRDY must be >4 μs or a spurious BDRQ pulse may exist for up to 4 μs after rising edge of BRDY.
6. $T_{RCF} = T_{WCF} \pm 15\%$.

Printed in U.S.A.

WD1001 Winchester Disk Controller

FEATURES

- SINGLE +5V SUPPLY
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROL FOR UP TO 4 DRIVES
- CONTROL FOR UP TO 8 R/W HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- 32 BIT ECC FOR BURST ERROR CORRECTION
- ERROR CORRECTION ON DATA FIELD ERRORS
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD BLOCK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 128, 256, OR 512 BYTES PER SECTOR (SOFTWARE SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON SEEK ERROR
- WD1001-55, -85 SAME FORM FACTOR AS WD1000
- WD1001-05 CAN BE MOUNTED ON 5¼" DRIVE

GENERAL DESCRIPTION

The WD1001 is a stand-alone, general purpose Winchester controller board designed to interface up to four Winchester disk drives to a host processor. The drive signals are based upon the floppy look-alike interface available on the Shugart Associates' SA 1000, the Seagate Technology ST506, the Quantum Q2000, and other compatible drives. All necessary buffers and receivers/drivers are included on the board to allow direct connection to the drive.

Communications to and from the host computer are made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive. The WD1001 is based upon a proprietary chip series, the WD1100, specifically designed for Winchester Control.

ORGANIZATION

The WD1001 has seven on-board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors.

The drive control cable is daisy-chained to each of the four drives. Although there is space for two drive control connectors, only one would normally be used for any particular configuration.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1001.

The host interface connector provides interface signals that are compatible with most microprocessors and mini-computers.

The WD1001 provides dual burst detection and single 5-bit burst correction ECC circuitry. The ECC polynomial has been computer generated for optimum error correction on Winchester Disks.

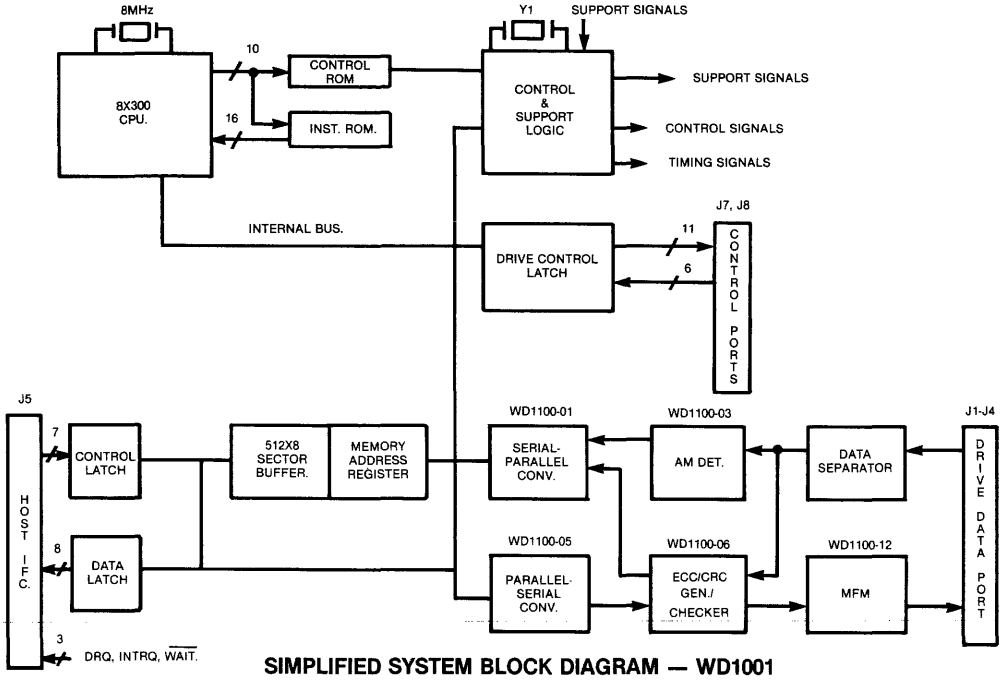
SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (512 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	10 μS to 7.5 mS (0.5 mS increments)
Data Transfer Rate:	4.34 Mbits/sec (WD1001-85) 5.000 Mbits/sec (WD1001-05, -55)
Write Precomp Time:	12 nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3M) max.
Host Cable Length:	3 ft. (1M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.)
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes

DIMENSIONS	WD1001-55, -85	WD1001-05
Length:	9.9 in. (24.9 cm)	8.5 in. (21.6 cm)
Width:	6.8 in. (17.1 cm)	5.75 in. (14.6 cm)
Height:	0.75 in. (1.9 cm)	0.75 in. (1.9 cm)
Mounting Centers:	6.375 x 9.375 in. (16 x 23.6 cm)	3.12 in. (7.9 cm)

HOST INTERFACING

The WD1001 is designed to easily interface to most micro computers and mini-computers. All interfacing



SIMPLIFIED SYSTEM BLOCK DIAGRAM — WD1001

is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers. The only exception is the inclusion of the WAIT line.

WAITS

The $\overline{\text{WAIT}}$ control line goes true whenever either of the following are true:

- The WD1001 is accessing data internally to send to the host during a read operation.
- The WD1001 has not accepted the data from the host during a write operation.

The definition of the $\overline{\text{WAIT}}$ line is very similar to the $\overline{\text{WAIT}}$ signal found on many popular processors. $\overline{\text{WAIT}}$ is also similar to the REPLY signal on Western Digital and other processors.

$\overline{\text{WAIT}}$ will not necessarily make a transition for each access to the WD1001. When the WD1001 can return the requested data within 100 nS, there will be no transition of the $\overline{\text{WAIT}}$ line. This should be interpreted as an instant REPLY on Western Digital Processors.

If the WD1001 cannot return the requested data within 100 nS, it will assert its $\overline{\text{WAIT}}$ line. The period of the $\overline{\text{WAIT}}$ signal will vary from 750 nS to 6 μS with 1.25 μS being about average. The period of the $\overline{\text{WAIT}}$ only approaches 6 μS during a read or write which happens immediately after a command is written to the command register. This means that longer waits may be encountered during the first read or write to any WD1001 register if that first read or write happens within approximately 6 μS of a command being issued.

During the time that $\overline{\text{WAIT}}$ is asserted, the host system **must** hold all of its strobe and address lines stable. On write operations, the DAL lines must also be held stable.

The Host Interface connector (J5) consists of an eight bit bi-directional bus, three bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. See Table 1:

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may write data to a selected register of the WD1000.
28	27	$\overline{RE}$	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the host may read data from a selected register of the WD1001.
30	29	$\overline{WAIT}$	Upon receipt of a $\overline{CS}$, the $\overline{WAIT}$ line may go active. It returns to the inactive state when the DAL lines are valid on a read, or data has been accepted on a write.
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exhausted or until a write or read is performed on the Cylinder Low register.
40	39	MR	The Master Reset line initializes all internal logic on the logic on the WD1001. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset.
	41	Not Connected	Not on WD1001-05
	42	Not Connected	
	43-50	+5V	8 power pins for regulated +5 volts. This power input is also available on J6, pin 3. Not on WD1001-05.
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1001, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Tables 2 and 3:

34 PIN DRIVE CONTROL CONNECTOR (WD1001-05, -55) **TABLE 2**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6	O	Write Gate
7	8	I	Seek Complete
9	10	I	TR000
11	12	I	Write Fault
13	14	O	Head Select 0
15	16	I	Sector
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24	O	Step
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32	O	Drive Select 4
33	34	O	Direction In

DRIVE CONTROL SIGNAL DESCRIPTIONS

RWC

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

Write Gate

This output signal allows data to be written on the disk.

Seek Complete

Informs the WD1001 that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

Track 000

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

50 PIN DRIVE CONTROL CONNECTOR FOR SA1000 TYPE INTERFACE (WD1001-85) **TABLE 3**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6		NC
7	8	I	Seek Complete
9	10		NC
11	12		NC
13	14	O	Head Select 0
15	16	I	Sector
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24		NC
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32	O	Drive Select 4
33	34	O	Direction In
35	36	O	Step
37	38		NC
39	40	O	Write Gate
41	42	I	TR000
43	44	I	Write Fault
45	46		NC
47	48		NC
49	50		NC

Write Fault

Informs the WD1001 that some fault has occurred on the selected drive. The WD1001 will not execute commands when this signal is true.

HS0 HS2

Head Select lines are used by the WD1001 to select a specific R/W head on the selected drive.

Index

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

Ready

Informs the WD1001 that the desired drive is selected and that its motor is up to speed. The WD1001 will not execute commands unless this line is true.

Step

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION IN line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

$\overline{\text{Direction In}}$

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

$\overline{\text{DS1}}$ $\overline{\text{DS4}}$

These four Drive Select lines are used to select one of four possible drives.

DRIVE DATA CONNECTOR

Four data connectors (J1-4) are provided for clock signals and data between the WD1001 and each drive. All lines associated with the transfer of data between the drive and the WD1001 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers that mate with Burndy #FRS20BS. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

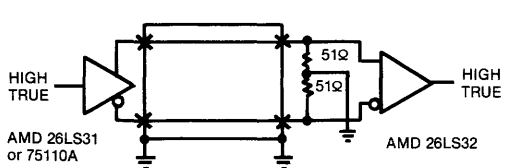
DATA CONNECTIONS AND DESCRIPTIONS

TABLE 4

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1	I	– Drive Selected
4	3		NC
6	5		NC
8	7		NC
	9	O	+ Timing Clock*
	10	O	– Timing Clock*
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

*WD1001-55, -85 only.

DIFFERENTIAL DATA DRIVER/RECEIVER



NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

Z_χ = 105Ω
FLAT RIBBON OR TWISTED PAIR
MAX 10 FT.

POWER CONNECTOR

A three pin Molex connector (J6) is provided for power input to the WD1001-55 and -85. A four pin Amp connector is used on the WD1001-05. See Table 5:

TABLE 5

PIN	WD1001-55, -85	WD1001-05
1	Ground	Not Connected
2	NC	Ground
3	+ 5V Regulated	Ground
4	—	+ 5V Regulated
Housing	Molex 03-07-1032	Amp 1-4840429-0

COMMANDS

The WD1001 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1001 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mispositions, the WD1001 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the WD1001 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. No command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1001 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types which are summarized in Table 6:

TABLE 6

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r_3	r_2	r_1	r_0
I	Seek	0	1	1	1	r_3	r_2	r_1	r_0
II	Read Sector	0	0	1	0	D	M	L	0
III	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

r_3-r_0 — STEPPING RATE

0000 = 35μS	1000 = 4.0mS
0001 = 0.5mS	1001 = 4.5mS
0010 = 1.0mS	1010 = 5.0mS
0011 = 1.5mS	1011 = 5.5mS
0100 = 2.0mS	1100 = 6.0mS
0101 = 2.5mS	1101 = 6.5mS
0110 = 3.0mS	1110 = 7.0mS
0111 = 3.5mS	1111 = 7.5mS

D = DMA Read Mode
0 = Programmed I/O Mode
1 = DMA Mode

L = Long Read/Write
0 = Normal Read/Write
1 = Long Read/Write

M = 1 = Multiple Sector Read/Write
0 = Single Sector Read/Write

NOTE:
The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D = 0), the interrupt will occur before the first DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. If the DMA bit is set (D = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

RESTORE

The Restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the TR000 line goes true. Upon receipt of the Restore command, the Busy bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is rest.

If no errors are encountered thus far, the internal head position register for the selected drive is cleared. The TR000 line is sampled. If TR000 is true, an interrupt is generated and the Busy bit is reset. If TR000 is not true, stepping pulses at a rate determined by the stepping rate field are issued until the TR000 line is activated. When TR000 is activated, the Busy bit is reset and an interrupt is issued. If the TR000 line is not activated within 1023 stepping pulses, the TR000 Error bit in the Error Register and the Error bit in the Status Register are set, the Busy bit is reset and an interrupt is issued.

SEEK

The Seek command positions the R/W head to a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Upon receipt of the Seek command, the Busy bit in the Status Register is set. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is updated, the direction line is set to the proper direction and a step pulse is issued for each cylnder to be read and an interrupt is issued. Note that the Seek Complete line is not sampled after the Seek command, allowing multiple seek operations to be started using drives with buffered seek capability.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1001 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

READ SECTOR

The Read Sector command is used to read a sector of data from the disk to the host computer. Upon receipt of the Read command, the Busy bit in the Status register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line does not go true within 128 Index pulses, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

Once the head has settled over the desired cylinder, the WD1001 will attempt to read the sector. The WD1001 performs all retries necessary to recover the data during the read command. The controller attempts to read the desired sector up to 16 times. It will attempt a retry if it does not find an ID, if the ID of that sector has a bad CRC or if the Data Address Mark (DAM) couldn't be found or even if the data was actually read from the disk but incurred an uncorrectable error.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to read the sector once again. An auto-restore will be performed only once per read or write sector command.

If the WD1001 encounters an ECC error, it will attempt to correct the data in its sector buffer. If it can correct the data, the Corrected bit in the Status

register will be set, if not, the Uncorrectable Error bit is set.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. If the Uncorrectable bit is set, the data that last produced that error will be available in the sector buffer. The Error bit in the Status Register is set and a normal completion is simulated.

READ LONG

This variation of the Read command allows the user to read the ECC check bits directly. The check bits are placed in the data buffer immediately behind the data. This increases the effective buffer length by four bytes.

TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the host to the WD1001 buffer. These commands have implicit stepping rates as set by the last Restore or Seek command.

WRITE SECTOR

The Write Sector command is used to write a sector of data from the host computer to the disk. Upn receipt of the Write command, the controller generates DRQs for each byte to be written to the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

After all data has been sent to the sector buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line doesn't go true within 128 Index pulses, then the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, it will attempt to read the ID of the sector. The WD1001 performs all retries necessary to recover the ID during the write command. The controller attempts to read the ID of the desired sector up to 16 times. It will attempt a retry if it doesn't find an ID or if the ID of that sector has a bad CRC.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to write the sector once again.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. The Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If the proper sector is located, the sector buffer is written to the disk, an interrupt is generated and the Busy bit is reset.

WRITE LONG

This variation of the write command allows the user to introduce various error patterns to check correction capability. The check bits follow the data in the sector buffer. This increases the effective buffer length by four bytes.

FORMAT TRACK

The Format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format command, the controller generates DRQs for each byte of the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

After all data has been sent to the buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault lines are sampled. If an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. No verification of track positioning accuracy is performed because the track may not have any ID fields present. After the Seek operation has been performed, the Seek Complete line is sampled. If the Seek Complete line is not asserted within 128 Index pulses, the Aborted command bit in the Error Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, the controller starts writing a pattern of 4E's until the index is encountered. Once the index is found, a number of ID fields and nulled data fields are written to the disk. The number of sectors written is equal to the contents of the Sector Count Register. As each sector is written, the Sector Count Register is decremented, and consequently, must be updated before each format operation.

NOTE:

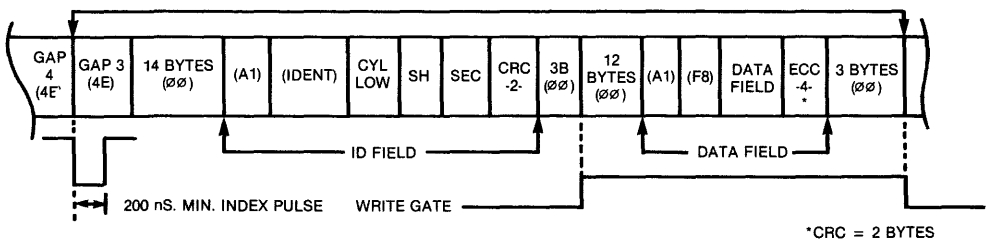
1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's ECC or CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high

These values are:

FE = 0 to 255 cylinders
FF = 256 to 511 cylinders
FC = 512 to 767 cylinders
FD = 768 to 1023 cylinders

6) GAP 3 values are:

SECTOR LENGTH	GAP 3
128	15
256	15
512	30



After the last sector is written, the controller backfills the track with 4E's. When the next index pulse after the last sector is written is encountered, the format operation is terminated, an Interrupt is generated and the Busy bit is reset.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1001 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1001 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1001 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/head	Size/Drive/head
0	1	1	1	Status Register	Command Register

SDH REGISTER

BIT	7	6 5	4 3	2 1 0
FUNCTION	Sec Ext	Sec Size	Drive Select	Head Select

BIT 7	SECTOR EXTENSION
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Drive Sel 1
0	1	Drive Sel 2
1	0	Drive Sel 3
1	1	Drive Sel 4

BIT 2	BIT 1	BIT 0	HEAD SELECTED
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	Uncorrectable
5	Write Fault	CRC Error — ID Field
4	Seek Complete	ID Not Found
3	Data Request	—
2	Corrected	Aborted Command
1	—	TR000 Error
0	Error	DAM not found

PROGRAMMING

Users familiar with floppy disk systems will find programming the WD1001 a pleasant surprise. A substantial amount of intelligence that was required by the host computer has been incorporated into the WD1001. The WD1001 performs all needed retries, even on data ECC and head positioning errors. Most commands feature automatic 'implied' seek which means that seek commands need not be issued to perform basic read/write functions. The WD1001 keeps track of the position of up to four read/write head assemblies, so the host system does not have to maintain track tables. All transfers to and from the disk are through an on-board full sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1001 simulates a normal completion so that special error recovery software is not needed.

ERROR CORRECTION

General Description

The WD1001 with ECC is specifically designed to add error correction capabilities to 8″ or 5.25″ Winchester disk drives. The Polynomial selected is a computer generated code, optimized for sector sizes of 128, 256 and 512 byte data fields. The forur ECC bytes appended by this device enable correction of a single burst of 8 bits. Simultaneously it can detect a double burst of two bits in error.

During a write operation, the input stream is divided by the polynomial, X32 + X28 + X26 + X19 + X17 + X10 + X6 + X2 + 1 and the resulting 32 bit remainder is used as the four check bytes. In a Read operation the check bit are recomputed and compared to the recorded check bits to generate the four syndrome bytes. If the syndrome is zero, no errors were detected. Otherwise, the non-zero syndrome is used by the ECC processor to compute the displacement and the error vector within the sector. This information is then used to correct the data if a single burst of no more than 5 bits in error occurred.

Data Accuracy

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be reread before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected, erroneous data by rereading until the error goes away.

Correction is applied only after the syndrome has been received and has the following parameters:

1. Single burst detection span with correction = 20 bits with max. correction span = 5 bits
2. Double burst detection span with correction = 4 bits with max. correction span = 5 bits
3. Non detection probability = 2.3 E-10
4. Miscorrection probability = 8.00 E-6 for max. correction span = 5 bits (256 byte Sector)

*All parameters given with respect to a 256 byte record length.

Correction Time Performance

All real time operations are performed with error correction hardware. The software algorithims used on the WD1001 get involved only after an error has been detected.

The following correction times are for a serial algorithim such as that used on the WD1001:

a) 30mS max.
b) 15mS min.
c) 20mS ave.

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PRELIMINARY

WD1002-05 Winchester/Floppy Controller

FEATURES

- SINGLE +5V POWER SUPPLY.
- CONTROL FOR UP TO 3 WINCHESTER AND 4 FLOPPY DRIVES.
- ON BOARD DATA SEPARATOR AND WRITE PRECOMPENSATION.
- 128, 256, 512, AND 1024 BYTE SECTOR SIZES.
- PROGRAMMABLE SECTOR SIZES TO 1K.
- AUTOMATIC TRACK FORMATTING ON HARD AND FLOPPY DISKS.
- MULTIPLE SECTOR OPERATIONS.
- 5 BIT SINGLE BURST ERROR CORRECTION ON WINCHESTER.
- CRC GENERATION/VERIFICATION ON ID FIELDS.
- 5 MBIT DATA TRANSFER RATE.
- ECC DIAGNOSTIC COMMANDS (READ LONG & WRITE LONG).

DESCRIPTION

The WD1002-05 Winchester-Floppy Controller (WFC) is a stand-alone general purpose board designed to interface up to three 5¼" Winchester hard disks and up to four 5¼" floppy disk drives. The WFC implements all the logic required for a variable length sector (to 1K bytes), ECC correction, data separation and host interface circuitry. The Winchester interface is based on the Seagate ST506 and the floppy interface on the Shugart SA450. All necessary buffers and drivers/receivers are on board.

Communication to and from the host is made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on-board sector buffer allows data transfers to the host computer at a rate independent of the drive transfer rate.

The WD1002-05 Controller board is based on the WD1014 EDS device and 1015 Buffer Controller device, as well as the WD2797 Floppy Disc Controller and WD1010 Winchester Disk Controller chips. It is form factor compatible with most 5¼" Winchesters and may be directly mounted on the drive.

ARCHITECTURE

The Block Diagram of the WD1002-05 is shown in Figure 1. The heart of the system is the WD1015 Buffer/Controller, which generates and processes all data and control lines, along with the WD1014 EDS that generates all control signals that cannot be handled in real time by the WD1015.

Commands, parameters, and data are entered via the Host Interface Logic. The WD1015 accepts both floppy and Winchester commands in identical format, converting these parameters to the WD2797/WD1010 protocol. Data is read from the selected drive and transferred to the sector buffer. If an error in the data field has been encountered, the WD1015 will instruct one of the controllers to perform retries automatically. In the case of an access on a Winchester drive, the WD1014 ECC device will be enabled and error correction procedures will be invoked. Error Correction may be disabled via software from the Host to allow "CRC-only" formatted Winchester drives to be used in the system. Data Separation and Write Precompensation Logic is on-board for Winchester transfers, while the WD2797 Floppy Controller provides an integrated separator and ajustable precomp. After the sector buffer is full, the WD1015 informs the Host Interface Logic that data may be read by the Host. The use of an on-board sector buffer provides both transparent error correction and data transfers to the Host that are independent of drive transfer rates.

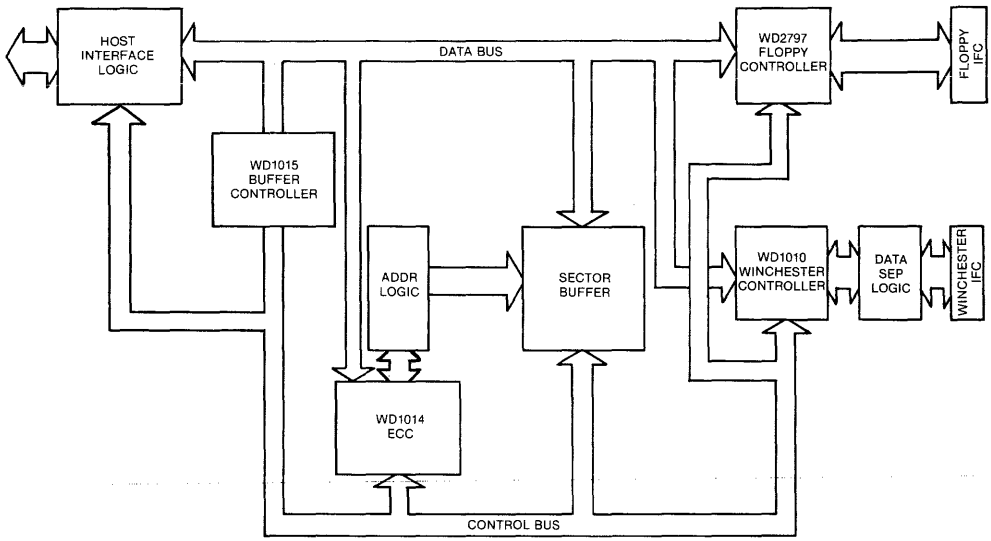

Figure 1. WD1002-05 BLOCK DIAGRAM

HOST INTERFACE

The WD1002-05 has been designed to interface to a Host processor via a parallel port or CPU bus configurations. The specific signals are compatible with the Western Digital WD1000/WD1001 series of Winchester-only controller boards. With the inclusion of the WD1015, the previous WAIT signal is no longer necessary but has been provided for compatibility; status information is always available to the Host for monitoring command progress. When the Busy bit is set, no other status bits are valid.

The Host Interface connector (J5) consists of an 8 bit bi-directional bus, three address lines, and read and write strobes. All functions within the WD1002-05 are initiated by the Host Interface.

HOST INTERFACE CONNECTOR

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written vis the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may read data to a selected register of the WD1002-05.
28	27	$\overline{RE}$	When Read Enable is active along with $\overline{CS}$, the host may read data from a selected register of the WD1002-05.
30	29	Pull-Up (PUP)	Used only when replacing WD1000 or WD1001 with WD1002-05. Tied to a pull-up resistor.
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.
38	37	DRQ	The data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the buffer has been exhausted or filled by the host.
40	39	MR	The Master Reset line initializes all internal logic on the logic on the WD1002-05. Sector Number, Cylinder Number and SDH are cleared, stepping rate for Winchester devices are set to 7.5 mS, stepping rate for floppies is set to 40 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset.
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONNECTORS

Six connectors are provided for connection of up to 3 Winchester and 4 Floppy drives. All applicable drivers and receivers have been included on the board to allow direct connections to the drives. All signals to the Floppies are daisy-chained and require the last (or only) drive to contain termination resistors.

The Winchester control cable is also daisy-chained and requires similar termination. Most Floppy/Winchester drives can be configured to provide this. The data cables on the Winchester are radially connected to each drive. Three data cable connectors are included on the board.

FLOPPY DRIVE CONTROL/DATA CONNECTOR

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2		NC
3	4		NC
5	6	O	Drive Select 1
7	8	I	Index/Sector
9	10	O	Drive Select 2
11	12	O	Drive Select 3
13	14	O	Drive Select 4
15	16	O	Motor On
17	18	O	Direction In
19	20	O	Step
21	22	O	Write Data
23	24	O	Write Gate
25	26	I	Track 00
27	28	I	Write Protect
29	30	I	Read Data
31	32	O	Side Select
33	34		NC

34 PIN WINCHESTER DRIVE CONTROL CONNECTOR

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6	O	Write Gate
7	8	I	Seek Complete
9	10	I	TR000
11	12	I	Write Fault
13	14	O	Head Select 0
15	16		NC
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24	O	Step
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32		NC
33	34	O	Direction In

WINCHESTER DRIVE DATA CONNECTIONS AND DESCRIPTIONS

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1		NC
4	3		NC
6	5		NC
8	7		NC
10	9		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

POWER CONNECTOR

A four pin AMP connector is used for power input to the WD1002-05. The pin-outs are as shown:

POWER CONNECTOR

PIN	SIGNAL NAME
1	NC
2	GROUND
3	GROUND
4	+ 5V REGULATED

COMMANDS

The WD1002-05 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1002-05 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mis- positions, the WD1002 will automatically perform a restore and a re-seek. If the error is completely uncoverable, the WD1002-05 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. On Write/Format operations, the Sector buffer must be filled with the required data before the command can be executed by the WD1002-05. On Winchester drives no command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1002-05 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types:

TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r3	r2	r1	r0
I	Seek	0	1	1	1	r3	r2	r1	r0
II	Read Sector	0	0	1	0	D	M	L	0
II	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

R_3-R_0 = STEPPING RATES

$R_3R_2R_1R_0$	Winchester	Floppy
0 0 0 0	20 μsec	≈15 μsec
0 0 0 1	0.5 msec	1 mS
0 0 1 0	1.0 msec	2
0 0 1 1	1.5 msec	3
0 1 0 0	2.0 msec	4
0 1 0 1	2.5 msec	5
⋮	⋮	6
1 1 1 1	7.5 msec	6
		8
		8
		10
		12
		14
		16
		18
		20
		25
		40

D = DMA Read Mode

D = 0, Programmed I/O Mode
D = 1, DMA Mode

L = Read/Write Long

L = 0, Normal R/W Transfer
L = 1, R/W ECC Bytes from Host

M = Multiple Sector

M = 0, Single Sector R/W
M = 1, Multiple Sector R/W

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

Restore

The Restore command is used to move the R/W heads to the Track 0 position. It is usually performed after a power-up operation. When Restoring a Winchester drive, the specified stepping rate is not used; the actual Restore rate is handshaked with Seek Complete Time. When Restoring on a floppy drive, the R_3-R_0 rate is used when the rate is equal to or slower than 8 mS. On rates faster than 8 mS, the restore stepping rate defaults to 8 mS. On both floppy and Winchester, the rate is stored for subsequent implied Seeks for Read/Write commands.

Seek

The Seek command is used to position the Read/Write heads to a specified location. Since the Read and Write commands feature implied Seek, this command is normally used to perform simultaneous (overlap Seek) operations on multiple drives. The specified stepping rate is used for Track to Track access time.

The desired location is loaded into the cylinder registers prior to issuing the command. On Winchester drive, the Write Fault, Seek Complete, and Ready lines must be true for the command to execute. The Seek Complete line is not checked after all stepping pulses have been issued. A Seek operation on a floppy drive will be performed regardless of the state of Write Protect on the Drive Interface.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1002-05 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

Read Sector

The Read Sector command is used to transfer a specified sector from any drive to the Host buffer. The stepping rate, specified in an earlier Restore or Seek command, is used to automatically perform a Seek prior to execution of the Read. After the task file has been loaded with the desired parameter, the on-board sector buffer is filled with the data from the disk. The Host may then read this data by accessing the data register repeatedly.

The 'D' Flag allows the Interrupt line (INTRQ) to be activated when the data is available. The Data Request signal is always activated when the WD1002-05 either needs data (in the case of the Write commands) or has data available for the Host. If the 'D' Flag is not set, then the INTRQ will be activated before start of data transfer. If set, then INTRQ will be set after the last byte of the last sector has been transferred to the host.

The 'L' Flag allows the Host to both Read and Write and ECC polynomial to a Winchester drive. This function may be used for diagnostic and performance purposes by allowing the Host to compute and check ECC operation. Since the floppy disk format does not allow ECC, the 'L' Flag is a "don't care" bit in this case.

The 'M' Flag allows multiple sectors to be transferred via one command. The Sector Count register in the task file is used to specify the number of sectors to be transferred from a track. Retries and ECC correction (if applicable) will be performed on each sector.

Write Sector

The Write Sector command is used to transfer a block of data from the on-board buffer to a specified sector. After the command is issued, the WD1002-05 generates a DRQ and the Host proceeds to fill the buffer. Once filled, the desired sector is searched for. This may include an implied Seek. After the ID field is found the Write Gate signal is activated and the data is MFM encoded and written serially to the selected drive. The Write Precompensation Register in the task file specifies the starting cylinder on a Win-

chester drive where precomp is to be enabled. The WFC is configured with no precompensation when writing to the floppies. The user may cut the etch on WD2797 pin 1 so that precomp is always enabled or jumper it to pin 29 so that precomp is enabled for tracks greater than 43.

The option Flags 'L' and 'M' are also available and work exactly as described in the Read Sector command.

TYPE III COMMANDS

Format Track

This command is used to format a drive prior to reading or writing. It causes ID fields, gaps, and all information to be written to a selected Track for initialization. The on-board sector buffer serves a different purpose for this command; it contains the Bad Block Flag and the physical numbers of the sectors to be recorded. Since the actual sector numbers are now taken from the buffer, unlimited Interleaving is allowed. The Sector Count register in the task file, normally used during a multiple sector R/W, now specifies the number of sectors to be formatted. The Format Track command also features the implied Seek option, so that the entire drive can be formatted by incrementing the cylinder number after each execution.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1002-05 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1002-05 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1002-05 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp*
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High**	Cylinder High**
0	1	1	0	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

*Not used on Floppy

**When LSB = 1, permits 48 t.p.i. Floppy disk to be read on 96 t.p.i. Floppy disk system.

SDH REGISTER

BIT	7	6 5	4 3	2 1 0
Function	Sec Ext	Sec Size	Drive Select	Head/ Drive Select

BIT 7	SECTION EXTENSION (WINCHESTER ONLY)
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	0	1024 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Winchester Drive Sel 1
0	1	Winchester Drive Sel 2
1	0	Winchester Drive Sel 3
1	1	Floppy Drive Sel

BIT 2	BIT 1	BIT 0	WIN-CHESTER HEAD NR	FLOPPY DRIVE & HEAD NRS
0	0	0	0	DR1 HD0
0	0	1	1	DR1 HD1
0	1	0	2	DR2 HD0
0	1	1	3	DR2 HD1
1	0	0	4	DR3 HD0
1	0	1	5	DR3 HD1
1	1	0	6	DR4 HD0
1	1	1	7	DR4 HD1

STATUS & ERROR REGISTERS

The Status Register is used to monitor command flow and to supply the Host with specific information about the drive. A bit called "Busy" (Bit 7) indicates that the WD1002-05 is executing a current command and register access is prohibited. This bit can be read at any time by the host but all other bits are invalid when this status bit is set.

The Error Register is used to report different types of errors caused by execution of the last command. To ease programming, the LSB of the STATUS register will be set if any of the bits in the error register are also set.

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	ECC/CRC Error Data Field
5	Write Fault	—
4	Seek Complete	ID Not Found
3	Data Request	—
2	Corrected Data	Aborted Command
1	—	TR000 Error
0	Error	DAM Not Found

SPECIFICATIONS:

	HARD DISK	FLOPPY DISK
Encoding method:	MFM	MFM
Cylinders per Head:	Up to 1024	Up to 245
Sectors per Track:	Up to 64	Up to 64
Heads:	8	2
Drive Selects:	3 (ST506)	4 (SA450)
Step Rate:	35 μS to 7.5 mS (0.5 mS increments)	0-40 mS (1 of 16 rates in this range)
Data Transfer Rate:	5.0 Mbits/sec	250 Kbits/sec
Write Precomp Time:	12 nsec	100-300 nsec adj.
Sectoring:	Soft	
Host Interface:	8 Bit bi-directional bus	
Drive Cable Length:	10 ft (3M) max.	
Host Cable Length:	3 ft (1M) max.	
Power Requirements:	+5V ± 5%, 3.0A Max.	
Ambient Temperature Operating:	0°C to 50°C (32°F to 122°F)	
Relative Humidity:	20% to 80%	
MTBF:	10,000 POH	
MTTR:	30 minutes	
Length:	8.00 in	
Width:	5.75 in	
Height:	0.75 in	
Mounting Centers:	7.50 X 5.250 in	

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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PRELIMINARY

WD1002-SHD Winchester Disk Controller

FEATURES

- SINGLE +5V SUPPLY
- SASI™ HOST INTERFACE
- CONTROL FOR UP TO 2 WINCHESTER DRIVES, UP TO 8 R/W HEADS EACH
- 32 BIT ECC FOR WINCHESTER DATA CORRECTION
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD TRACK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 256 OR 512 BYTES PER SECTOR
- SELECTABLE INTERLEAVE
- MULTIPLE SECTOR READS AND WRITES
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- OVERLAPPED SEEKS
- IMPLIED SEEKS
- 0°C to 55°C OPERATIONS

DESCRIPTION

The WD1002-SHD is a stand alone, general purpose Winchester Controller Board designed to interface up to two Winchester Disk Drives to a Host Processor. The Winchester Drive signals are based upon the Floppy look-alike interface available on the Seagate Technology ST506 and other compatible drives. All necessary receivers and drivers are included on the board to allow direct connection to the drive.

Communications to and from the Host Computer are made via a separate computer access port. This port conforms to the popular Shugart Associates System Interface (SASI). It consists of control signals and an 8-bit bi-directional bus. All data to be written to or read from the disk, status information, and command parameters are transferred via this bus. An on-board Data Buffer allows bus transfers to be executed independently of the actual Data Transfer of the drive.

The WD1002-SHD is based upon the WD1010, and WD1100-13, specifically designed for Winchester disk drive control.

SASI™ is a trademark of Shugart Assoc.

ARCHITECTURE

The WD1002-SHD has five on-board interface connectors. Other connectors are for test only and should not be used.

The five connectors consist of a Power Connector, Host Interface Connector, Winchester Drive Control Connector and Two Winchester Data Cable Connectors.

The Winchester Drive Control Cable is daisy-chained to the drive. The drive Data Connectors carry differential signals and are radially connected.

The Host Interface Connector provides a path to the Host thru a SASI bus. Other SASI-Compatible controllers may also be connected to the same bus.

SPECIFICATIONS:

DRIVE INTERFACES

Encoding Method	MFM
Cylinders per Drive	Programmable
Bytes per Sector	Selectable, 256 or 512
Sectors per Track	32 (256 bytes/sector) 17 (512 bytes/sector)
Head Selects	8
Drive Selects	2
Stepping Rates/Algorithms	Programmable
Data Transfer Rate	5Mbits/sec
Write Precomp Time	12 nsec
Sectoring	Soft
Max Cable Length	
Control (Total Daisy Chain)	6M (20ft.)
Data (Radial — each)	6M (20ft.)

HOST INTERFACE

Type	SASI
Max Cable Length (Total Daisy Chain)	4.5M (15ft.)
Termination	Socketed 220/330 pack
Addressing	Jumperable, 0 to 7

POWER

Voltage	5V + 5%
Current	2.0A Max, 1.5A TYP
Ripple	.1 volts max, .1 to 25MV

MECHANICAL

Length	8″
Width	5.75″
Height (Max incl leads, board, & components)	.75″

ENVIRONMENTAL — OPERATING

Ambient Temperature	0° to 55°C
Relative Humidity	10% to 90% condensing
Altitude	0 to 3000M (10,000 ft)

CONNECTORS

MECHANICAL INFORMATION

Table 1 defines the connectors and a source for the mating connectors on the associated cables. The connector locations may be found in figure XX.

Table 1. CONNECTORS

REFERENCE DESIGNATION	INTERFACE FUNCTION	EQUIVALENT MATING CONNECTOR
P1	Power	AMP1-480424-0 (Housing) AMP350078-4 (Pins) AMP88379-8
P2	SASI Bus	
J1	Winchester Control (Daisy-Chain)	AMP88373-3
J2, J3	Winchester Data (Radial)	AMP88377-4
J4	Test — do not use	

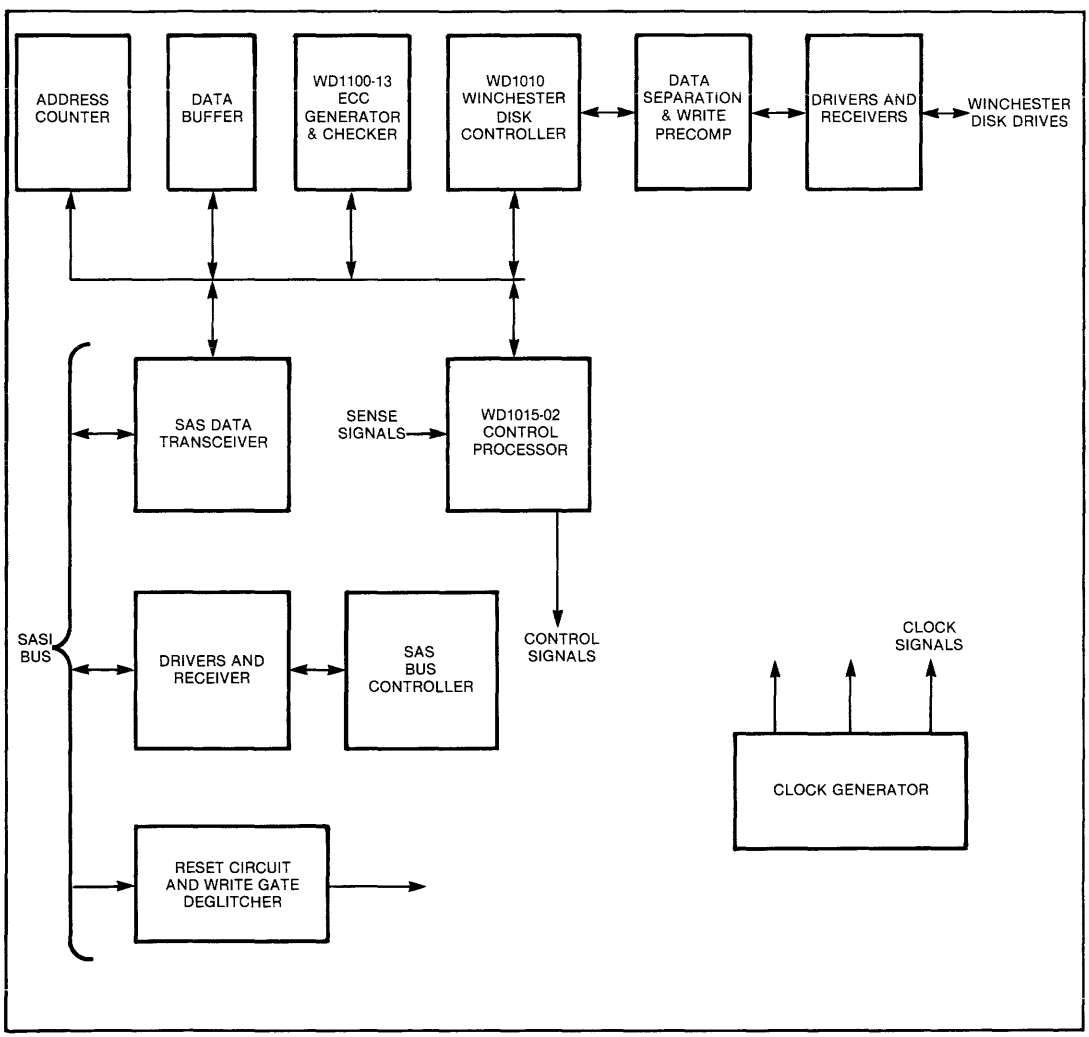


Figure 1. WD1002-SHD BLOCK DIAGRAM

HOST INTERFACING

The WD1002-SHD Controller has been designed to interface to the Shugart Associates System Interface (SASI) bus. All interfacing is done through the SASI connector (P2). Up to eight SASI compatible devices (including the Host) may be connected to this bus. The cable terminating resistor pack is socketed on the controller to aid flexibility in daisy-chaining bus devices. The controller is shipped from the factory configured to respond to SASI device address 0. This may be changed by the user to any SASI address (0 through 7).

HOST INTERFACE CONNECTOR

The host interface connector is a 50 pin vertical header. The connector pin-outs are as follows:

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
1	2	DATA 0 (LSB)	Bi-directional bytewide bus bits D0-D7.
3	4	DATA 1	
5	6	DATA 2	
7	8	DATA 3	
9	10	DATA 4	
11	12	DATA 5	
13	14	DATA 6	
15	16	DATA 7 (MSB)	
17	18	SPARE	
19	20	SPARE	
21	22	SPARE	
23	24	SPARE	
25	26	SPARE	
27	28	SPARE	
29	30	SPARE	
31	32	SPARE	
33	34	SPARE	
35	36	BUSY	Controller-to-host signal whose falling edge acknowledges receipt of SEL and own address. Rising edge indicates transaction complete.
37	38	ACK	Host-to-controller handshake for byte transfers (both edges used).
39	40	RST	100 nsec low level initiate (host-to-controller).
41	42	MSG	Controller-to-host MESSAGE signal to indicate type of bus transfer (see INFORMATION TRANSFER PHASE).
43	44	SEL	Host-to-controller low level signal gives control of bus to address target.
45	46	C/D	Controller-to-host COMMAND/DATA signal used to indicate type of bus transfer (see INFORMATION TRANSFER PHASE).
47	48	REQ	Controller-to-host handshake for byte transfers (both edges used).
49	50	I/O	0 = INPUT to host. 1 = OUTPUT from host. (see INFORMATION TRANSFER PHASE)

WINCHESTER DRIVE CONTROL CONNECTOR

The drive control connector is a 34 pin PC card edge connector that provides a low speed bus that is daisy chained to each of the Winchester drives in the system. To properly terminate the open collector outputs from the WD1002-SHD, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. No other drives should have this termination. The drive control signals and pin-outs are as follows:

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME (I/O)	DESCRIPTION
1	2	$\overline{RWC}$ (O)	When the Reduce Write Current ($\overline{RWC}$) line is activated by Write Gate ($\overline{WG}$), a lower write current is used to compensate for a greater bit packing density on the inner cylinders. $\overline{RWC}$ is only valid when $\overline{WG}$ is low.
3 13 17	4 14 18	$\overline{HS2}$ (O) $\overline{HS0}$ (O) $\overline{HS1}$ (O)	Head Select lines are used by the WD1002-SHD to select a specific R/W head on the drive.
5	6	$\overline{WG}$ (O)	Write Gate ($\overline{WG}$) enables data to be written on the disk. Special circuitry has been included to ensure that this signal will not "glitch" at power-on. This enables the disk drive to remain powered on while the WD1002-SHD power is being cycled.
7	8	$\overline{SC}$ (I)	Seek Complete ($\overline{SC}$) informs the WD1002-SHD that the head of a selected drive has stabilized.
9	10	$\overline{TR000}$ (I)	Track 000 ($\overline{TR000}$) indicates that the R/W heads are positioned on the outermost cylinder.
11	12	$\overline{WF}$ (I)	Write Fault ($\overline{WF}$) informs the WD1002-SHD that some fault has been detected by the selected drive.
15	16		NC
19	20	$\overline{IND}$ (I)	Index ($\overline{IND}$) indicates the index point for synchronization during formatting. $\overline{IND}$ is also used as a time-out mechanism for retries. $\overline{IND}$ should pulse once for each disk rotation.
21	22	$\overline{RDY}$ (I)	Ready ($\overline{RDY}$) informs the WD1002-SHD that the desired drive is selected and its motor is up to speed.
23	24	$\overline{STEP}$ (O)	$\overline{STEP}$ is pulsed for each desired step. The direction of the step is determined by the $\overline{DIRIN}$ line.
25 27	26 28	$\overline{DS0}$ $\overline{DS1}$	The Drive Select bits ($\overline{DS0}$-$\overline{DS1}$) are used to select either drive 1 or drive 2.
29	30		NC
31	32		NC
33	34	$\overline{DIRIN}$	Direction In ($\overline{DIRIN}$) determines the direction of movement of the R/W heads when $\overline{STEP}$ is pulsed: $\overline{DIRIN}$ = 1 = direction out $\overline{DIRIN}$ = 0 = direction in

WINCHESTER DRIVE DATA CONNECTOR

Two data connectors are provided for data transfer between the controller and each drive. All lines associated with the transfer of data between the drive and the controller are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers. The cable pinouts are as follows:

SIGNAL GROUND	SIGNAL PIN	(I/O)	SIGNAL NAME
2	1	I	Drive Selected
4	3	—	NC
6	5	—	NC
8	7	—	NC
10	9	—	NC
12	11	—	GND
	13	O	+ MFM Write Data
	14	O	− MFM Write Data
16	15	—	GND
	17	I	+ MFM READ DATA
	18	I	− MFM READ DATA
20	19	—	GND

POWER CONNECTOR

A four pin AMP connector is provided for power input to the board. The pin-outs are as follows:

PIN	SIGNAL
1	NC
2	GROUND
3	GROUND
4	+ 5 V regulated

HOST INTERFACE DETAILED BUS OPERATION

With regard to bus operations, time can be partitioned into the following mutually exclusive phases:

1. Reset
2. Bus Free
3. Target Selection
4. Information Transfer
5. Bus Release

Bus Phase Sequencing

A Reset Phase may occur at any time. It is followed by the Bus Free Phase. In the absence of a Reset Phase, the bus alternates between the Bus Free Phase and one Transaction.

A Transaction always consists of the following sequence:

1. one Target Selection Phase
2. one or more Information Transfer Phases
3. one Bus Release Phase

The five bus phases are described below. The Information Transfer Phase is broken down into its mutually exclusive categories, which are also called phases.

1. RESET PHASE

Defined as the time $\overline{\text{RESET}}$ is low. It is used by a host to force the controller(s) on the bus to the same state as that following a power on condition.

2. BUS FREE PHASE

Defined as the time between completion (Bus Release Phase) of one Transaction and initiation (Target Selection Phase) of the next Transaction. It can also be thought of as the time during which no unit has control of the bus. All eight control lines are high. The Data Lines are in an undefined state.

3. TARGET SELECTION PHASE

This phase begins when the host places a target address on the bus. The host then brings $\overline{\text{SEL}}$ low. The phase ends when the target corresponding to that address responds by bringing $\overline{\text{BUSY}}$ low. Note: the host must bring $\overline{\text{SEL}}$ high before completion of the current Transaction (end of next Bus Release Phase).

The target address consists of one of $\overline{\text{D0}}$ through $\overline{\text{D7}}$ low and the other seven high. The controller's default address corresponds to $\overline{\text{D0}}$ low. It may be changed to any address by jumpering. Two controllers may not have the same address.

4. INFORMATION TRANSFER PHASE

This phase is used to transfer one or more bytes over the bus. It begins when the currently selected controller sets $\overline{\text{I/O}}$, $\overline{\text{C/D}}$, and $\overline{\text{MSG}}$ to one of the five legal combinations in the following table. This indicates to the host the type of byte transfer(s) which will follow.

$\overline{\text{I/O}}$	$\overline{\text{C/D}}$	$\overline{\text{MSG}}$	TYPE OF TRANSFER PHASE	NUMBER OF BYTES
1	0	1	Command Block (from host)	6
1	1	1	Data Block (from host)	3, 8, 256, 260, 512 or 516
0	1	1	Data Block (to host)	1, 4, 256, 260, 512 or 516
0	0	1	Status Byte (to host)	1
0	0	0	Message Byte (to host)	1

For each byte transferred, the following operations must occur in sequence to perform the asynchronous handshake.

1. The controller brings $\overline{REQ}$ low
2. The host brings $\overline{ACK}$ low
3. The controller brings $\overline{REQ}$ high
4. The host brings $\overline{ACK}$ high

For controller to host transfers, the eight bits are valid on the bus at least 125 nsec before $\overline{REQ}$ goes low. For host to controller transfers, they must be valid on the bus no later than 375 nsec after $\overline{ACK}$ goes low. Note: for debugging, it is useful to know that bytes are valid on the bus at the rising edge of $\overline{REQ}$ during any transfer.

The Command Block Transfer Phase is used to send a block of parameters to the controller. This block specifies the operation to be performed (e.g. Format Disk).

The Data Transfer Phase is primarily used to send one or more sectors of data (with or without ECC) in either direction. It is also used to send an extra block of parameters to the controller or to send byte(s) of controller operational information to the host. During the Status Transfer Phase, byte(s) are sent to the host. They are encoded to indicate the nature of errors that may have been detected.

During the Message Byte Transfer Phase, one byte of all zeroes is sent to the host. This is necessary to satisfy the protocol.

5. BUS RELEASE PHASE

This phase is simply the low-to-high transition of $\overline{BUSY}$. This event signifies to the host that the current Transaction has terminated and the associated target is no longer controlling the bus.

Now in more detail, a transaction always consists of the following sequence:

a. One Target Selection Phase
b. One Command Block Transfer Phase
c. Zero or more Data Block Transfer Phase(s) (type and number determined by the preceding Command Block parameters)
d. One Status Byte Transfer Phase
e. One Message Byte Transfer Phase
f. One Bus Release Phase

During a transaction, all Data Block Transfer Phases are in the same direction and of the same size.

COMMAND BLOCKS

A transaction is initiated by the host to instruct the controller to execute a command. During the Command Block Transfer Phase, six bytes of information specifying the command are transferred to the controller. There is a specific format for these bytes, shown in figure below.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	Command Class			OP Code				
1	Logical Unit Number			Logical Sector Address (high)				
2	Logical Sector Address (Middle)							
3	Logical Sector Address (Low)							
4	Interleave or Block Count							
5	Control Byte							

Byte 0 is transferred first. Byte 0 must be specified for all commands. Each command has exactly one Byte 0 value associated with it.

Depending on the value of Byte 0, each parameter in Bytes 1 through 5 may require specification. Table specifies the supported commands and their parameters. It also includes information in data transfers required during execution. All other commands are reserved.

LOGICAL UNIT NUMBER (LUN)

This is contained in the upper three bits of Byte 1. The allowed values are 0, 1. The designators in the Command Table are:

Drive 0 (LUN 0) or 1 (LUN 1)

LOGICAL SECTOR ADDRESS (L)

This is a 21 bit field contained in Bytes 1, 2, and 3. It is computed from the Cylinder (C), Head (H), and Sector (S) address, as well as the drive parameters, heads per drive (HD) and Sectors per track (ST):

$$L = (((C * Hd) + H) * ST) + S$$

C, H and S can be derived from L, HD, and ST as follows:

$$S = L \text{ Modulo } ST$$
$$H = ((L-S)/ST) \text{ Modulo } HD$$
$$C = (((L-S)/ST) - H)/HD$$

This field specifies a sector (or a beginning sector) for the Read and Write Drive commands. It specifies a track for the Format and Seek commands (marked with a * in the table). When only a track specification is required, the sector number implied by the Logical Sector Address is ignored.

INTERLEAVE OR BLOCK COUNT

This field makes up Byte 4. The Interleave Ratio (I) is specified in the Five Format commands. The maximum ratio is the sectors-per-track minus 1.

The Block Count (B) is specified in the Read, Write, Read Long, and Write Long commands. It specifies the number of Logical Sectors to be transferred.

Both Interleave Ratio and Block Count use all 8 bits to specify the parameters.

CONTROL BYTE

This Byte is broken into the following fields:

FIELD	BIT(s)	FUNCTION
S	0-3	Used in all commands which may cause an explicit seek. Contains a code corresponding to a seek stepping algorithm. See Device Control Block (Fast Step Options).
U	4	Reserved. Unused.
P	5	Used in the format commands. If 0, fill data fields with hex 6C. If 1, fill with the pattern in the sector buffer.
A	6	Used in the Read Drive command with LUN indicating Winchester. Normally 0. If 1, do not re-read before attempting error correction.
R	7	Used in all commands which will cause an ID field to be read. Normally 0. If 1, Disable retries.

NOTE:
If one or more of the above fields are required to be specified for a command, then all the other fields in that control byte must be set to zero. If none are required, all eight bits are interpreted as "don't cares."

WD1002-SHD DEVICE CONTROL BLOCK

FAST STEP OPTIONS

The fast step option field contains an unsigned 3-bit integer. These integers correspond to the following fast step algorithms:

OPTION	
0	Default: 3 milliseconds per step
1	Half-step for Seagate & Texas Instrument drives
2	3 Msec
3	3 Msec
4	200 microseconds per step. This is appropriate for buffered steps on drives made by Computer Memories, Inc. and Rotating Memories, Inc.
5	70 microseconds per step.
6	30 microseconds per step.
7	15 microseconds per step.
8	2 milliseconds per step.
9	3 Msec
B-F	Spare (3 Msec)

COMMAND STATUS BYTE

BITS	
0	0
1	Error flag: 0 → no error 1 → error
2	0
3	0
4	0
5-7	Logical unit number

At the completion of execution of each command a command status byte is sent by the WD1002/SHD to the host to indicate to the host whether or not the command was successful.

The logical unit number returned is simply the contents of the logical unit field in the drive control block. For those commands that do not take a logical unit number as an input parameter, the logical unit number returned in the command status byte is not meaningful.

COMMAND COMPLETION BYTE

The command completion byte is an all zero byte sent by the WD1002/SHD to the host immediately following each command status byte. It indicates to the host that the WD1002/SHD has freed the SASI bus.

COMMANDS

Each command is briefly described below.

1. TEST DRIVE READY (CLASS 0, OPCODE 1)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0
1	Bits 5-7 = Logical unit number Bits 0-4	 don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, invalid command, no seek complete, drive not ready, no index pulses, write fault.

Action

Select the drive and determine whether or not it is ready.

For a Winchester drive, read its status register and test the ready bit and busy bit. For Winchester drives supporting buffered seeks this command is useful for determining the first drive to reach its target track.

2. RECALIBRATE (CLASS 0, OPCODE 1)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0
1	Bits 5-7 = Logical unit number Bits 0-4	 don't care
2		don't care
3		don't care
4		don't care
5	Control field Bit 7 Bit 6 — Immediate ECC: 0 → no immediate correction Bit 4 — Reserved for future use. Must be zero. Bit 5 — Format data. Bits 0-3	don't care 0 0 0 don't care

Possible Error Codes

No error, invalid command. Track 0 not found, drive not ready, write fault.

Action

Position the heads to cylinder 0.

3. REQUEST STATUS (CLASS 0, OPCODE 3)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 3
1	Bits 5-7 = Logical unit number Bits 0-4	 don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, invalid command.

Action

Send the host the error byte and a 3-byte logical sector address for the specified drive.

The following non-drive error codes are treated as drive 0 errors: RAM failure (30.), ROM failure (31.), ECC failure (32.). Hence, if command RAM diagnostic or command controller diagnostic detects an error, then status for drive 0 should be requested.

Error Byte

BITS	
7	Logical sector address flag: 0 → sector address not valid 1 → sector address valid
6	Not used. Set to 0.
0-5	Error codes

Logical Sector Address

BYTE	
0	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21
1	Logical sector address bits 8-15
2	Logical sector address bits 16-23

If the most recent non-request-status command to the specified drive required a logical sector address, then the logical sector address flag is 1; else, it is 0. If the logical sector address flag is 0, then the logical sector address is not meaningful.

If there was an error on the immediately preceding command and the logical sector address flag is 1, then the logical sector address indicates the sector or track on which the error occured. If the command was a format type command, then the logical sector address indicates the track; else, it indicates the sector.

If there was no error on the immediately preceding command and the command was a format type command, then the logical sector address indicates the track one beyond the last track accessed.

If there was no error and the command was not a format type command, then the logical sector address indicates the last sector accessed.

3A. ERROR CODES

Disk Drive Error Codes

0 No error
1 No index pulses
2 No seek complete
3 Write fault
4 Drive not ready
6 Track 0 not found

Controller Error Codes

10/14 Not used because WD1010 bumps CRC with several other errors in an I.D. field as errors not found.
11 Uncorrectable data error
12 Address mark not found
15 Seek error
18 Error burst corrected
19 Bad track

1A Format error
1C Illegal (direct) access to an alternate track
1D Alternate track already used
1E Alternate track not marked as alternate
1F Alternate track equals bad track

Command Error Codes

20 Invalid command
21 Invalid sector address

Miscellaneous Error Codes

30 RAM failure
31 ROM failure
32 ECC hardware failure

3B. ERROR CODE DESCRIPTIONS

No Seek Complete (2)

This error code is only returned by the test drive ready command when the target drive is a Winchester that supports buffered seeks. It indicates that drive is busy doing a buffered seek.

Write Fault (3)

Indicates that there was write current to the head when write the write gate was off. This is a very serious problem and should be fixed immediately.

Track 0 Not Found (6)

This error code is only returned by the recalibrate command. It indicates that the track 0 status from the drive did not become active after the maximum necessary steps towards cylinder 0.

Uncorrectable Data Error (11)

For a Winchester drive this error code indicates one or more error bursts in the data field were beyond the error correction code's ability to correct. The sector data for the sector in error is not sent to the host.

Address Mark Not Found (12)

Indicates that the header for the target sector was found, but its address mark was not detected.

Error Burst Corrected (18)

Indicates that the error correction code (ECC) was used to successfully correct an error. The corrected sector data is sent to the host. This is the only error condition for which sector data is sent to the host.

Bad Track (19)

This usually indicates access of a track that was formatted as a bad track. However, there is a very small chance that it indicates that a track formatted as a bad track with alternate is so faulty that none of the multiple, duplicate pointers to the alternate track can be read.

Format Error (1A)

This error code is returned by the check track format command. It indicates that the track is not formatted, the track is not formatted with the specified interleave factor, or at least one sector header is unreadable.

This error code is returned by drive diagnostic to indicate that a bad-track-with-alternate does not contain a valid pointer to the alternate track.

Alternate Track Already Used (1D)

This error code is only returned by the format alternate track command. It indicates that the specified alternate track is already an alternate or bad track.

Alternate Track Not Marked As An Alternate (1E)

This error code indicates that access of a bad-track-with-alternate caused access to an alternate track which was not marked as an alternate track.

Alternate Track Equals Bad Track (1F)

This error code is only returned by the format alternate track command. It indicates that the same track was specified as the bad track and the alternate track.

Invalid Command (20)

This error code indicates that the command class, command code, logical unit number, interleave factor, or fast step number were invalid.

ROM Failure (30)

This error code indicates one of the following conditions: (1) The program memory ROM checksum does not match the calculated checksum. (2) The RAM in the microprocessor failed. (3) The microprocessor CPU failed.

4. FORMAT DRIVE (CLASS 0, OPCODE 4)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 4
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data: 0 → hex 6C 1 → contents of sector buffer	
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, write fault.

Action

Format from the specified track to the end of the disk. The previous contents of the formatted tracks are ignored.

5. CHECK TRACK FORMAT (CLASS 0, OPCODE 5)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 5
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0

5. CHECK TRACK FORMAT (Continued)

BYTE		CONTENTS
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, seek error, format error, drive not ready, write fault.

Action

Verify that the specified track is formatted with the specified interleave factor. Do not read the sector data fields.

6. FORMAT TRACK (CLASS 0, OPCODE 6)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 6
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data: 0 → hex 6C 1 → contents of sector buffer	
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, write fault.

Action

Format the specified track. The current contents of the specified track are ignored.

7. FORMAT BAD TRACK (CLASS 0, OPCODE 7)

The WD1002-SHD writes the data fields.

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 7
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7	don't care
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, write fault.

Action

Format the specified track with a bad block mark in each sector header. The previous contents of the specified track are ignored. The contents of a bad track are not accessible.

8. READ (CLASS 0, OPCODE 8)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 8
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction 1 → immediate correction	
	Bit 5 — Format data	0

8. READ (CLASS 0, OPCODE 8) (Continued)

BYTE		CONTENTS
	Bit 4 — Reserved for future use. Must be zero. Bits 0-3 = Fast step option integer	0

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, error burst corrected, uncorrectable data error, write fault.

Action

Read the specified number of consecutive sectors beginning with the specified sector.

9. WRITE (CLASS 0, OPCODE 0A)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0A
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, write fault.

Action

Write the specified number of sectors beginning with the specified sector.

10. SEEK (CLASS 0, OPCODE 0B)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0B
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4		don't care
5	Control field	don't care
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, write fault.

Action

Move the read/write head to the specified cylinder. Do not read any sector header to verify start or end position.

11. SET PARAMETERS (CLASS 0, OPCODE 0C)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0C
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

If parameters out of range, "INVALID COMMAND."

Action

Set the following parameters for both of the Winchester drives (logical units 0 and 1): Number of cylinders, number of heads, starting reduced write current cylinder, starting write precompensation cylinder, and the maximum length of an error burst to be corrected. These parameters are sent by the host to the WD1002/SHD in a parameter block with the following format:

Parameter Block

BYTE	
0	Most significant byte of number of cylinders
1	Least significant byte of number of cylinders
2	Bits 4-7. Must be 0. Bits 0-3 = Number of heads
3	Most significant byte of starting reduced write current cylinder
4	Least significant byte of starting reduced write current cylinder
5	Most significant byte of starting write precompensation cylinder
6	Least significant byte of starting write precompensation cylinder
7	Bits 4-7. Must be 0. Bits 0-3 = Maximum length of an error burst to be corrected

Power up and reset set these parameters to the following defaults:

153. = Number of cylinders
4 = Number of heads
128. = Starting reduced write current cylinder
64. = Starting write precompensation cylinder
11. = Maximum length of an error burst to be corrected

The acceptable range of values for these parameters are as follows:

1 — 1024. Number of cylinders
1 — 8 Number of heads
0 — 1023. Starting reduced write current cylinder
0 — 1023. Starting write precompensation cylinder
1 — 11. Maximum length of error burst to be corrected.

If one of the parameters is out of range, then all parameters up to but not including the parameter in error are set for drive 0 and no parameter for drive 1 is set. The error code for this error is "invalid command."

Starting Reduced Write Current Cylinder

The specified starting reduced write current cylinder number is rounded down to the nearest integer multiple of four. That is, the actual starting reduced write current cylinder numbers are 0, 4, 8, 12, . . . 1020.

Maximum Length of Error Burst To Be Corrected

For almost all applications the maximum length of error burst to be corrected should be about 5. Correcting longer bursts greatly increases the chances of miscorrecting.

12. LAST CORRECTED BURST LENGTH (CLASS 0, OPCODE 0D)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0D
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error.

Action

Send the host one byte of data containing the length of the most recently corrected error burst. If no error burst has been corrected since the last power up or reset, then a length of zero is sent to the host.

Error Burst Length Block

BYTE	
0	Number of bits in most recently corrected error burst.

13. FORMAT ALTERNATE TRACK (CLASS 0, OPCODE 0E)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0E
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data: 0 → hex 6C 1 → contents of sector buffer	
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, alternate track already used, alternate track equals bad track, write fault.

Action

Format the specified track as a bad-track-with-alternate. Format the specified alternate track with the specified interleave factor. The alternate track is specified by the host by sending an alternate sector address block to the WD1002/SHD after the DCB.

Alternate Sector Address Block

BYTE	
0	Bits 5-7. Must be 0. Bits 0-4 = Logical sector address bits 16-21
1	Logical sector address bits 8-15
2	Logical sector address bits 0-7

14. WRITE SECTOR BUFFER (CLASS 0, OPCODE 0F)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0F
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error.

Action

Write data from the host to the WD1002/SHD sector buffer. The host must send as many bytes as there are in a sector on logical unit 0. This data is not written to any disk. This command is used to initialize the format data optionally used by the format commands.

15. READ SECTOR BUFFER (CLASS 0, OPCODE 10)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 10
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error.

Action

Send the host the current contents of the WD1002's sector buffer. The host must accept as many bytes as there are in a sector on logical unit 0.

16. RAM DIAGNOSTIC (CLASS 7, OPCODE 0)

The WD1002-SHD does not preserve the sector buffer.

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 0
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, RAM failure.

Action

Test the sector buffer by writing and reading various patterns into it.

17. DRIVE DIAGNOSTIC (CLASS 7, OPCODE 3)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 3
1	Bits 5-7 = Logical unit number Bits 0-4	don't care
2		don't care
3		don't care
4		don't care

17. DRIVE DIAGNOSTIC (Continued)

BYTE		CONTENTS
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, drive not ready, seek error, format error, write fault.

Action

Recalibrate the target drive then scan ID on each track. This command does not write to the disk. Nor does it send any sector data to the host.

The effect of drive diagnostic is to verify that at least one sector header can be read on each track. It does not report an error when it encounters a track that has been formatted as a "bad track," "bad-track-with-alternate," or "alternate track."

18. CONTROLLER DIAGNOSTIC (CLASS 7, OPCODE 4)

The WD1002-SHD does not preserve the sector buffer.

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 4
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, ROM failure, RAM failure, ECC hardware failure.

Action

Calculate a checksum for the program ROM, test the microprocessor, the sector buffer, and the ECC hardware. This command does not access any disk drive.

19. READ LONG (CLASS 7, OPCODE 5)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 5
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, write fault.

Action

Read the specified number of consecutive sectors and their ECC bytes beginning with the specified sector. There are four bytes of ECC per sector. This command is only useful for diagnostic purposes.

20. WRITE LONG (CLASS 7, OPCODE 6)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 6
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, write fault.

Action

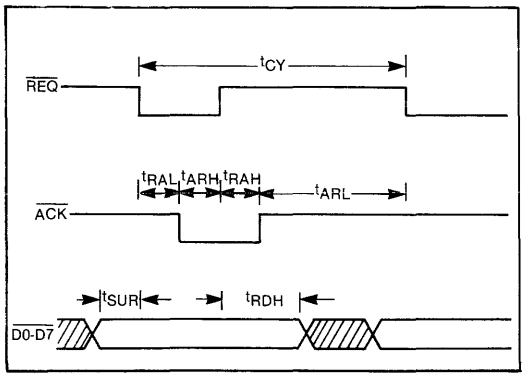
Write the specified number of consecutive sectors beginning with the specified sector. Following each sector the host sends four ECC bytes to the WD1002/SHD these are written to the disk as the ECC bytes for the sector.

This command is useful for diagnostic purposes. It allows the generation of a sector containing a correctable ECC error.

COMMAND NAME	CLASS + OP CODE	LUN	LOGICAL SECTOR ADDRESS	INTER-LEAVE OR BLOCK COUNT	CON-TROL BYTE OPTIONS	# OF SASI DATA BLOCK TRANSFERS	DATA BLOCK SIZE	DIRECTOR
Test Drive Ready	0,0	W	—	—	—	0	—	—
Restore To Track 0	0,1	W	—	—	R,S	0	—	—
Return Status	0,3	W	—	—	—	1	4	To Host
Format Drive	0,4	W	L*	I	R,P,S	0	—	—
Check Track Format	0,5	W	L*	I	R,S	0	—	—
Format Track	0,6	W	L*	I	R,P,S	0	—	—
Format Bad Track	0,7	W	L*	I	R,P,S	0	—	—
Read Drive	0,8	W	L	B	R,A,S	B	Sector	To Host
Write Drive	0,A	W	L	B	R,S	B	Sector	To CTLR
Seek	0,B	W	L*	—	R,S	0	—	—
Winchester Parameters	0,C	W	—	—	—	1	8	To CTLR
Return Burst Error Length	0,D	W	—	—	—	1	1	To Host
Format Alternate Track	0,E	W	L*	I	R,P,S	1	3	To CTLR
Write Sector Buffer	0,F	—	—	—	—	1	— Sector	To CTLR
Read Sector Buffer	0,10	—	—	—	—	1	— Sector	To Host
Perform RAM Diagnostics	7,0	—	—	—	—	0	—	—
Perform Drive Diagnostics	7,3	W	—	—	R,S	0	—	—
Perform Controller Diagnostics	7,4	—	—	—	—	0	—	—
Read Drive Long	7,5	W	L	B	R,S	B	— Sector +4	To Host
Write Drive Long	7,6	W	L	B	R,S	B	— Sector +4	To CTLR

LEGEND

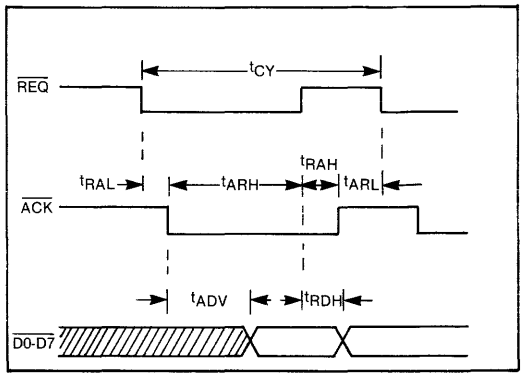
W Winchester
L* Logical sector address used only to specify track
I Interleave
B Block count
R Retry enable/disable
A Attempt immediate error correction enable/disable
S Stepping algorithm
P Used with format commands for determining data field pattern



CONTROLLER-TO-HOST TIMING

tXX	MIN*	MAX*
tCY**	1152	
tRAL†	0	
tARH	200	448
tRAH††	0	
tARL	200	848
tSUR	125	
tRDH	152	

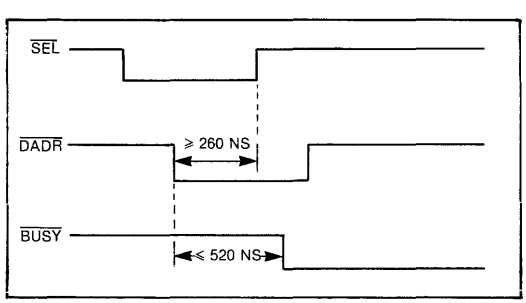
*nsec
**If conditions in † and †† are met, then tCYtYP = 1200 nsec and tCY max = 1248 nsec.
†If tRAL ⩽ 497 nsec, than no wait states are inserted.
††If tRAH⩽ 200 nsec, then no wait states are inserted.



HOST-TO-CONTROLLER TIMING

tXX	MIN*	MAX*
tCY**	1152	
tRAL†	0	
tARH	600	840
tRAH††	0	
tARL	200	448
tADV		375
tRDH	0	

*nsec
**If conditions in † and †† are met, then tCYtYP = 1200 nsec and tCY max = 1248 nsec.
†If tRAL ⩽ 89 nsec, than no wait states are inserted.
††If tRAH⩽ 97 nsec, then no wait states are inserted.



CONTROLLER SELECT TIMING

NOTE:
NO RESTRICTION ON SEQUENCE OF SEL AND DADR FALLING EDGES. BOTH MUST BE LOW TO ENSURE CONTROLLER SELECTION.

Printed in U.S.A.

PRELIMINARY

WD1002-MTB Multibus™ Winchester/Floppy Disk Controller

FEATURES

- ON-BOARD MICROPROCESSOR CONTROL
- MULTIBUS INTERFACE
- 16 BIT DATA BUS AND 24 BIT ADDRESSING
- DMA CONTROL
- SELF-TEST DIAGNOSTIC CAPABILITY
- INTERFACE COMPATIBLE WITH SEAGATE ST506/SHUGART SA450 TECHNOLOGY
- BUILT-IN DATA SEPARATOR/WRITE PRECOMP LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROLS UP TO 2 WINCHESTER DRIVES AND 8 READ/WRITE HEADS PER DRIVE
- 1024 CYLINDER/256 SECTOR PER TRACK ADDRESSING RANGE
- CRC GENERATION/VERIFICATION ON ALL ID FIELDS
- DIAGNOSTIC READS AND WRITES FOR CHECKING ECC
- AUTOMATIC FORMATTING
- 128, 256, 512, AND 1024 BYTES PER SECTOR (USER SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY (INCLUDING INTERLEAVE FACTOR ONE)
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS (ONLY IF DRIVE HAS BUFFERED SEEKS)
- PROGRAMMABLE STEP RATES FROM 7.5 mS TO 35 μS IN 500 μS INCREMENTS
- MULTIPLE SECTOR TRANSFERS (UP TO 65,535 SECTORS)
- AUTOMATIC TRACK/CYLINDER BOUNDARY CROSSING ON MULTI SECTOR TRANSFERS
- PROGRAMMABLE DISK PARAMETERS
- ECC 5 BIT CORRECTION ON ALL SECTORS, MULTIPLE BURST DETECTION TO 8 BITS
- PARALLEL ECC IMPLEMENTATION
- COMPUTER GENERATED ECC POLYNOMIAL
- ECC DISABLING CAPABILITY SUPPORTS READ/WRITE, SHORT/LONG FEATURES
- ERROR REPORTING SUPPORTS DISK AND CONTROLLER ERRORS
- SUPPORTS BAD BLOCK MAPPING
- CONTROLS UP TO FOUR 5.25″ FLOPPY DISK DRIVES
- PROGRAMMABLE DISK PARAMETERS
- SINGLE SIDED, SINGLE DENSITY; DOUBLE SIDED, SINGLE OR DOUBLE DENSITY SUPPORTED
- INTEGRAL PLL DATA SEPARATOR
- SOFT SECTOR FORMAT COMPATIBILITY

DESCRIPTION

The WD1002-MTB is a custom single board disk controller, specifically designed to interface to Multibus. The WD1002-MTB conforms to all conditions set forth in the IEEE 796 Bus Standard. The purpose of the board is to provide disk control for up to two 5.25″ Winchester disk drives and up to four 5.25″ Floppy disk drives. All necessary buffers and driver/receivers are included on the board to allow direct connection to the various drives. Power is derived from a single +5VDC supply.

Communications between the host CPU and the WD1002-MTB, as well as all data transfers, are accomplished through DMA transfers. A uniquely defined system of I/O parameter blocks (IOPB) is utilized to establish command structures. One exception to DMA communication exists; e.g. the initial controller "Wake-Up" when the host CPU must pass the vector address of the IOPB to the WD1002-MTB via a specialized vector-stack port, located on the WD1002-MTB.

ARCHITECTURE

The WD1002-MTB architecture is illustrated in Figure 1. The WD1002-MTB board has seven on- board connectors including a test connector (J5) for initial test and alignment procedures. The remaining six connectors consist of two Multibus interface connectors (P1 and P2), one Winchester drive control connector (J1), two Winchester drive data connectors (J3 and J4), and a Floppy disk control connector (J2).

Additional capabilities include interleave factor one capability on hard disk media and extensive use of Western Digital proprietary logic devices. These include the WD1010 Winchester Controller, WD2797 Floppy Controller, WD1100-13 ECC Logic Support Device, WD1802 Octal Comparator, WD1100-10 Write Precomp/Data Separator Logic Support Device, and the DMA Controller.

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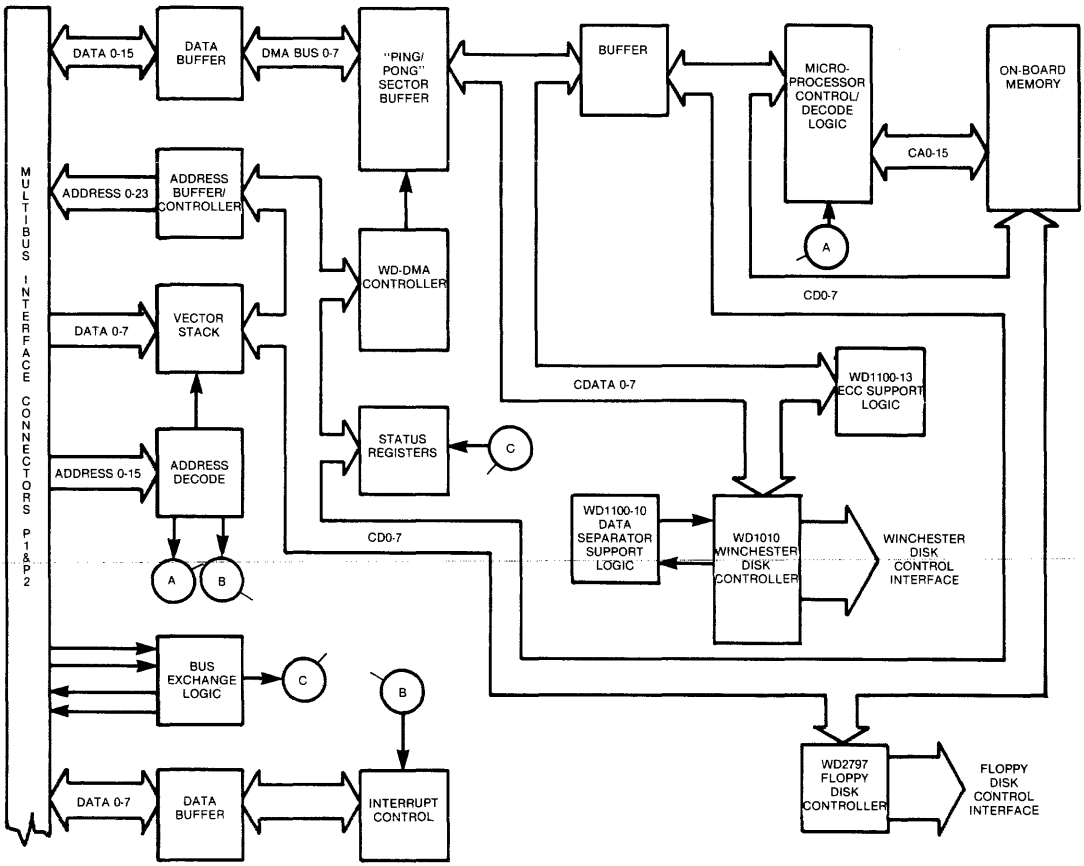


Figure 1. WD1002-MTB SIMPLIFIED BLOCK DIAGRAM

"PING PONG" SECTOR BUFFER ARCHITECTURE

The "ping/pong" buffer consists of dual RAM and counter combinations in two identical halves. All of the buffer controls are multiplexed through a single PAL (U23) for the purpose of properly switching buffers between DMA and microprocessor busses.

It is the unique architecture of these buffers which allows the controller to perform data transfers with 1:1 disk interleaving. It allows data to be written or read simultaneously to both host and controller simply by switching buffers back and forth as they become full and empty.

As can be seen in the preceding illustration, the controller bus and DMA are at opposite sides of the ping/pong. The buffers (tri-state devices) are switched in such a way that the entire ping/pong circuit looks like a single RAM buffer to either the controller or DMA.

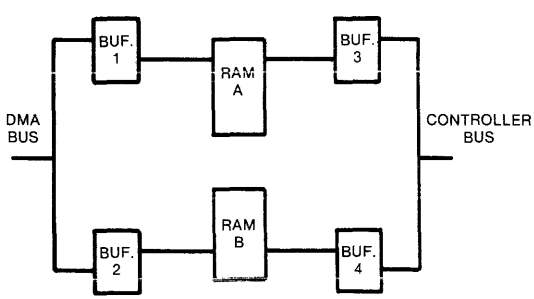


Figure 2. PING/PONG ARCHITECTURE

Example: Buffers 1 & 4 are switched simultaneously 'on' and 'off' and likewise 2 & 3 in opposition to 1 & 4. Neither bus is allowed access to the RAM at the same time. Data starts into one RAM, is switched via the buffers to the opposite bus, and taken in or out there, while more data is being transferred to the second buffer. As the two RAMs become empty and full respectively, they are switched back again for continued operation. All control of the "Ping/Pong" buffer is handled by the on-board Microprocessor while data is transferred by the respective disk controllers (WD1010, WD2797) and DMA. The "Ping/Pong" buffer control 'PAL' contains the following logical equations:

"PING PONG" SECTOR BUFFER OPERATIONAL EQUATIONS

SIGNAL	EQUATION
ARD	$\overline{WCS} * \overline{CCRD} * \overline{SELA} * ACTRO + \overline{DMASTB} * \overline{DMAWR} * SELA$
BRD	$\overline{WCS} * \overline{CCRD} * SELA * \overline{BCTRO} + \overline{DMASTB} * \overline{DMAWR} * \overline{SELA}$
AWR	$\overline{WCS} * \overline{CCWR} * \overline{SELA} * ACTRP\ \overline{DMASTB} * \overline{DMAWR} * SELA$
BWR	$\overline{WCS} * \overline{CCWR} * SELA * \overline{BCTRO} + \overline{DMASTB} * DMAWR * \overline{SELA}$
ADEC	$\overline{AWR} + \overline{WCS} * \overline{CCRD} * \overline{SELA} * ACTRO + \overline{DMASTB} * \overline{DMAWR} * SELA$
BDEC	$\overline{BWR} + \overline{WCS} * \overline{CCRD} * SELA * BCTRO + \overline{DMASTB} * \overline{DMAWR} * \overline{SELA}$
IBUFRDY	$ACTRO * \overline{SELA} + BCTRO * SELA$
SMBRDY	$ABSY * SELA + BBSY * \overline{SELA}$

SPECIFICATIONS

TEMPERATURE:

Operating Range . . . . . 5 to 65°C*
Storage Range . . . . . – 10 to + 50°C
Transit . . – 40 to + 60 maximum gradient @ 20°C/hr.

*The 65°C includes a maximum 20°C rise in the internal unit.

RELATIVE HUMIDITY:

Operating Range . . . . . 5% to 90%*
Storage Range . . . . . 10% to 90%*

*The range of relative humidity is predicated on the basis of 0% condensation.

ALTITUDE:

Operating Range . . . . . up to 9850 ft. (3000 meters)

POWER:

+ 5VDC + / – 5%, 3.5 amps typical (4.5 amps max)

DRIVE CONTROL SPECIFICATIONS

	WINCHESTER	FLOPPY
Encoding method	MFM	MFM
Cylinders/head	1024	—
Sectors/track	up to 256	17
Drive selects	2	4 (dual head)
Heads	8	—
Step rate	7.5ms to 35μs (500μs incr.)	programmable
Data transfer rate	5 Mbytes/sec	—
Write precomp time	12 ns	—
Drive capability	10 LS loads	—
Head load time	—	programmable
Intersector gap size	—	54 bytes
Motor-off delay time	—	programmable
Sectoring	soft	soft
Cable length (drive)	10 ft(3 m) max.	10 ft(3 m) max.

HOST INTERFACE

The WD1002-MTB is designed specifically as a Multibus compatible peripheral. Interfacing is accomplished in accordance with the IEEE P796 Bus Interface Standard and by the inclusion of an I/O parameter block scheme for command structure. The most direct approach to understanding the interface is to follow a simple interface scenario, which should serve as an overview only.

The host computer writes the address of an IOPB to the WD-1002-MTB. This address is written in 3 bytes, the first two of which are written to the base address of the board and the third, which is written to the base address +1. This third "WRITE" produces a 'wake-up' interrupt to the on-board processor which in turn reads the vector stack port where the address was stored (basically, a FIFO operation). This is the only instance in which communications will take place outside of DMA control.

The on-board processor now arbitrates for the bus, via Multibus convention and, once received, becomes the bus master. The controller now transfers, via DMA, the IOPB pointed to by the vector address and responds to the commands contained therein.

Once an operation has been completed by the controller a completion status is passed back to the host in the IOPB format, as well as any other pertinent information with respect to a given command. Also, upon completion of such commanded transfer, the controller will relinquish this bus for a period of about 500ns for the purpose of allowing other bus masters reasonable access. Burst length is programmable.

In addition, the controller contains an on-board interrupt controller which is entirely the host computer responsibility. That is, the controller has no communication lines with this chip at all, other than to issue it an interrupt. All initialization, set-up, and servicing of this chip must be handled by the host.

An interrupt will be issued by the controller at the completion of all commands or an aborted sequence, provided the interrupt controller is appropriately initialized.

This port is provided for the covenience of interrupt driven systems. If the host is a non-interrupt driven system, an alternative interface can be accomplished by polling the interrupt line or polling the completion code in the host memory.

MULTIBUS INTERFACE CONNECTORS

The Multibus interface connectors (P1 and P2) are card edge connectors compatible with IEEE Microcomputer Bus Standard (P796). Table 1 provides the pin descriptions for P1 and Table 2 provides the pin descriptions for P2.

Table 1. MULTIBUS INTERFACE CONNECTOR P1 PIN DESCRIPTIONS

COMPONENT SIDE				CIRCUIT SIDE		
FUNCTION	**PIN**	**SIGNAL**	**DESCRIPTION**	**PIN**	**SIGNAL**	**DESCRIPTION**
Power Supplies	1	GND	Signal Ground	2	GND	Signal Ground
	3	+5V	+5VDC	4	+5V	+5VDC
	5	+5V	+5VDC	6	+5V	+5VDC
	7		Spare	8		Spare
	9		Spare	10		Spare
	11	GND	Signal Ground	12	GND	Signal Ground
Bus Controls	13	$\overline{\text{BCLK}}$	Bus Clock	14	$\overline{\text{INIT}}$	Initialization
	15	$\overline{\text{BPRN}}$	Bus Priority In	16	$\overline{\text{BPRO}}$	Bus Priority Out
	17	$\overline{\text{BUSY}}$	Bus Busy	18	$\overline{\text{BREQ}}$	Bus Request
	19	$\overline{\text{MRDC}}$	Mem Read Command	20	$\overline{\text{MWTC}}$	Mem Write Command
	21	$\overline{\text{IORC}}$	I/O Read Command	22	$\overline{\text{IOWC}}$	I/O Write Command
	23	$\overline{\text{XACK}}$	Transfer Acknowledge	24		Spare
	25		Spare	26		Spare
Bus Controls and Address	27	$\overline{\text{BHEN}}$	Byte Hi Enable	28	$\overline{\text{AD10}}$	Address Bus
	29	$\overline{\text{CBRQ}}$	Common Bus Request	30	$\overline{\text{AD11}}$	
	31	$\overline{\text{CCLK}}$	Constant Clock	32	$\overline{\text{AD12}}$	
	33	$\overline{\text{INTA}}$	Interrupt Acknowledge	34	$\overline{\text{AD13}}$	
Interrupts	35	$\overline{\text{INT6}}$	Parallel Interrupt Requests	36	$\overline{\text{INT7}}$	Parallel Interrupt Requests

Table 1. MULTIBUS INTERFACE CONNECTOR P1 PIN DESCRIPTIONS (Continued)

COMPONENT SIDE				CIRCUIT SIDE		
FUNCTION	PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
	37	$\overline{INT4}$		38	$\overline{INT5}$	
	39	$\overline{INT2}$		40	$\overline{INT3}$	
	41	$\overline{INT0}$		42	$\overline{INT1}$	
Address	43	$\overline{ADRE}$	Address Bus	44	$\overline{ADRF}$	Address Bus
	45	$\overline{ADRC}$		46	$\overline{ADRD}$	
	47	$\overline{ADRA}$		48	$\overline{ADRB}$	
	49	$\overline{ADR8}$		50	$\overline{ADR9}$	
	51	$\overline{ADR6}$		52	$\overline{ADR7}$	
	53	$\overline{ADR4}$		54	$\overline{ADR5}$	
	55	$\overline{ADR2}$		56	$\overline{ADR3}$	
	57	$\overline{ADR0}$		58	$\overline{ADR1}$	
Data	59	$\overline{DATE}$	Data Bus	60	$\overline{DATF}$	Data Bus
	61	$\overline{DATC}$		62	$\overline{DATD}$	
	63	$\overline{DATA}$		64	$\overline{DATB}$	
	65	$\overline{DAT8}$		66	$\overline{DAT9}$	
	67	$\overline{DAT6}$		68	$\overline{DAT7}$	
	69	$\overline{DAT4}$		70	$\overline{DAT5}$	
	71	$\overline{DAT2}$		72	$\overline{DAT3}$	
	73	$\overline{DAT0}$		74	$\overline{DAT1}$	
	75	GND	Signal Ground	76	GND	Signal Ground
	77		Spare	78		Spare
	79		Spare	80		Spare
	81		Spare	82		Spare
	83		Spare	84		Spare
	85	GND	Signal Ground	86	GND	Signal Ground

Table 2. MULTIBUS INTERFACE CONNECTOR P2 PIN DESCRIPTIONS

COMPONENT SIDE				CIRCUIT SIDE		
FUNCTION	PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
	1-53 (odd)		Spare	2-54 (even)		Spare
Address	55	$\overline{ADR16}$	Address Bus	56	$\overline{ADR17}$	Address Bus
	57	$\overline{ADR14}$		58	$\overline{ADR15}$	
	59		Spare	60		Spare

WINCHESTER DRIVE CONNECTORS

Winchester Drive Control and Data Connectors

The Winchester drive control connector (J1) is daisy-chained to each of the two Winchester disk drives supported by the WD1002-MTB. The Winchester drive data connectors (J3 and J4) carry differential signals and are radially connected to the Winchester drives. The Winchester drive control requires the last drive to contain termination resisters. Table 3 provides the pin descriptions for Winchester Drive Control connector J1 and Table 4 provides the pin descriptions for Winchester Drive Data connectors J3 and J4.

Table 3. WD1002-MTB WINCHESTER DRIVE CONTROL CONNECTOR J1 PIN DESCRIPTIONS

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL	DESCRIPTION
1	2	O	$\overline{RWC}$	Reduce Write Current
3	4	O	$\overline{HS2}$	Head Select 2
5	6	O	$\overline{WG}$	Write Gate
7	8	I	$\overline{SEEK}$	Seek
9	10	I	$\overline{TR000}$	Track 000
11	12	I	$\overline{WF}$	Write Fault
13	14	O	$\overline{HS0}$	Head Select 0
15	16	—	$\overline{NC}$	No Connection
17	18	O	$\overline{HS1}$	Head Select 1
19	20	I	$\overline{IND}$	Index
21	22	I	$\overline{RDY}$	Ready
23	24	O	$\overline{STEP}$	Step
25	26	O	$\overline{DS1}$	Drive Select 1
27	28	O	$\overline{DS2}$	Drive Select 2
29	30	O	$\overline{DS3}$	Drive Select 3
31	32	O	$\overline{DS4}$	Drive Select 4
33	34	O	$\overline{DIRIN}$	Direction In

Table 4. WD1002-MTB WINCHESTER DRIVE DATA CONNECTORS J3 AND J4 PIN DESCRIPTIONS

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL	DESCRIPTION
2	1	I	$\overline{DS}$	Drive Select
4	3	—	NC	No Connection
6	5	—	NC	No Connection
8	7	—	NC	No Connection
—	9	—	NC	No Connection
—	10	—	NC	No Connection
11	—	—	GND	Ground
12	—	—	GND	Ground
—	13	O	+ MFMWD	+ MFM Write Data
—	14	O	– MFMWD	– MFM Write Data
15	—	—	GND	Ground
16	—	—	GND	Ground
—	17	I	+ MFMRD	+ MFM Read Data
—	18	I	– MFMRD	– MFM Read Data
19	—	—	GND	Ground
20	—	—	GND	Ground

WINCHESTER DRIVE CONTROL SIGNAL DESCRIPTIONS

$\overline{\text{Reduce Write Current}}$

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

$\overline{\text{Write Gate}}$

This output signal allows data to be written on the disk.

Seek Complete

Informs the WD1002-MTB that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

Track 000

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

Write Fault

Informs the WD1002-MTB that some fault has occurred on the selected drive. The WD1002-MTB will not execute commands when this signal is true.

HS0-HS2

Head Select lines are used by the WD1002-MTB to select a specific R/W head on the selected drive.

Index

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

Ready

Informs the WD1002-MTB that the desired drive is selected and that its motor is up to speed. The WD1002-MTB will not execute commands unless this line is true.

Step

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION IN line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

Direction In

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

DS1-DS4

These four Drive Select lines are used to select the desired drive.

Floppy Drive Control Connector

All commands and data to the Floppy drives are transferred via the Floppy drive control connector (J2) which is daisy-chained to the Floppy drives supported by the WD1002-MTB (up to four). The last Floppy drive in the chain also requires termination resisters. Table 5 provides the pin descriptions for Floppy drive control connector J2.

Table 5. FLOPPY DRIVE CONTROL CONNECTOR J2 PIN DESCRIPTION

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL	DESCRIPTION
1	2	—		Spare
3	4	O	$\overline{\text{READY}}$	In Use
5	6	O	$\overline{\text{DS4}}$	Drive Select 4
7	8	I	$\overline{\text{I/S}}$	Index/Sector
9	10	O	$\overline{\text{DS1}}$	Drive Select 1
11	12	O	$\overline{\text{DS2}}$	Drive Select 2
13	14	O	$\overline{\text{DS3}}$	Drive Select 3
15	16	O	$\overline{\text{MO}}$	Motor On
17	18	O	$\overline{\text{DIRC}}$	Direction
19	20	O	$\overline{\text{STEP}}$	Step
21	22	O	$\overline{\text{WD}}$	Write Data
23	24	O	$\overline{\text{WG}}$	Write Gate
25	26	I	$\overline{\text{TR00}}$	Track 00
27	28	I	$\overline{\text{WPRT}}$	Write Protect
29	30	I	$\overline{\text{RD}}$	Read Data
31	32	O	$\overline{\text{SS}}$	Side Select
33	34	—		Spare

HOST COMPUTER OPERATION

The WD1002-MTB provides the host computer a signal interface to both the floppy and Winchester disks. It does not buffer commands. The host gives the controller a single command and then waits until the controller interrupts the host to signal operation complete.

The WD1002-MTB deals only with physical drives. If the host wishes to treat one physical drive as several logical devices, then the host must keep track of these correspondences and must specify to the controller the appropriate physical drive and physical block(s) for each operation.

The host constructs an INPUT/OUTPUT Parameter Block (IOPB) to specify the desired operation and passes the address of that IOPB to the controller, via the vector address stack.

The host then waits for an interrupt from the controller. Until this interrupt occurs, the IOPB belongs to the controller and none of its contents are valid. When the interrupt occurs, the host checks the completion code returned in the IOPB to determine the success or failure of the operation.

IOPB OUTLINE

BYTES	DESCRIPTION
0	Command code (WD1002-MTB input parameter)
1	Completion code (WD1002-MTB output parameter)
2	Subdevice number (WD1002-MTB input parameter)
3	Not used
4,5,6,7	Block address (WD1002-MTB input parameter)
8,9,10,11	Memory address (WD1002-MTB input parameter)
12,13	Block count (WD1002-MTB input parameter)
14,15	Reserved for future use

As shown above, the Input/Output Parameter Block (IOPB) contains 16 bytes. For the convenience of the host computer each 2-byte field is aligned on a word boundary and each 4-byte field is aligned on a lone word boundary within the IOPB. The significance ordering of the bytes in each multi-byte field is selectable by two jumpers on the WD1002-MTB board (E44 to E43) and (E50 to E51). For 68000 operation [most significant byte (MSB) in least significant address (LSA)] E44,43 is left in tact and no jumper is required on E50,51. For Intel operation the E43,44 etch must be cut and a jumper placed on E50,51. All IOPB transfers are performed in the byte made only and therefore only the byte ordering as outlined is significant. The IOPB vector stack address must be received with the least significant byte first.

COMMANDS

0 = No action
1 = Sense Status
2 = Restore
3 = Seek
4 = Read Blocks
5 = Write Blocks
6 = Read Diagnostic
7 = Write Diagnostic
8 = Write Deleted Block
9 = Set Device Parameter
10 = Set Control Parameter
11 = Self-Test
12 = Format Blocks
13 = Reset
14 = Read bad block table
15 = Write bad block table
16 = Read device parameter
17 = Read control parameter

COMPLETION CODES

0 = No error
1 = Controller error
2 = Parameter error
3 = Aborted command
4 = Bad block
5 = Not used
6 = Block not found
7 = CRC error
8 = Write protect
9 = Write fault
A = Time-out
B = Host cancel
C = Multibus error
D = Data address mark not found
E = Track zero not found
F = Possible flex media change notification

The following commands return completion codes: no action, restore, seek, read blocks, write blocks, read diagnostic, write diagnostic, write deleted block, set device parameter, set control parameter, format blocks, reset, read bad block table, and write bad block table.

The following commands do not return completion codes: sense status and self-test.

A completion code is returned only if it is applicable and if no higher priority completion code is applicable. The completion codes in order from lowest to highest priority are: No error, Parameter error, Block not found, CRC error, Bad block, Aborted command, Write protect, Write fault, Time-out, Controller error, Multibus error and Host cancel.

NOTE:
Bit seven of the completion code is reserved as the controller busy bit for systems operating in a polled rather than an interrupt environment. An 80 hex should be written into the completion code byte prior to initiating an operation. The controller will then clear the bit at the end of command execution.

At the end of a command execution two bytes are transferred back to the host. The first byte is the command code and the second byte is the completion code.

Command Code

The command code specifies the operation to be performed by the WD1002-MTB. The command code is a WD1002-MTB input parameter.

Completion Code

The completion code indicates the success or reason for failure of a command. Completion code zero indicates successful completion of the command. A non-zero completion code indicates an error. The completion code is a WD1002-MTB output parameter.

All commands except sense status and self-test return a completion code. Sense status returns a status code and self-test returns a test result code. For both of these parameters the value zero indicates no error just as it does for the completion code. However, a non-zero status code or test result code does not mean what the same value completion code means.

Subdevice Number

The subdevice number specifies the operation's target disk drive. Subdevice numbers 0 and 1 specify Winchester drives 0 and 1, and the subdevice numbers 4 to 7 specify floppy drives 0 to 3. The subdevice number is a WD1002-MTB input parameter.

Block Address

For all operations except seek, the block address specifies the first block to be accessed. For a seek operation the block address specifies the target cylinder. The block address is a WD1002-MTB input parameter.

The block address is calculated from the block number, head number, and cylinder number using the formula:

BLOCK ADDRESS = Block number + (head number * blocks per track) + (cylinder number * number of heads * blocks per track).

Note that the blocks are numbered 0, 1, 2, 3, . . . up to the number of blocks per track minus one. The standard floppy formats all number blocks 1, 2, 3, . . . Consequently, the WD1002-MTB adds one to the block number to obtain the block number that is actually in the block header on the disk.

Memory Address

The memory address is a one-byte offset from the Multibus memory base address. That is, it is a "Multibus memory address." It is the Least Significant Address (LSA) in a buffer. A read operation transfers data from disk to Multibus memory beginning at this address. A write operation transfers data from Multibus memory beginning at this address to disk. Format uses the interleave table beginning at this address in Multibus memory. The memory address is a WD1002-MTB input parameter.

Block Count

The block count specifies the number of blocks to be transferred. It is a WD1002-MTB input parameter.

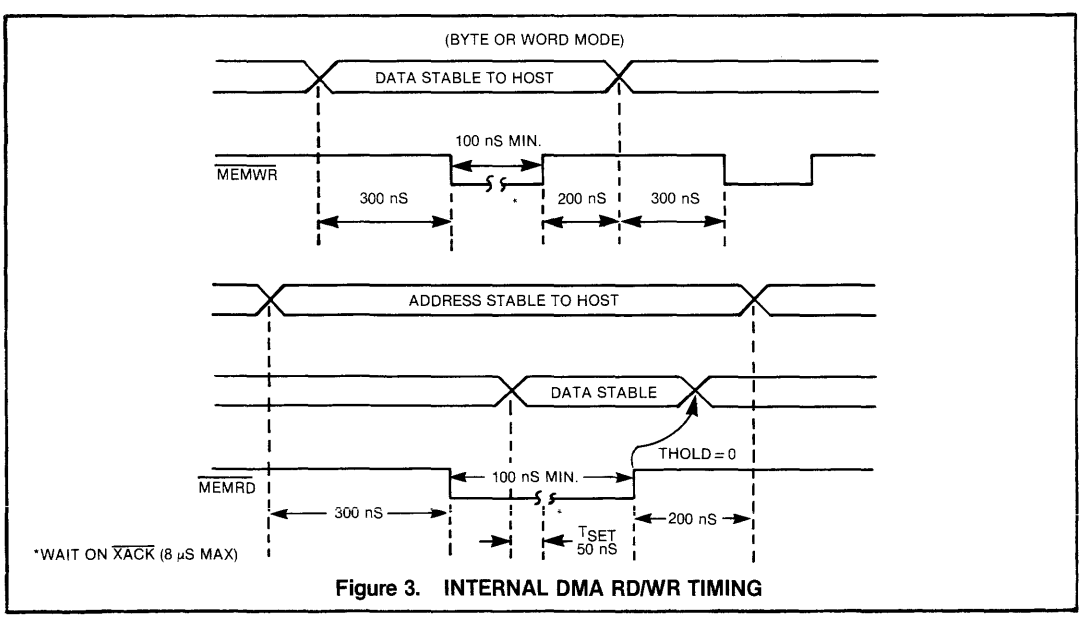


Figure 3. INTERNAL DMA RD/WR TIMING

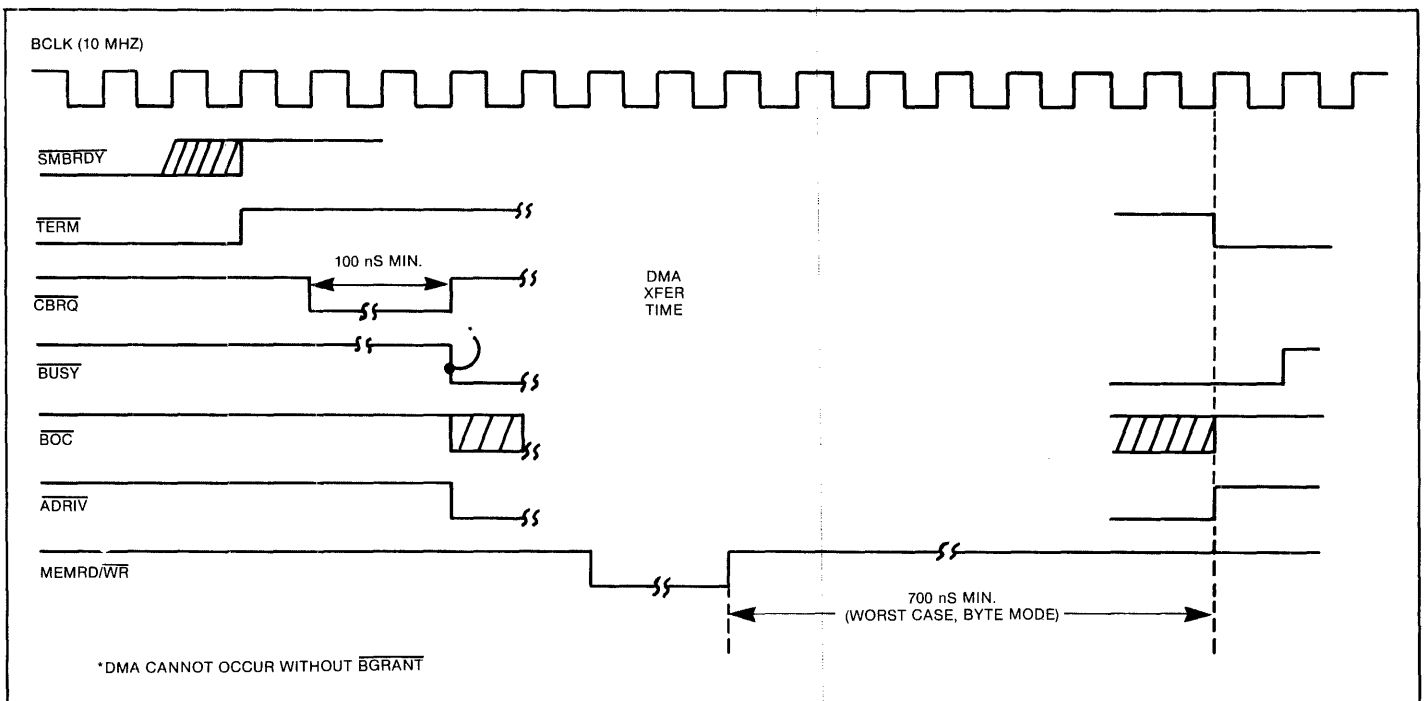


Figure 4. DMA/MULTIBUS TIMING

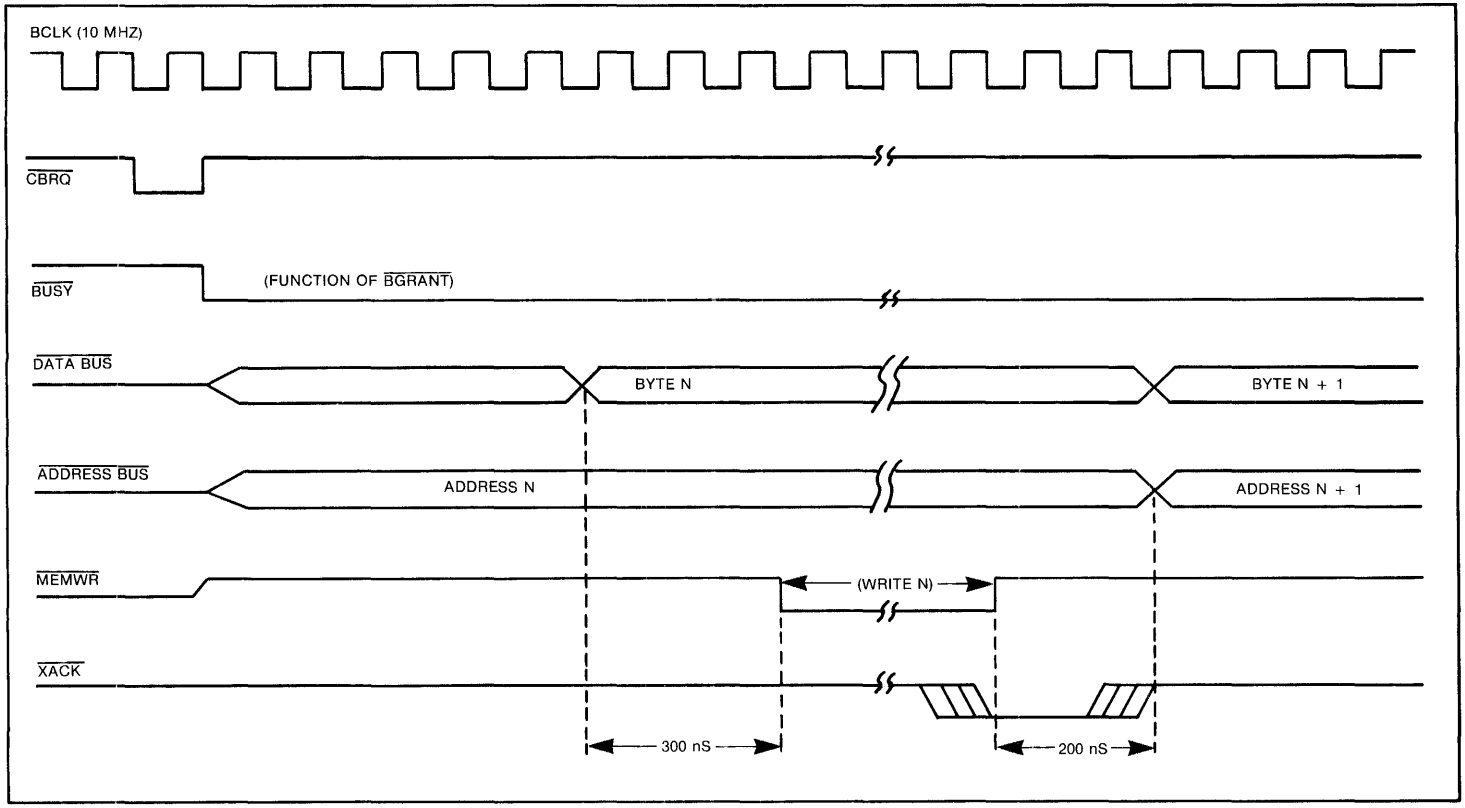


Figure 5. FIRST DMA WRITE TO HOST TIMING

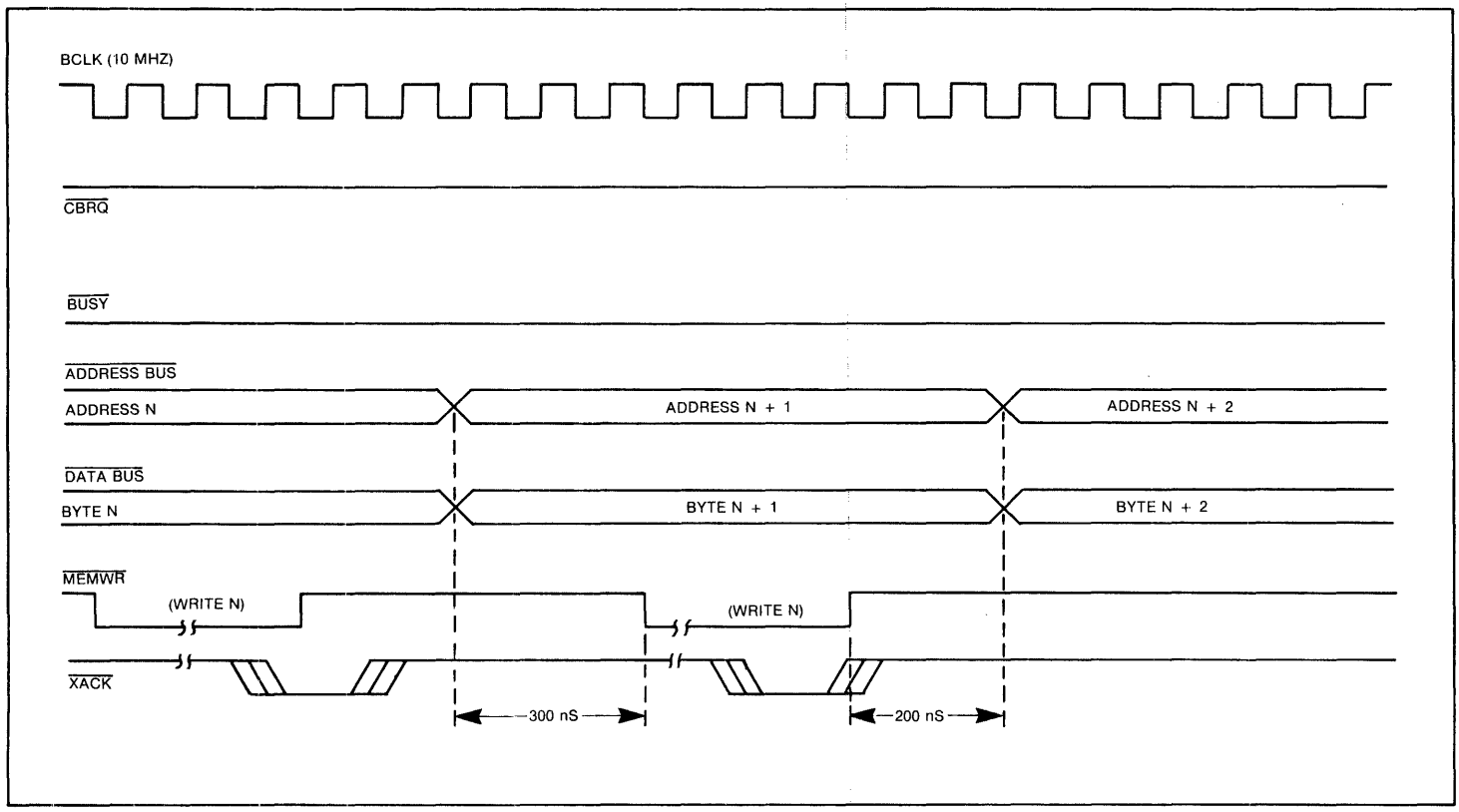


Figure 6. INTERIM WRITE DMA TO HOST TIMING

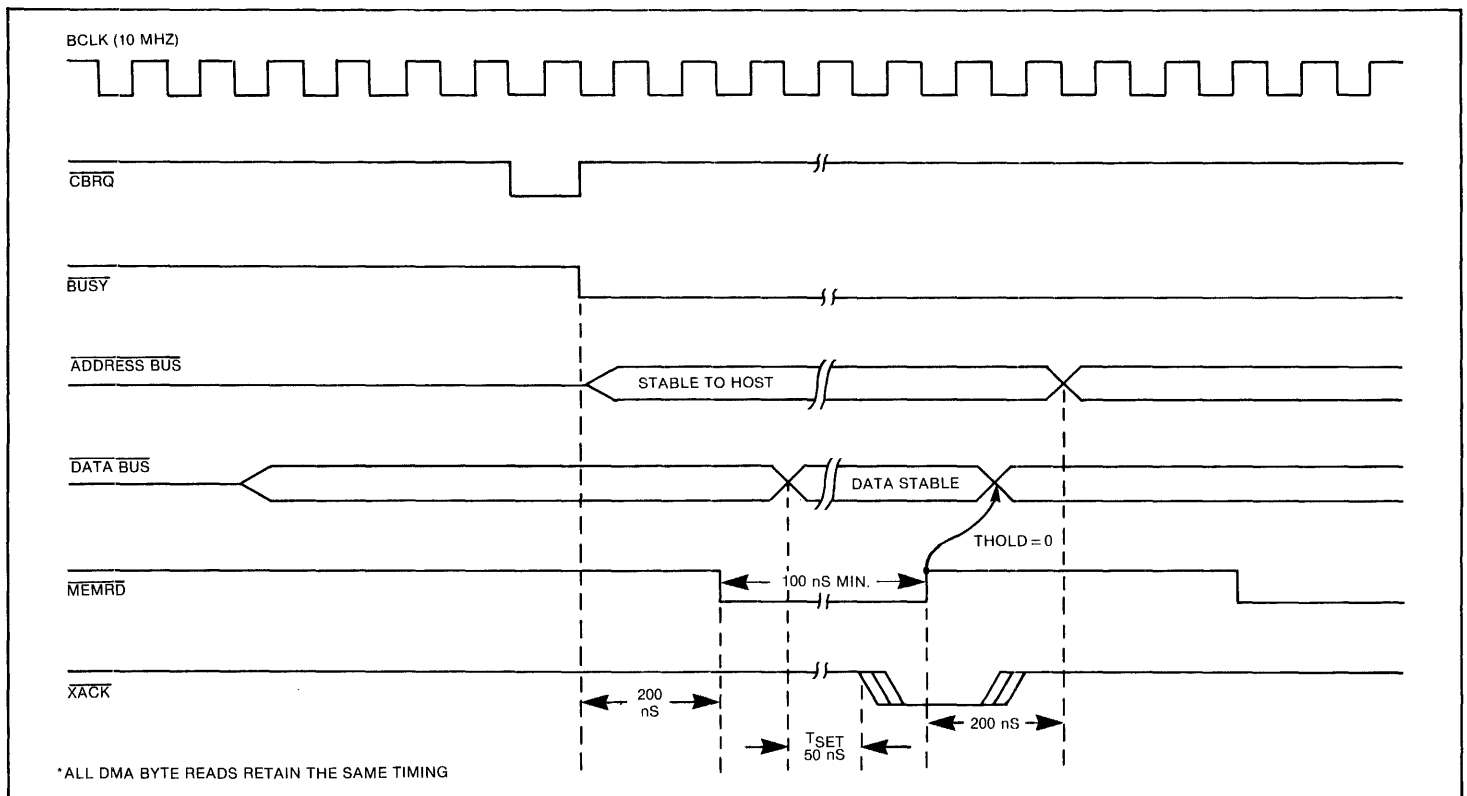


Figure 7. DMA BYTE READ (FROM HOST) TIMING

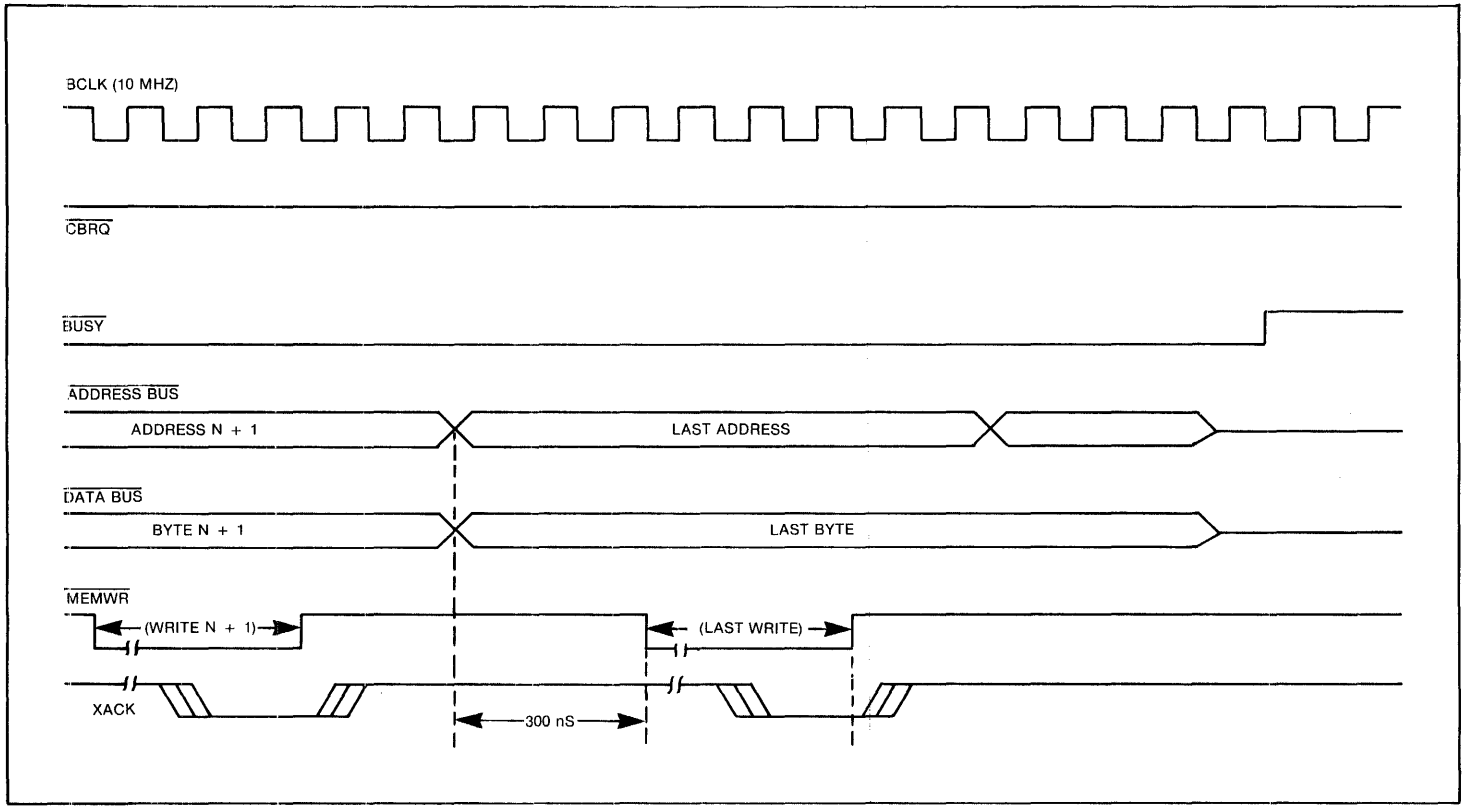


Figure 8. LAST DMA BYTE WRITE TO HOST

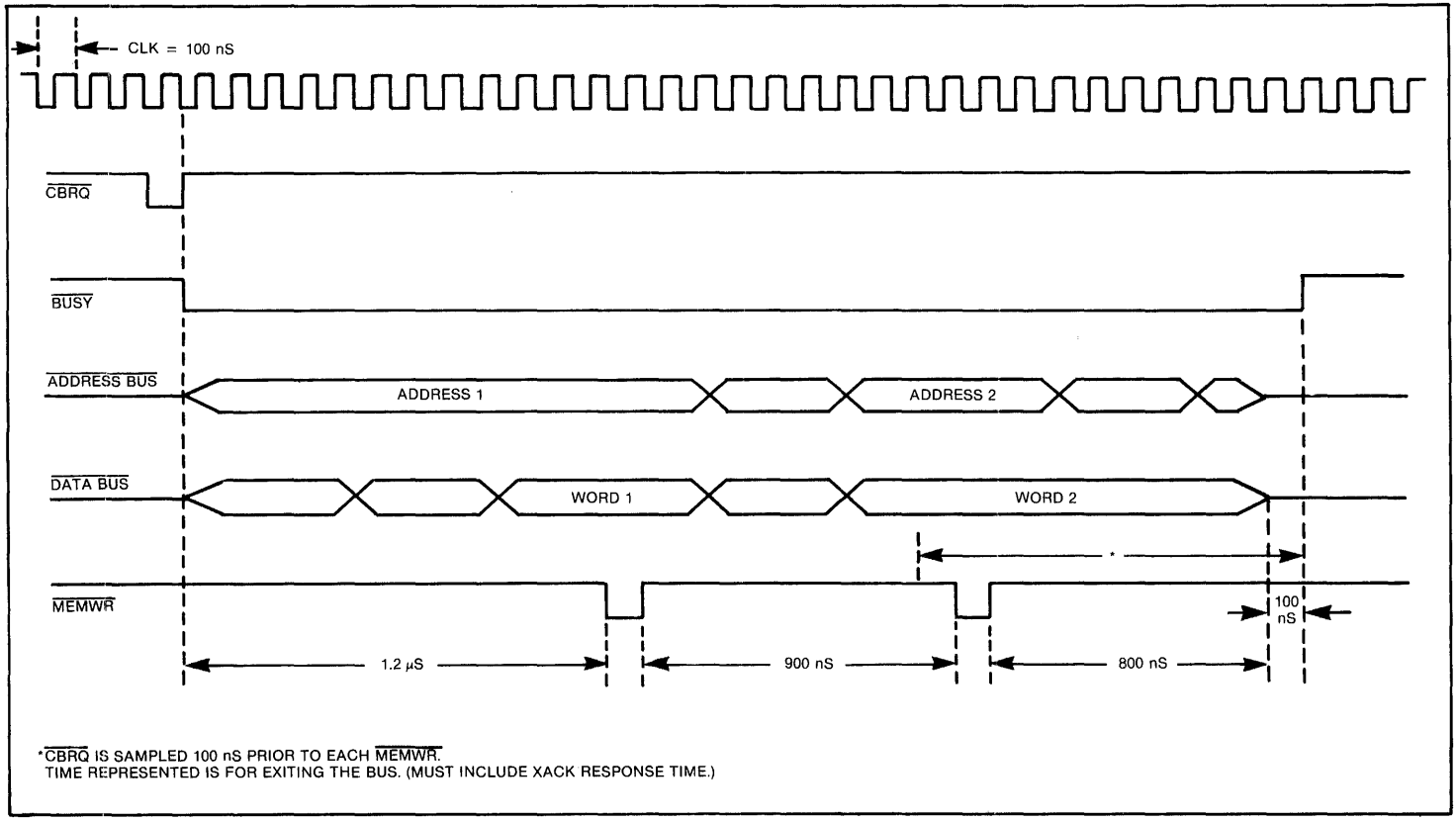


Figure 9. TYPICAL 2-WORD DATA TRANSFER TO HOST

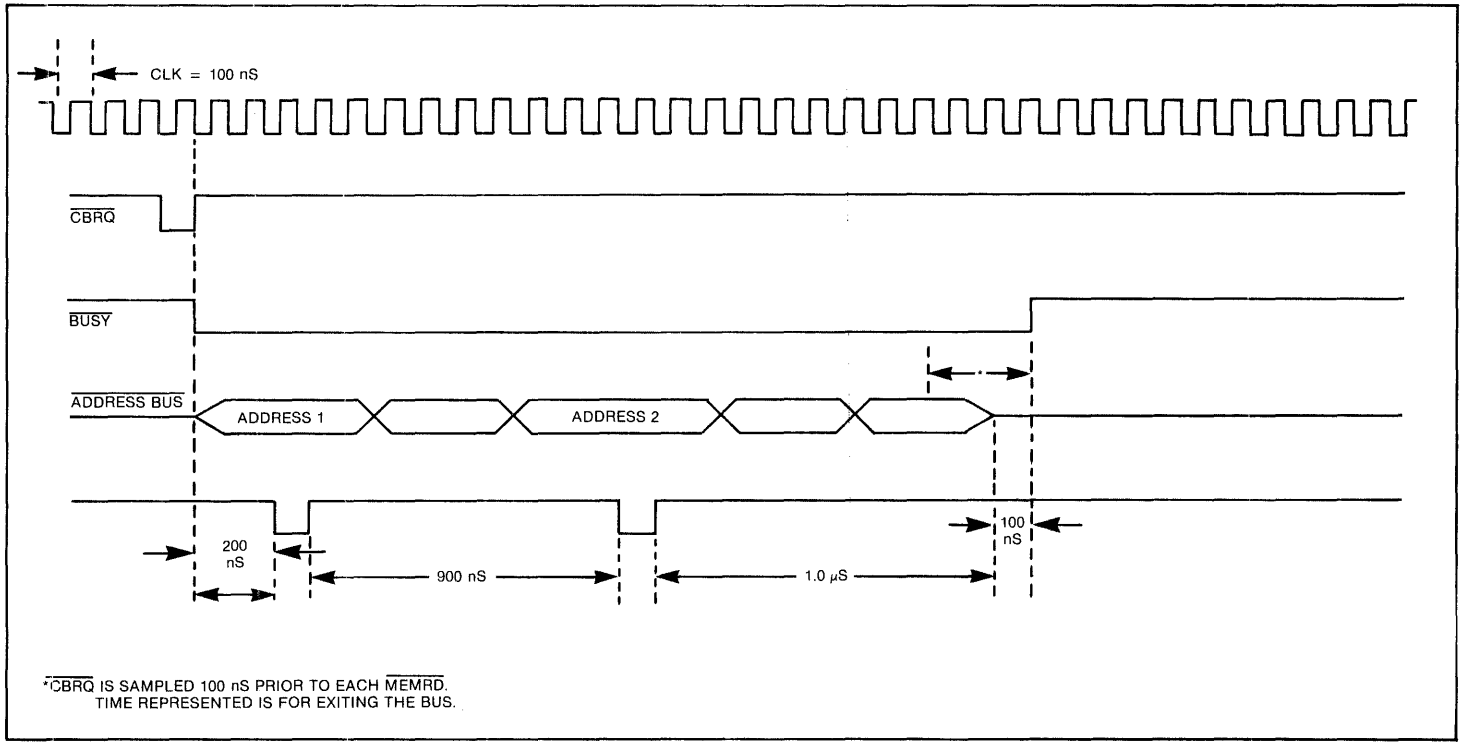


Figure 10. TYPICAL 2-WORD DATA TRANSFER FROM HOST

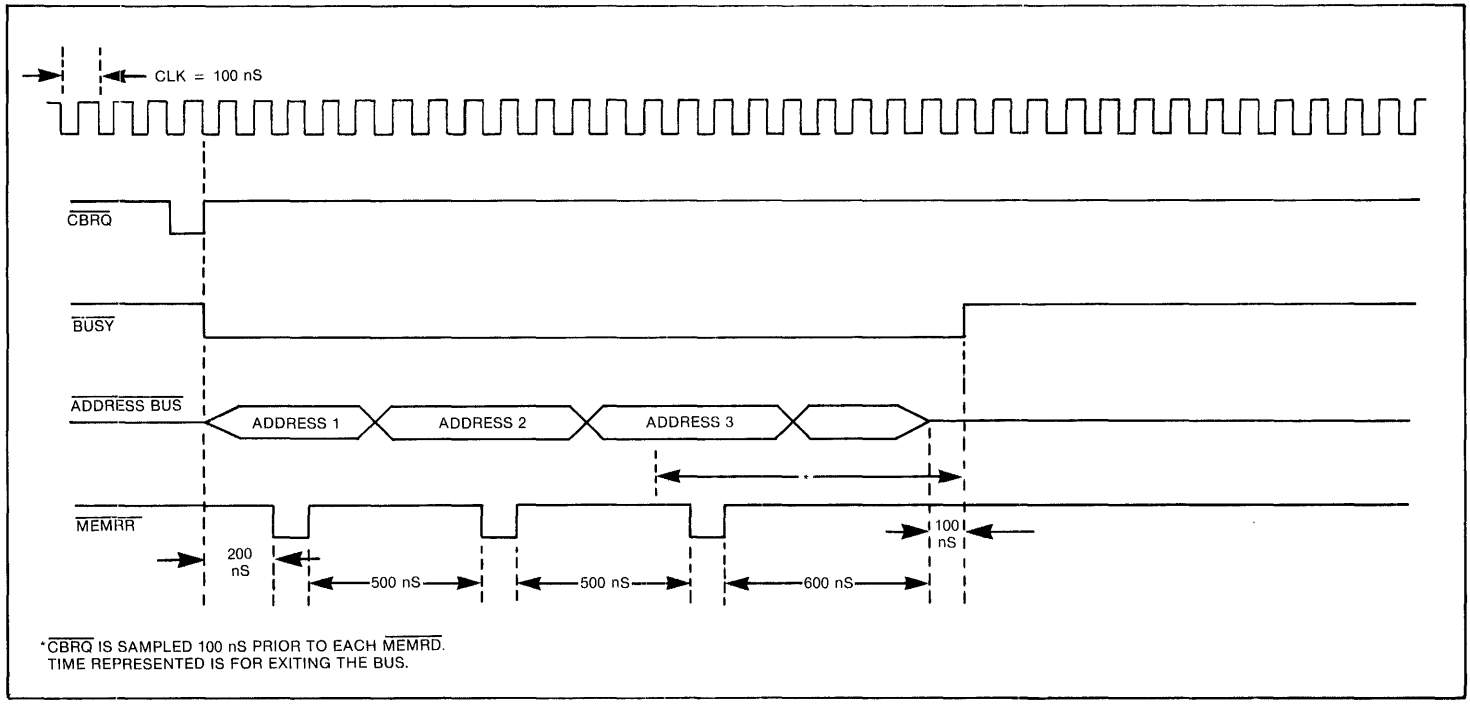
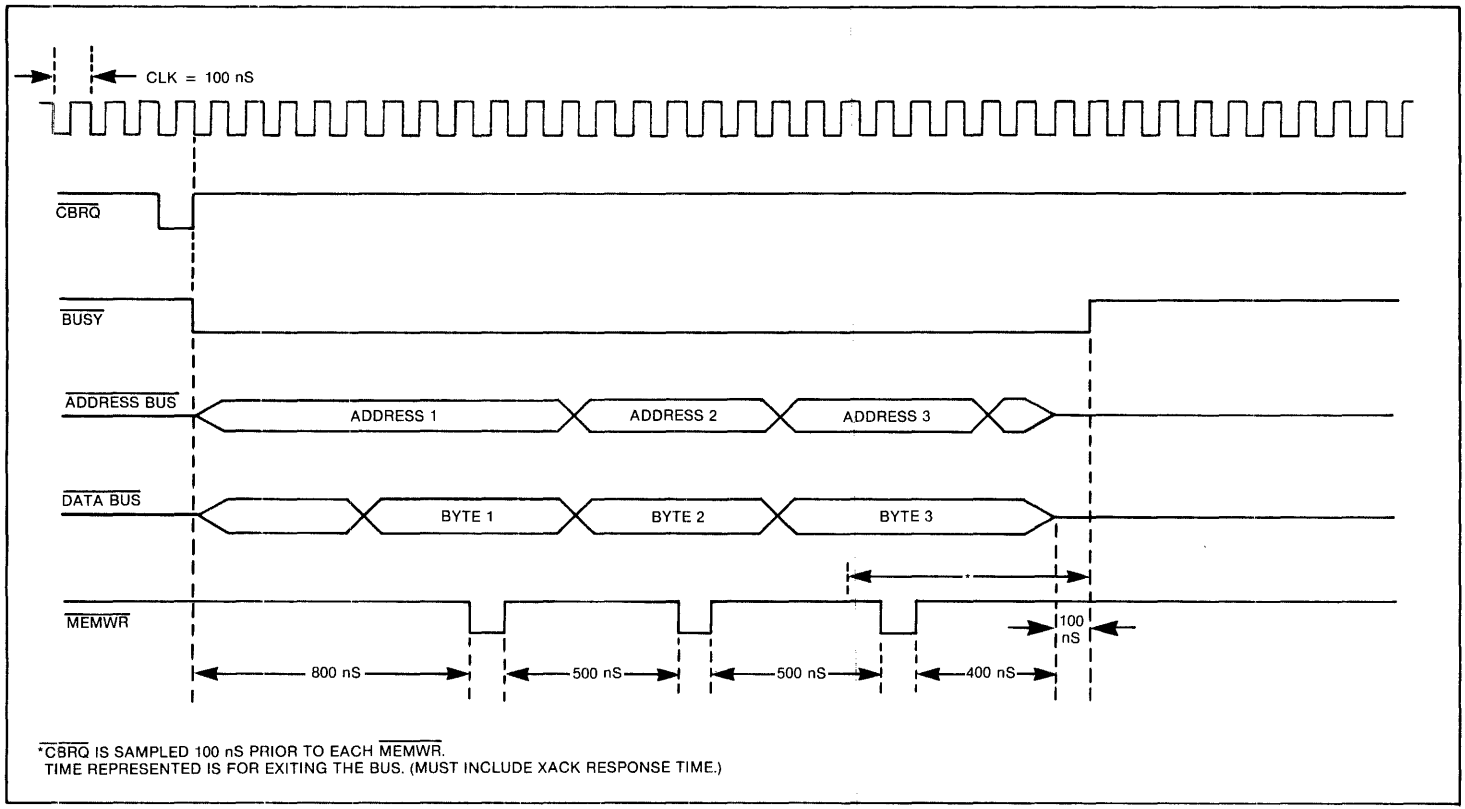


Figure 11. TYPICAL 3-WORD DATA TRANSFER TO HOST



*CBRQ IS SAMPLED 100 nS PRIOR TO EACH MEMWR.
TIME REPRESENTED IS FOR EXITING THE BUS. (MUST INCLUDE XACK RESPONSE TIME.)

Figure 12. TYPICAL 3-BYTE TRANSFER TO HOST

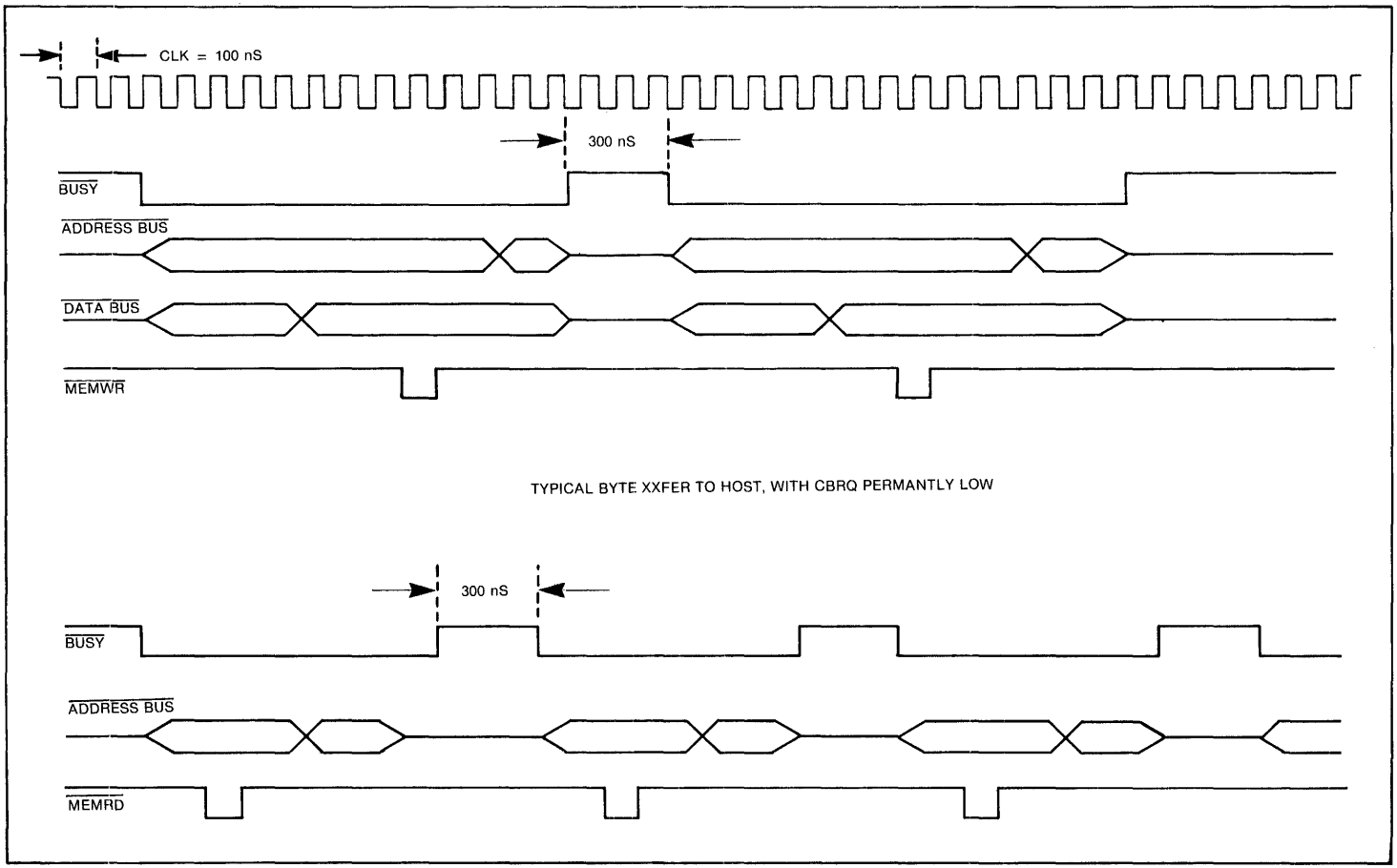


Figure 13. TYPICAL BYTE XFER FROM HOST WITH CBRQ PERMANTLY LOW

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WD1055-SCS SMD Controller Board

FEATURES

- SMD DRIVE INTERFACE COMPATABILITY
- 56 BIT ECC
- 1K ON-BOARD BUFFER
- 10 MBIT DATA TRANSFER RATE
- SASI™ HOST INTERFACE COMPATIBILITY
- 8/16 BIT INTERFACE WITH HOST
- CAPABLE OF 1:1 INTERLEAVE
- PROGRAMMABLE POLYNOMIAL GENERATOR
- MARGINAL DATA RECOVERY CAPABILITY
- SINGLE/MULTIPLE RECORD OPERATION
- HARD SECTOR FORMAT
- SINGLE/MULTIPLE UNIT DRIVE SUPPORT

DESCRIPTION

The WD1055-SCS provides the necessary interface and control for Host systems to store and retrieve data from SMD disk drives. The WD1055-SCS is fully compatible with Host systems using the SASI bus interface. This includes the logic necessary for communicating with the Host via the SASI bus and all sequencing and control signals required for operation.

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WESTERN DIGITAL
CORPORATION

WD1055-MTB Multibus™ SMD Disk Drive Controller Board

FEATURES

- SMD DRIVE INTERFACE COMPATABILITY
- 56 BIT ECC
- 1K ON-BOARD BUFFER
- 10 MBITS/SEC DATA TRANSFER RATE (SMD INTERFACE)
- MULTIBUS (IEEE 796) COMPATABILITY
- 8/16 BIT DATA STRUCTURE ON HOST INTERFACE
- CAPABLE OF 1-1 INTERLEAVE
- MARGINAL DATA RECOVERY CAPABILITY
- SINGLE/MULTIPLE RECORD OPERATION
- HARD SECTOR FORMAT
- SINGLE/MULTIPLE UNIT DRIVE SUPPORT

DESCRIPTION

The WD1055-MTB provides facilities necessary for Host Systems to store and retrieve data from SMD disk drives. The WD1055-MTB is also compatible with host systems conforming to the Multibus electrical and mechanical discipline as described in the IEEE 796 specification. This includes the logic necessary to communicate with the host or hosts via the Multibus and all the sequencing and control signals required for the operation of one or more masters within the Multibus module.

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WESTERN DIGITAL
CORPORATION

WD8206 Error Detection and Correction Unit

FEATURES

- Detects and Corrects All Single Bit Errors.
- Detects All Double Bit and Most Multiple Bit Errors
- 52 ns Maximum for Detection; 67 ns Maximum for Correction (16 Bit System)
- Expandable to Handle 80 Bit Memories
- Syndrome Outputs for Error Logging
- Separate Input and Output Busses — No Timing Strobes Required
- Supports Reads With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes
- HMOS Technology for Low Power
- 68 Pin Leadless JEDEC Package
- Single +5V Supply

GENERAL DESCRIPTION

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.

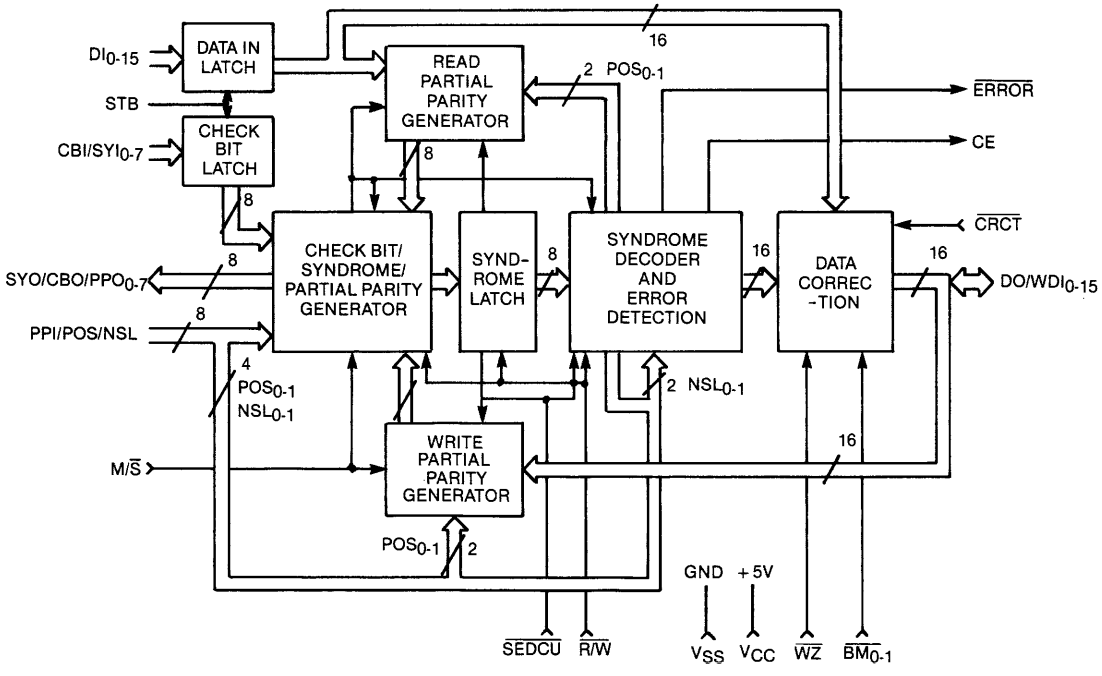


Figure 1. 8206 BLOCK DIAGRAM

Table 1. PIN DESCRIPTION

PIN NUMBER	SYMBOL	TYPE	NAME AND FUNCTION
1, 68-61, 59-53	DI_{0-15}	I	**Data In:** These inputs accept a 16 bit data word from RAM for error detection and/or correction.
5	CBI/SYI_0	I	**Check Bits In/Syndrome In:** In a single 8206 system, or in the master in a multi-8206 system, these inputs accept the check bits (5 to 8) from the RAM. In a single 8206 16 bit system, CBI_{0-5} are used. In slave 8206's these inputs accept the syndrome from the master.
6	CBI/SYI_1	I	
7	CBI/SYI_2	I	
8	CBI/SYI_3	I	
9	CBI/SYI_4	I	
10	CBI/SYI_5	I	
11	CBI/SYI_6	I	
12	CBI/SYI_7	I	
51	DO/WDI_0	I/O	**Data Out/Write Data In:** In a read cycle, data accepted by DI_{0-15} appears at these outputs corrected if CRCT is low, or uncorrected if CRCT is high. The BM inputs must be high to enable the output buffers during the read cycle. In a write cycle, data to be written into the RAM is accepted by these inputs for computing the write check bits. In a partial-write cycle, the byte not to be modified appears at either DO_{0-7} if BM_0 is high, or DO_{8-15} if BM_1 is high, for writing to the RAM. When WZ is active, it causes the 8206 to output all zeroes at DO_{0-15}, with the proper write check bits on CBO.
50	DO/WDI_1	I/O	
49	DO/WDI_2	I/O	
48	DO/WDI_3	I/O	
47	DO/WDI_4	I/O	
46	DO/WDI_5	I/O	
45	DO/WDI_6	I/O	
44	DO/WDI_7	I/O	
42	DO/WDI_8	I/O	
41	DO/WDI_9	I/O	
40	DO/WDI_{10}	I/O	
39	DO/WDI_{11}	I/O	
38	DO/WDI_{12}	I/O	
37	DO/WDI_{13}	I/O	
36	DO/WDI_{14}	I/O	
35	DO/WDI_{15}	I/O	
23	$SYO/CBO/PPO_0$	O	**Syndrome Out/Check Bits Out/Partial Parity Out:** In a single 8206 system, or in the master in a multi-8206 system, the syndrome appears at these outputs during a read. During a write, the write check bits appear. In slave 8206's the partial parity bits used by the master appear at these outputs. The syndrome is latched (during read-modify-writes) by R/W going low.
24	$SYO/CBO/PPO_1$	O	
25	$SYO/CBO/PPO_2$	O	
27	$SYO/CBO/PPO_3$	O	
28	$SYO/CBO/PPO_4$	O	
29	$SYO/CBO/PPO_5$	O	
30	$SYO/CBO/PPO_6$	O	
31	$SYO/CBO/PPO_7$	O	
13	PPI_0/POS_0	I	**Partial Parity In/Position:** In the master in a multi-8206 system, these inputs accept partial parity bits O and 1 from the slaves. In a slave 8206 these inputs inform it of its position within the system (1 to 4). Not used in a single 8206 system.
14	PPI_1/POS_1	I	
15	PPI_2/NSL_0	I	**Partial Parity In/Number of Slaves:** In the master in a multi-8206 system, these inputs accept partial parity bits 2 and 3 from the slaves. In a multi-8206 system these inputs are used in slave number 1 to tell it the total number of slaves in the system (1 to 4). Not used in other slaves or in a single 8206 system.
16	PPI_3/NSL_1	I	
17	PPI_4/CE	I/O	**Partial Parity In/Correctable Error:** In the master in a multi-8206 system this pin accepts partial parity bit 4. In slave number 1 only, or in a single 8206 system, this pin outputs the correctable error flag. CE is latched by R/W going low. Not used in other slaves.
18	PPI_5	I	**Partial Parity In:** In the master in a multi-8206 system these pins accept partial parity bits 5 to 7. The number of partial parity bits equals the number of check bits. Not used in single 8206 systems or in slaves.
19	PPI_6	I	
20	PPI_7	I	

Table 1. PIN DESCRIPTION (CONTINUED)

PIN NUMBER	SYMBOL	TYPE	NAME AND FUNCTION
22	ERROR	O	**Error:** This pin outputs the error flag in a single 8206 system or in the master of a multi-8206 system. It is latched by R/W going low. Not used in slaves.
52	CRCT	I	**Correct:** When low this pin causes data correction during a read or read-modify-write cycle. When high, it causes error correction to be disabled, although error checking is still enabled.
2	STB	I	**Strobe:** STB is an input control used to strobe data at the DI inputs and check-bits at the CBI/SYI inputs. The signal is active high to admit the inputs. The signals are latched by the high-to-low transition of STB.
33 32	BM_0 BM_1	I I	**Byte Marks:** When high, the Data Out pins are enabled for a read cycle. When low, the Data Out buffers are tristated for a write cycle. BM_0 controls DO_{0-7}, while BM_1 controls DO_{8-15}. In partial (bytes) writes, the byte mark input is low for the new byte to be written.
21	R/W	I	**Read/Write:** When high this pin causes the 8206 to perform detection and correction (if CRCT is low). When low, it causes the 8206 to generate check bits. On the high-to-low transition the syndrome is latched internally for read-modify-write cycles.
34	WZ	I	**Write Zero:** When low this input overrides the BM_{0-1} and R/W inputs to cause the 8206 to output all zeros at DO_{0-15} with the corresponding check bits at CBO_{0-7}. Used for memory initialization.
4	M/S	I	**Master/Slave:** Input tells the 8206 whether it is a master (high) or a slave (low).
3	SEDCU	I	**Single EDC Unit:** Input tells the master whether it is operating as a single 8206 (low) or as the master in a multi-8206 system (high). Not used in slaves.
60	V_{CC}	I	**Power Supply:** +5V
26	V_{SS}	I	**Logic Ground**
43	V_{SS}	I	**Output Driver Ground**

FUNCTIONAL DESCRIPTION

The 8206 Error Detection and Correction Unit provides greater memory system reliability through its ability to detect and correct memory errors. It is a single chip device that can detect and correct all single bit errors and detect all double bit and some higher multiple bit errors. Some other odd multiple bit errors (e.g., 5 bits in error) are interpreted as single bit errors, and the CE flag is raised. While some even multiple bit errors (e.g., 4 bits in error) are interpreted as no error, most are detected as double bit errors. This error handling is a function of the number of check bits used by the 8206 (see Figure 2) and the specific Hamming code used. Errors in check bits are not distinguished from errors in a word.

A single 8206 handles 8 or 16 bits of data, and up to 5 8206's can be cascaded in order to handle data paths of 80 bits. For a single 8206 8 bit system, the DI_{8-15}, DO/WDI_{8-15} and BM_1 inputs are grounded. See the Multi-Chip systems section for information on 24-80 bit systems.

The 8206 has a "flow through" architecture. It supports two kinds of error correction architecture: 1) Flow-through, or correct-always; and 2) Parallel, or check-only. There are two separate 16-pin busses, one to accept data from the RAM (DI) and the other to deliver corrected data to the system bus (DO/WDI). The logic is entirely combinatorial during a read cycle. This is in contrast to an architecture with only one bus, with bidirectional bus drivers that must first read the data and then be turned around to output the corrected data. The latter architecture typically requires additional hardware (latches and/or transceivers) and may be slower in a system due to timing skews of control signals.

DATA WORD BITS	CHECK BITS
8	5
16	6
24	6
32	7
40	7
48	8
56	8
64	8
72	8
80	8

Figure 2: NUMBER OF CHECK BITS USED BY 8206

READ CYCLE

With the R/W pin high, data is received from the RAM outputs into the DI pins where it is optionally latched by the STB signal. Check bits are generated from the data bits and compared to the check bits read from the RAM into the CBI pins. If an error is detected the ERROR flag is activated and the correctable error flag (CE) is used to inform the system whether the error was correctable or not. With the BM inputs high, the word appears corrected at the DO pins if the error was correctable, or unmodified if the error was uncorrectable.

If more than one 8206 is being used, then the check bits are read by the master. The slaves generate a partial parity output (PPO) and pass it to the master. The master 8206 then generates and returns the syndrome to the slaves (SYO) for correction of the data.

The 8206 may alternatively be used in a "check-only" mode with the CRCT pin left high. With the correction facility turned off, the propagation delay from memory outputs to 8206 outputs is significantly shortened. In this mode the 8206 issues an ERROR flag to the CPU, which can then perform one of several options: lengthen the current cycle for correction, restart the instruction, perform a diagnostic routine, etc.

A syndrome word, five to eight bits in length and containing all necessary information about the existence and location of an error, is made available to the system at the SYO_{0-7} pins. Error logging may be accomplished by latching the syndrome and the memory address of the word in error.

WRITE CYCLE

For a full write, in which an entire word is written to memory, the data is written directly to the RAM, bypassing the 8206. The same data enters the 8206 through the WDI pins where check bits are generated. The Byte Mark inputs must be low to tristate the DO drivers. The check bits, 5 to 8 in number, are then written to the RAM through the CBO pins for storage along with the data word. In a multi-chip system, the master writes the check bits using partial parity information from the slaves.

In a partial write, part of the data word is overwritten, and part is retained in memory. This is accomplished by performing a read-modify-write cycle. The complete old word is read into the 8206 and corrected, with the syndrome internally latched by R/W going low. Only that part of the word not to be modified is output onto the DO pins, as controlled by the Byte Mark inputs. That portion of the word to be overwritten is supplied by the system bus. The 8206 then calculates check bits for the new word, using the byte from the previous read and the new byte from the system bus, and writes them to the memory.

READ-MODIFY-WRITE CYCLES

Upon detection of an error the 8206 may be used to correct the bit in error in memory. This reduces the probability of getting multiple-bit errors in subsequent read cycles. This correction is handled by executing read-modify-write cycles.

The read-modify-write cycle is controlled by the R/W input. After (during) the read cycle, the system dynamic RAM controller or CPU examines the 8206 ERROR and CE outputs to determine if a correctable error occurred. If it did, the dynamic RAM controller or CPU forces R/W low, telling the 8206 to latch the generated syndrome and drive the corrected check bits onto the CBO outputs. The corrected data is available on the DO pins. The DRAM controller then writes the corrected data and corresponding check bits into memory.

The 8206 may be used to perform read-modify-writes in one or two RAM cycles. If it is done in two cycles, the 8206 latches are used to hold the data and check bits from the read cycle to be used in the following write cycle. The WD8207 Advanced Dynamic RAM controller allows read-modify-write cycles in one memory cycle. See the System Environment section.

INITIALIZATION

A memory system operating with ECC requires some form of initialization at system power-up in order to set valid data and check bit information in memory. The 8206 supports memory initialization by the write zero function. By activating the WZ pin, the 8206 will write a data pattern of zeros and the associated check bits in the current write cycle. By thus writing to all memory at power-up, a controller can set memory to valid data and check bits. Massive memory failure, as signified by both data and check bits all ones or zeros, will be detected as an uncorrectable error.

MULTI-CHIP SYSTEMS

A single 8206 handles 8 or 16 bits of data and 5 or 6 check bits, respectively. Up to 5 8206's can be cascaded for 80 bit memories with 8 check bits.

When cascaded, one 8206 operates as a master, and all others as slaves. As an example, during a read cycle in a 32 bit system with one master and one

slave, the slave calculates parity on its portion of the word — "partial parity" — and presents it to the master through the PPO pins. The master combines the partial parity from the slave with the parity it calculated from its own portion of the word to generate the syndrome. The syndrome is then returned by the master to the slave for error correction. In systems with more than one slave the above description continues to apply, except that the partial parity outputs of the slaves must be XOR'd externally. Figure 3 shows the necessary external logic for multi-chip systems. Write and read-modify-write cycles are carried out analogously. See the System Operation section for multi-chip wiring diagrams.

There are several pins used to define whether the 8206 will operate as a master or a slave. Tables 2 and 3 illustrate how these pins are tied.

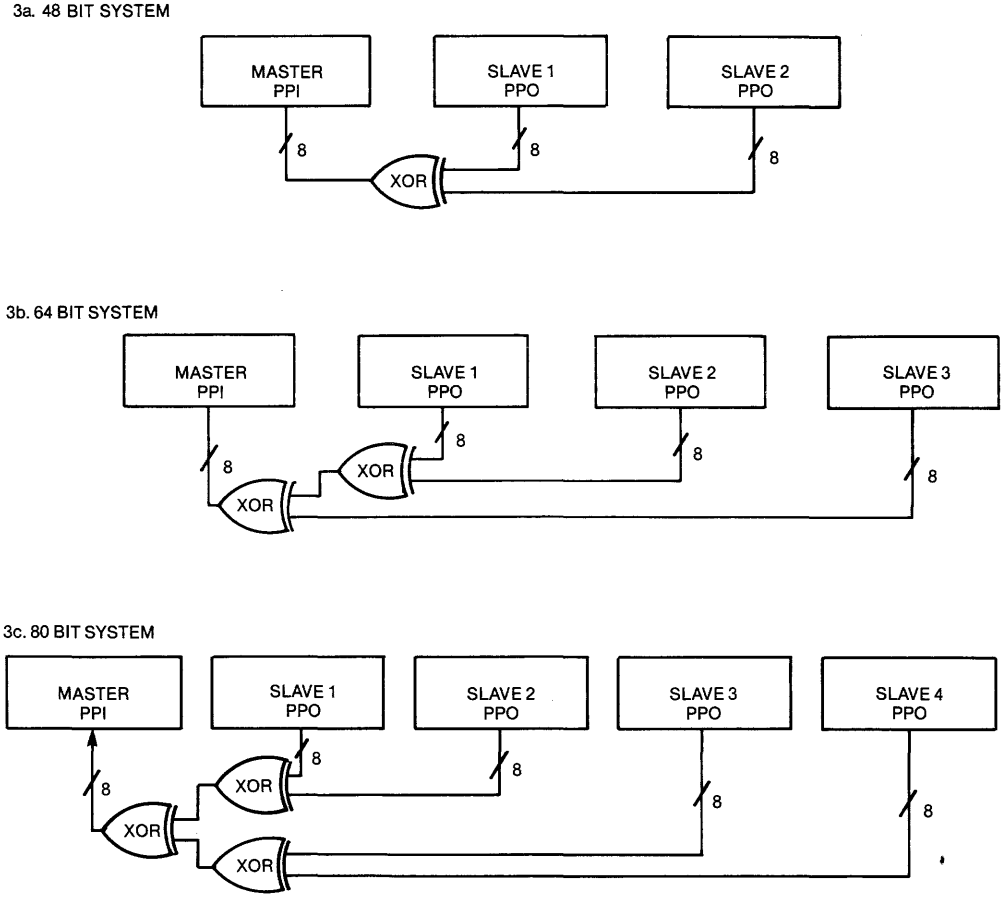


Figure 3. EXTERNAL LOGIC FOR MULTI-CHIP SYSTEMS

Table 2. MASTER/SLAVE PIN ASSIGNMENTS

PIN NO.	PIN NAME	MASTER	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4
4	M/S	+5V	Gnd	Gnd	Gnd	Gnd
3	SEDCU	+5V	+5V	+5V	+5V	+5V
13	PPI_0/POS_0	PPI	Gnd	+5V	Gnd	+5V
14	PPI_1/POS_1	PPI	Gnd	Gnd	+5V	+5V
15	PPI_2/NSL_0	PPI	*	+5V	+5V	+5V
16	PPI_3/NSL_1	PPI	*	+5V	+5V	+5V

* See Table 3.

NOTE:
Pins 13, 14, 15, 16 have internal pull-up resistors and may be left as N.C. where specified as connecting to +5V.

Table 3. NSL PIN ASSIGNMENTS FOR SLAVE 1

	NUMBER OF SLAVES			
PIN	1	2	3	4
PPI_2/NSL_0	Gnd	+5V	Gnd	+5V
PPI_3/NSL_1	Gnd	Gnd	+5V	+5V

The timing specifications for multi-chip systems must be calculated to take account of the external XOR gating in 3, 4, and 5-chip systems. Let tXOR be the delay for a single external TTL XOR gate. Then the following equations show how to calculate the relevant timing parameters for 2-chip (n = 0), 3-chip (n = 1), 4-chip (n = 2), and 5-chip (n = 2) systems:

Data-in to corrected data-out (read cycle) =
TDVSV + TPVSV + TSVQV + ntXOR

Data-in to error flag (read cycle) =
TDVSV + TPVEV + ntXOR

Data-in to correctable error flag (read cycle) =
TDVSV + TPVSV + TSVCV + ntXOR

Write data to check-bits valid (full write cycle) =
TQVQV + TPVSV + ntXOR

Data-in to check-bits valid (read-mod-write cycle) =
TDVSV + TPVSV + TSVQV + TQVQV +
TPVSV + 2ntXOR

Data-in to check-bits valid (non-correcting read-modify-write cycle) =
TDVQU + TQVQV + TPVSV + ntXOR

HAMMING CODE

The 8206 uses a modified Hamming code which was optimized for multi-chip EDCU systems. The code is such that partial parity is computed by all 8206's in parallel. No 8206 requires more time for propagation through logic levels than any other one, and hence no one device becomes a bottleneck in the parity operation. However, one or two levels of external TTL XOR gates are required in systems with three to five chips. The code appears in Table 4. The check bits are derived from the table by XORing or XNORing together the bits indicated by 'X's in each row corresponding to a check bit. For example, check bit 0 in the MASTER for data word 1000110101101011 will be "0." It should be noted that the 8206 will detect the gross-error condition of all lows or all highs.

Error correction is accomplished by identifying the bad bit and inverting it. Table 4 can also be used as an error syndrome table by replacing the 'X's with '1's. Each column then represents a different syndrome word, and by locating the column corresponding to a particular syndrome the bit to be corrected may be identified. If the syndrome cannot be located then the error cannot be corrected. For example, if the syndrome word is 00110111, the bit to be corrected is bit 5 in the slave one data word (bit 21).

The syndrome decoding is also summarized in Table 5, which can be used for error logging. By finding the appropriate syndrome word (starting with bit zero, the least significant bit), the result is either: 1) no error; 2) an identified (correctable) single bit error; 3) a double bit error; or 4) a multi-bit uncorrectable error.

Table 4. MODIFIED HAMMING CODE CHECK BIT GENERATION

Check bits are generated by XOR'ing (except for the CB0 and CB1 data bits, which are XNOR'ed in the Master) the data bits in the rows corresponding to the check bits. Note there are 6 check bits in a 16-bit system, 7 in a 32-bit system, and 8 in 48-or-more-bit systems.

BYTE NUMBER	0								1								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	XNOR
CB1 =	X	—	X	—	—	X	—	X	—	X	—	X	X	—	X	—	XNOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
CB5 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
CB6 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
CB7 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
DATA BITS	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	

16 BIT OR MASTER

	2								3								OPERATION
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	XOR
	X	X	X	—	—	X	—	X	X	X	—	—	—	—	—	X	XOR
	—	X	X	X	—	X	X	X	—	—	X	X	—	—	—	—	XOR
	X	X	—	—	X	—	X	X	X	—	—	X	X	—	—	—	XOR
	X	X	—	—	X	X	X	X	—	—	—	—	X	—	X	—	XOR
	—	—	—	X	X	X	X	X	—	X	X	X	—	—	X	X	XOR
	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3	
	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	

SLAVE #1

BYTE NUMBER	4								5								6								7								8								9								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	X	—	X	X	—	—	X	—	—	X	X	X	—	X	X	—	—	X	X	—	X	—	—	X	—	X	X	—	—	X	—	—	XOR
CB1 =	X	—	X	—	—	X	—	X	—	X	—	X	X	—	X	—	X	X	X	—	—	—	X	—	—	X	X	X	—	X	X	X	—	—	X	X	—	—	—	—	—	X	X	—	—	—	—	—	XOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	—	X	X	X	—	X	X	—	X	—	—	X	—	X	X	—	—	X	X	—	X	—	—	X	—	X	X	—	X	—	—	X	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	X	—	—	X	—	—	X	X	X	X	—	—	X	X	X	—	X	X	X	X	—	—	X	—	X	X	—	—	—	—	X	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	—	X	X	—	—	—	—	X	X	X	X	X	—	—	—	X	XOR
CB5 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	—	X	X	X	X	—	X	—	—	—	X	—	—	—	X	XOR
CB6 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	—	—	X	X	X	X	—	—	—	—	X	—	X	—	XOR
CB7 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
DATA BITS	3	3	3	3	3	3	3	3	4	4	4	4	4	4	4	4	4	4	5	5	5	5	5	5	5	5	5	5	6	6	6	6	6	6	6	6	6	6	7	7	7	7	7	7	7	7	7	7	
	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	

SLAVE #2 | SLAVE #3 | SLAVE #4

Table 5. SYNDROME DECODING

Syndrome Bits 7	6	5	4	0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 1 2 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 1 3 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
0	0	0	0	N CB0 CB1 D CB2 D D 18 CB3 D D 0 D 1 2 D
0	0	0	1	CB4 D D 5 D 6 7 D D 3 16 D 4 D D 17
0	0	1	0	CB5 D D 11 D 19 12 D D 8 9 D 10 D D 67
0	0	1	1	D 13 14 D 15 D D 21 20 D D 66 D 22 23 D
0	1	0	0	CB6 D D 25 D 26 49 D D 48 24 D 27 D D 50
0	1	0	1	D 52 55 D 51 D D 70 28 D D 65 D 53 54 D
0	1	1	0	D 29 31 D 64 D D 69 68 D D 32 D 33 34 D
0	1	1	1	30 D D 37 D 38 39 D D 35 71 D 36 D D U
1	0	0	0	CB7 D D 43 D 77 44 D D 40 41 D 42 D D U
1	0	0	1	D 45 46 D 47 D D 74 72 D D U D 73 U D
1	0	1	0	D 59 75 D 79 D D 58 60 D D 56 D U 57 D
1	0	1	1	63 D D 62 D U U D D U U D 61 D D U
1	1	0	0	D U U D U D D U 76 D D U D U U D
1	1	0	1	78 D D U D U U D D U U D D U D U
1	1	1	0	U D D U D U U D D U U D U D D U
1	1	1	1	D U U D U D D U U D D U D U U D

N = No Error
CBX = Error in Check Bit X
X = Error in Data Bit X
D = Double Bit Error
U = Uncorrectable Multi-Bit Error

SYSTEM ENVIRONMENT

The 8206 interface to a typical 32 bit memory system is illustrated in Figure 4. For larger systems, the partial parity bits from slaves two to four must be XOR'ed externally, which calls for one level of XOR gating for three 8206's and two levels for four or five 8206's.

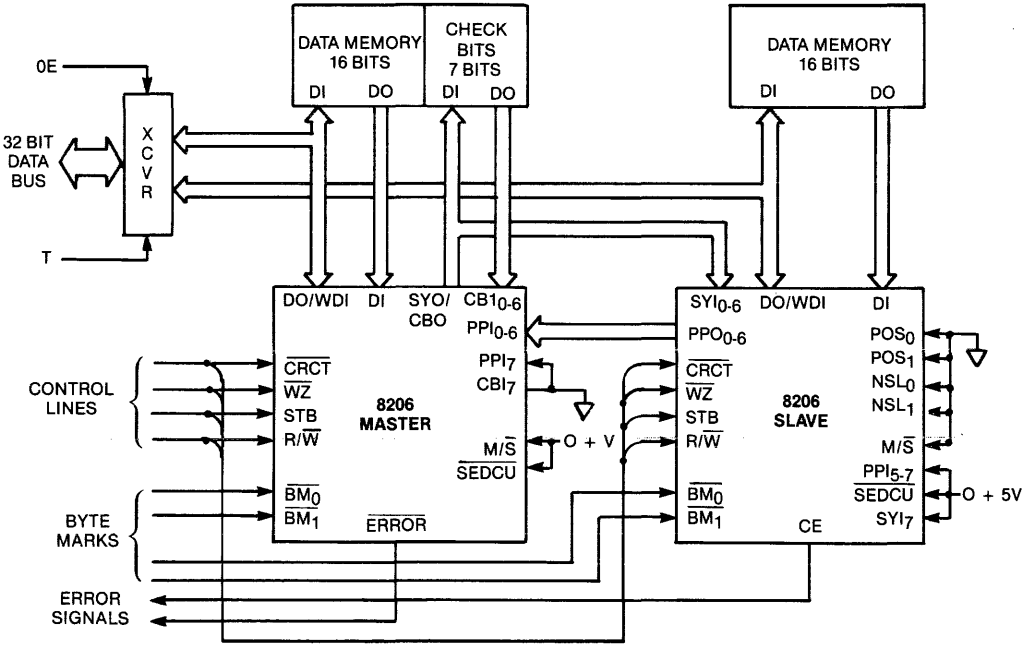


Figure 4. 32-BIT 8206 SYSTEM INTERFACE

The 8206 is designed for direct connection to the WD8207 Advanced Dynamic RAM Controller, due to be sampled in the first quarter of 1983. The 8207 has the ability to perform dual port memory control and Figure 5 illustrates a highly integrated dual port RAM implementation using the 8206 and 8207. The 8206/8207 combination permits such features as automatic scrubbing (correcting errors in memory during refresh), extending RAS and CAS timings for Read-Modify-Writes in single memory cycles, and automatic memory initialization upon reset. Together these two chips provide a complete dual-port, error-corrected dynamic RAM subsystem.

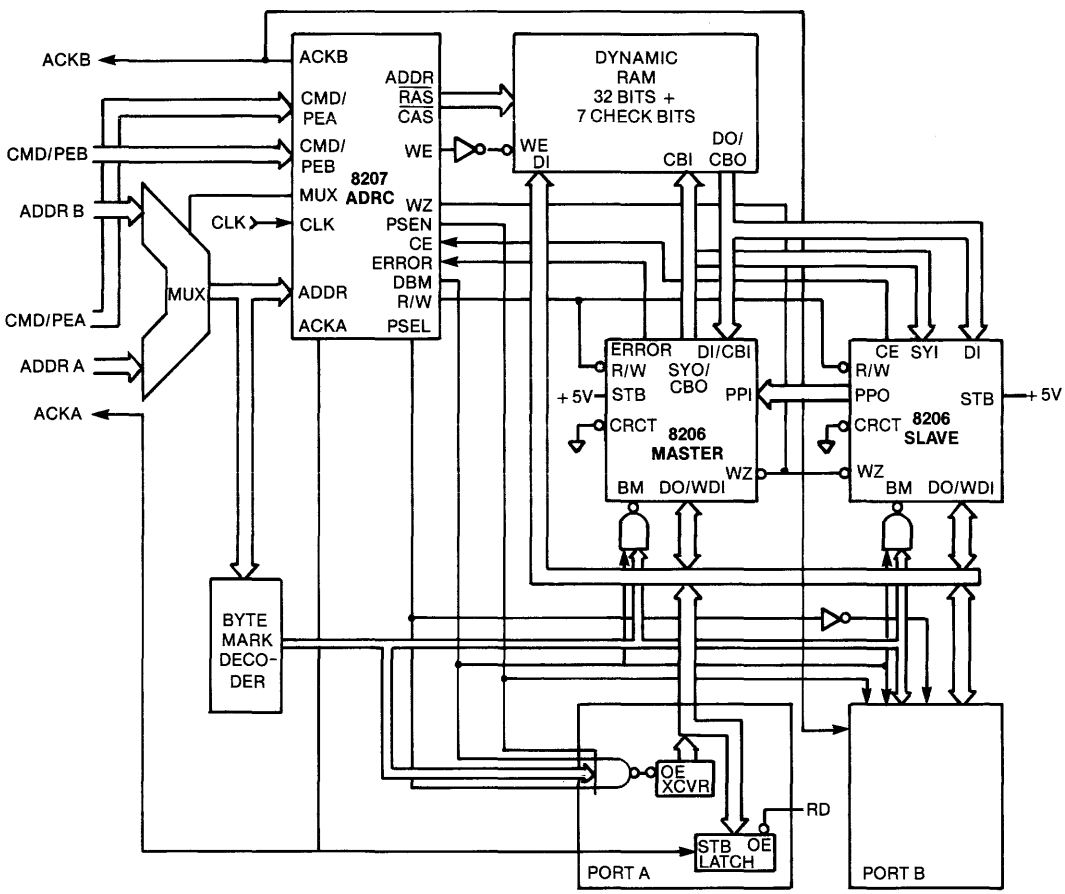


Figure 5. DUAL PORT RAM SUBSYSTEM WITH 8206/8207 (32-BIT BUS)

MEMORY BOARD TESTING

The 8206 lends itself to straightforward memory board testing with a minimum of hardware overhead. The following is a description of four common test modes and their implementation.

Mode 0 — Read and write with error correction.
Implementation: This mode is the normal 8206 operating mode.

Mode 1 — Read and write data with error correction disabled to allow test of data memory.
Implementation: This mode is performed with CRCT deactivated.

Mode 2 — Read and write check bits with error correction disabled to allow test of check bits memory.
Implementation: Any pattern may be written into the check bits memory by judiciously choosing the proper data word to generate the desired check bits, through the use of the 8206 Hamming code. To read out the check bits it is first necessary to fill the data memory with all zeros, which may be done by activating WZ and incrementing memory addresses with WE to the check bits memory held inactive, and then performing ordinary reads. The check bits will then appear directly at the SYO outputs, with bits CB0 and CB1 inverted.

Mode 3 — Write data, without altering or writing check bits, to allow the storage of bit combinations to cause error correction and detection.
Implementation: This mode is implemented by writing the desired word to memory with WE to the check bits array held inactive.

PACKAGE

The 8206 is packaged in a 68-pin, leadless JEDEC type A hermetic chip carrier. Figure 6 illustrates the package, and Figure 7 is the pinout.

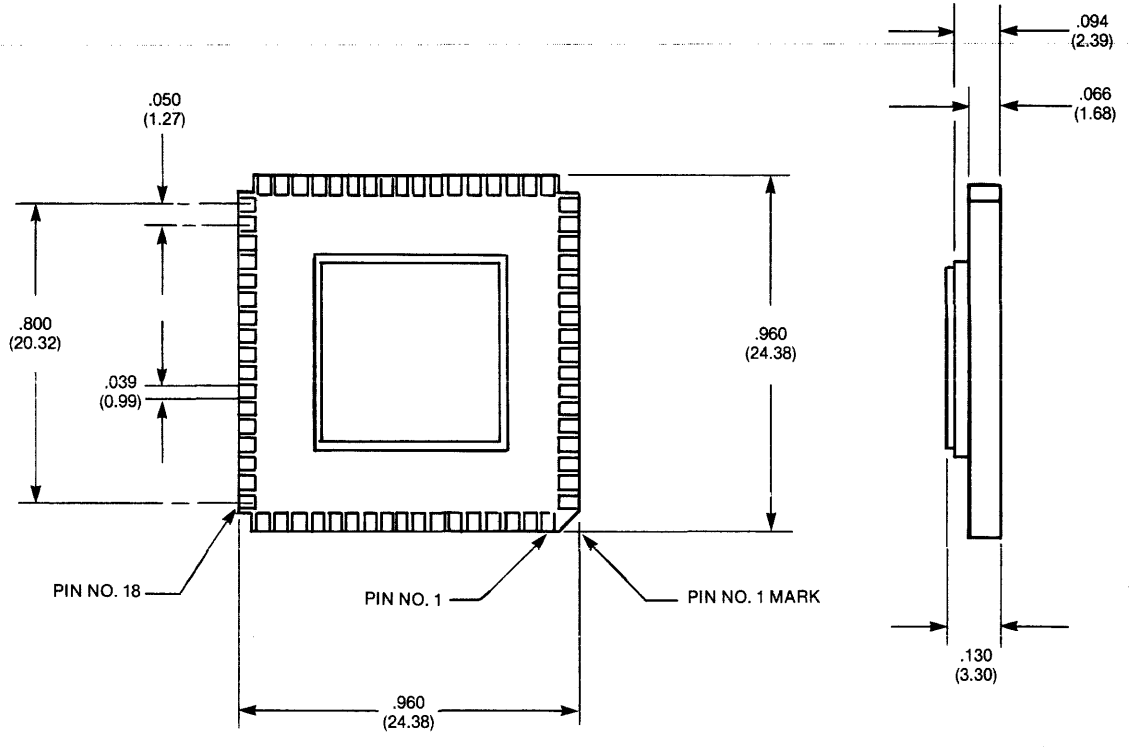


Figure 6. 8206 JEDEC TYPE A PACKAGE

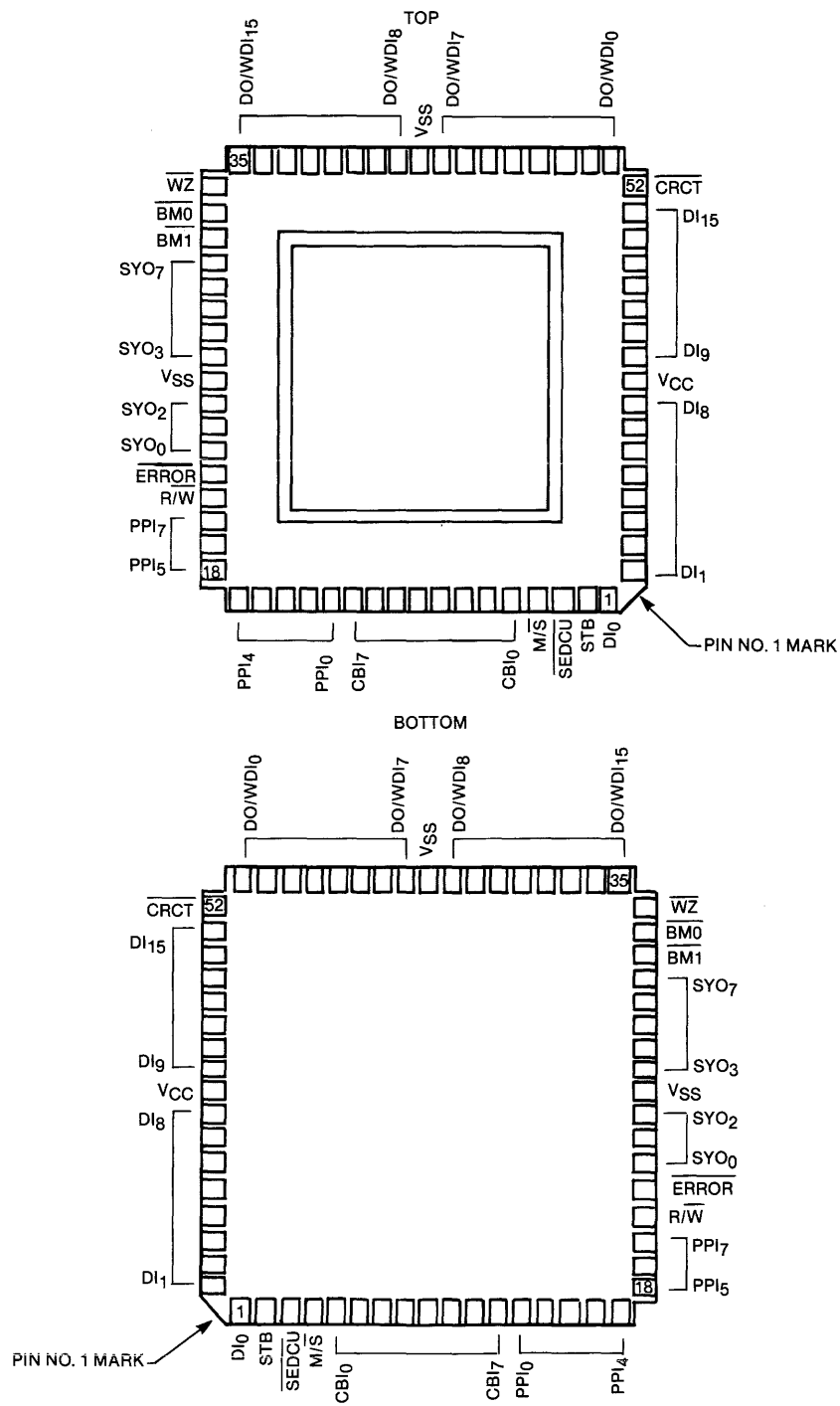


Figure 7. 8206 PINOUT DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 2.5 Watts

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

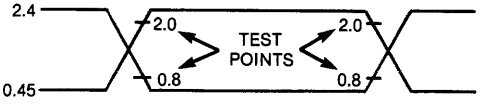
D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, V_{SS} = GND)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{CC}	Power Supply Current — Single 8206 or Slave #1 — Master in Multi-Chip or Slaves #2, 3, 4		 270 230	 mA mA	
V_{IL}[1]	Input Low Voltage	−0.5	0.8	V	
V_{IH}[1]	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage — DO — All Others	 	 0.4 0.4	 V V	 I_{OL} = 8mA I_{OL} = 2.0mA
V_{OH}	Output High Voltage — DO, CBO — All Other Outputs	 2.6 2.4	 	 V V	 I_{OH} = −2mA I_{OH} = 0.4mA
I_{LO}	I/O Leakage Current — PPI_4/CE — DO/WDI_{0-15}	 	 ± 20 ± 10	 μA μA	 0.45V ⩽ $V_{I/O}$ ⩽ V_{CC}
I_{LI}	Input Leakage Current — $PPI_{0-3, 5-7}$, CBI_{6-7}, SEDCU[2] — All Other Input Only Pins	 	 ± 20 ± 10	 μA μA	 0V ⩽ V_{IN} ⩽ V_{CC}

NOTES:

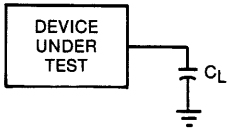
1. SEDCU (pin 3) and M/S (pin 4) are device strapping options and should be tied to V_{CC} or GND. V_{IH} min = V_{CC} − 0.5V and V_{IL} max = 0.5V.
2. PPI_{0-7} (pins 13-20) and CBI_{6-7} (pins 11, 12) have internal pull-up resistors and if left unconnected will be pulled to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 and 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1 AND 0.8V FOR A LOGIC 0.

A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V, C_L = 100pF; all times are in nsec.)

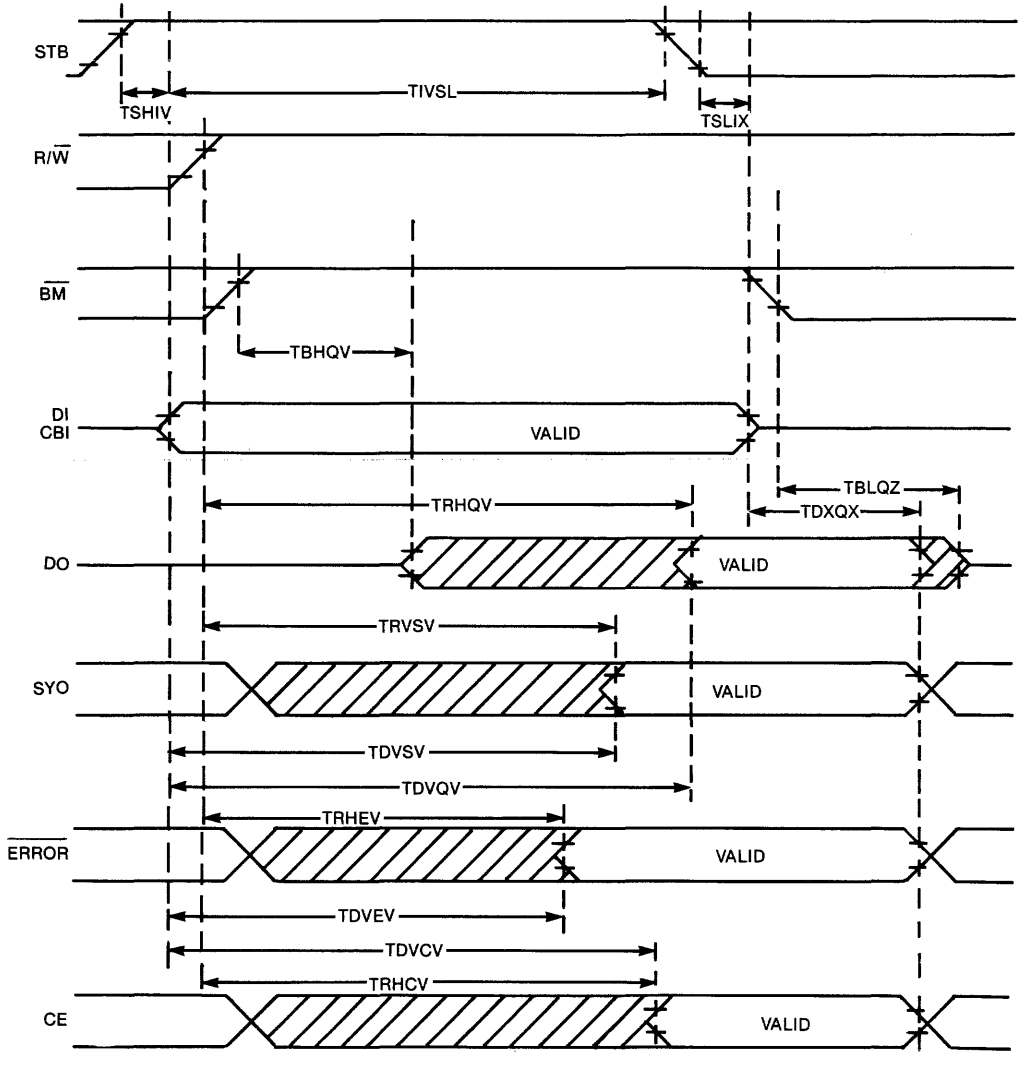
SYMBOL	PARAMETER	8206		8206-8		NOTES
		MIN.	MAX.	MIN.	MAX.	
TRHEV	ERROR Valid from R/W↑		25		34	
TRHCV	CE Valid from R/W↑ (Single 8206)		44		59	
TRHQV	Corrected Data Valid from R/W↑		54		66	1
TRVSV	SYO/CBO/PPO Valid from R/W		42		56	1
TDVEV	ERROR Valid from Data/Check Bits In		52		70	
TDVCV	CE Valid from Data/Check Bits In		70		94	
TDVQV	Corrected Data Valid from Data/Check Bits In		67		90	
TDVSV	SYO/PPO Valid from Data/Check Bits In		55		74	
TBHQV	Corrected Data Access Time		37		43	
TDXQX	Hold Time from Data/Check Bits In	0		0		1
TBLQZ	Corrected Data Float Delay	0	28	0	38	1
TSHIV	STB High to Data/Check Bits in Valid	30		40		2
TIVSL	Data/Check Bits In to STB↓ Set-up	5		5		
TSLIX	Data/Check Bits In from STB↓ Hold	25		30		
TPVEV	ERROR Valid from Partial Parity In		30		40	
TPVQV	Corrected Data (Master) from Partial Parity In		61		76	1
TPVSV	Syndrome/Check Bits Out from Partial Parity In		43		51	1
TSVQV	Corrected Data (Slave) Valid from Syndrome		51		69	
TSVCV	CE Valid from Syndrome (Slave number 1)		48		65	
TQVQV	Check Bits/Partial Parity Out from Write Data In		64		80	1
TRHSX	Check Bits/Partial Parity Out from R/W, WZ Hold	0		0		1
TRLSX	Syndrome Out from R/W Hold	0		0		
TQXQX	Hold Time from Write Data In	0		0		1
TSVRL	Syndrome Out to R/W↓ Set-up	17		22		
TDVRL	Data/Check Bits In to R/W Set-up	39		46		1
TDVQU	Uncorrected Data Out from Data In		32		43	
TTVQV	Corrected Data Out from CRCT↓		30		40	
TWLQL	WZ↓ to Zero Out		30		40	
TWHQX	Zero Out from WZ↑ Hold	0		0		

NOTES:

1. A.C. Test Levels for CBO and DO are 2.4V and 0.8V.
2. T_{SHIV} is required to guarantee output delay timings: T_{DVEV}, T_{DVCV}, T_{DVSV}. T_{SHIV} + T_{IVSL} guarantees a min STB pulse width of 35 ns (45 ns for the 8206-8).

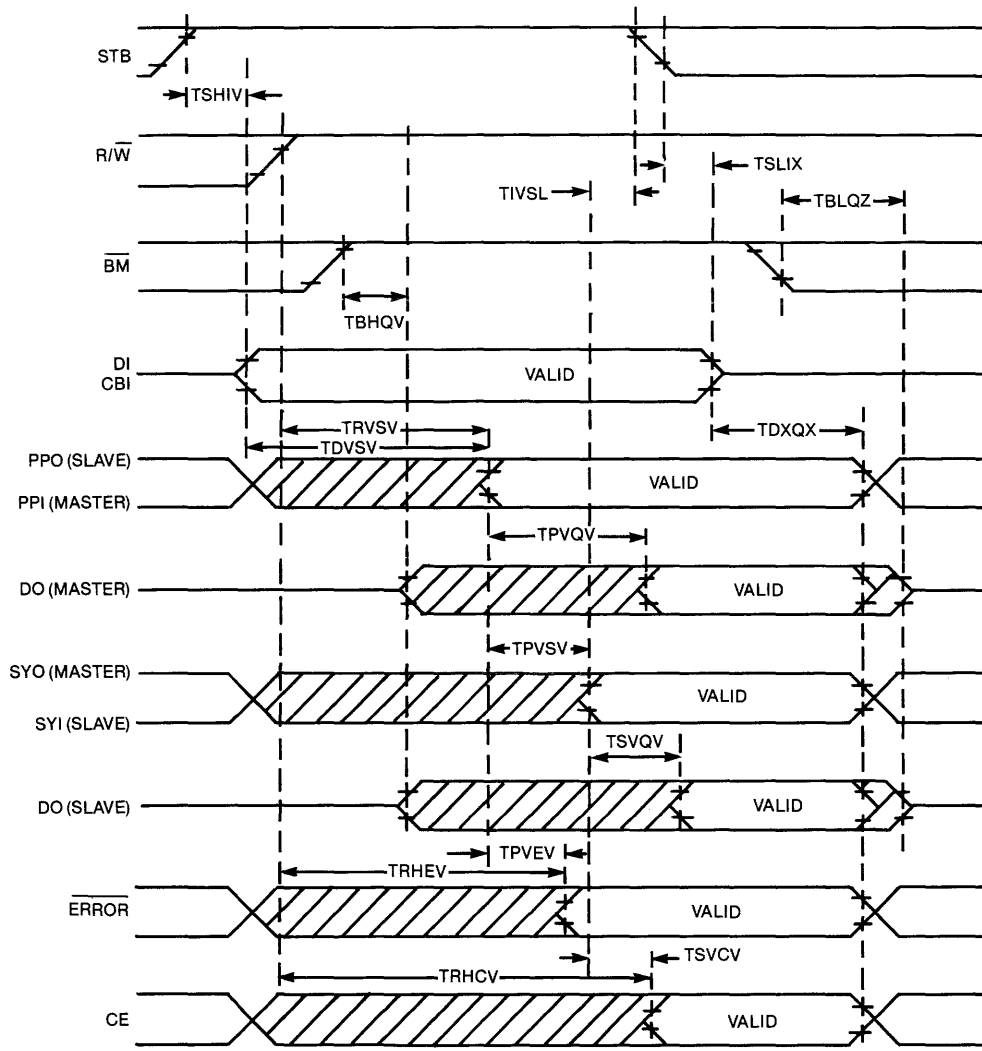
WAVEFORMS

READ — 16 BIT ONLY



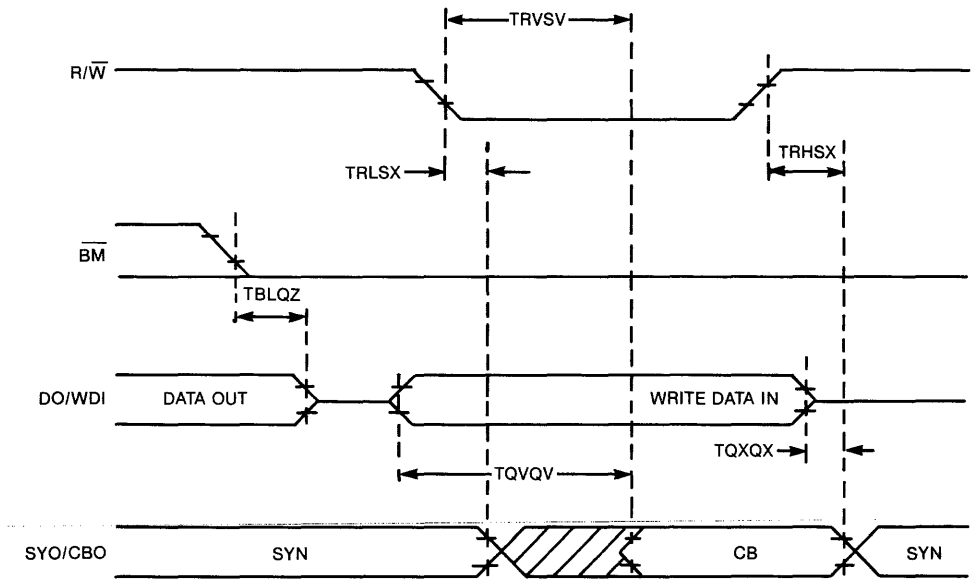
WAVEFORMS (Continued)

READ — MASTER/SLAVE

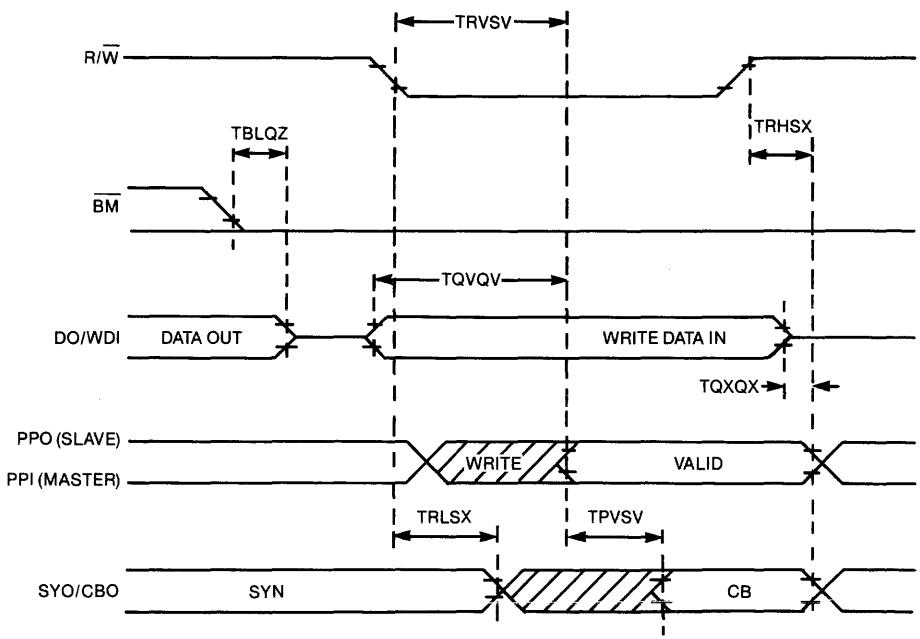


WAVEFORMS (Continued)

FULL WRITE — 16 BIT ONLY

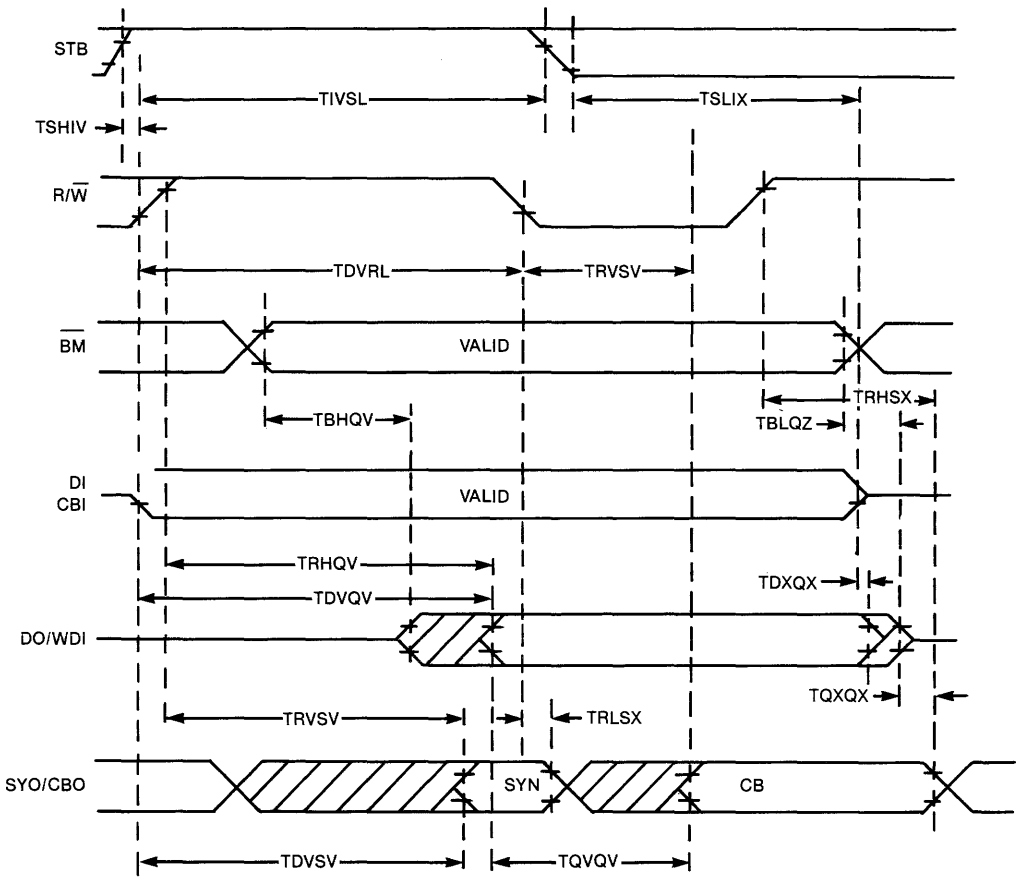


FULL WRITE — MASTER/SLAVE



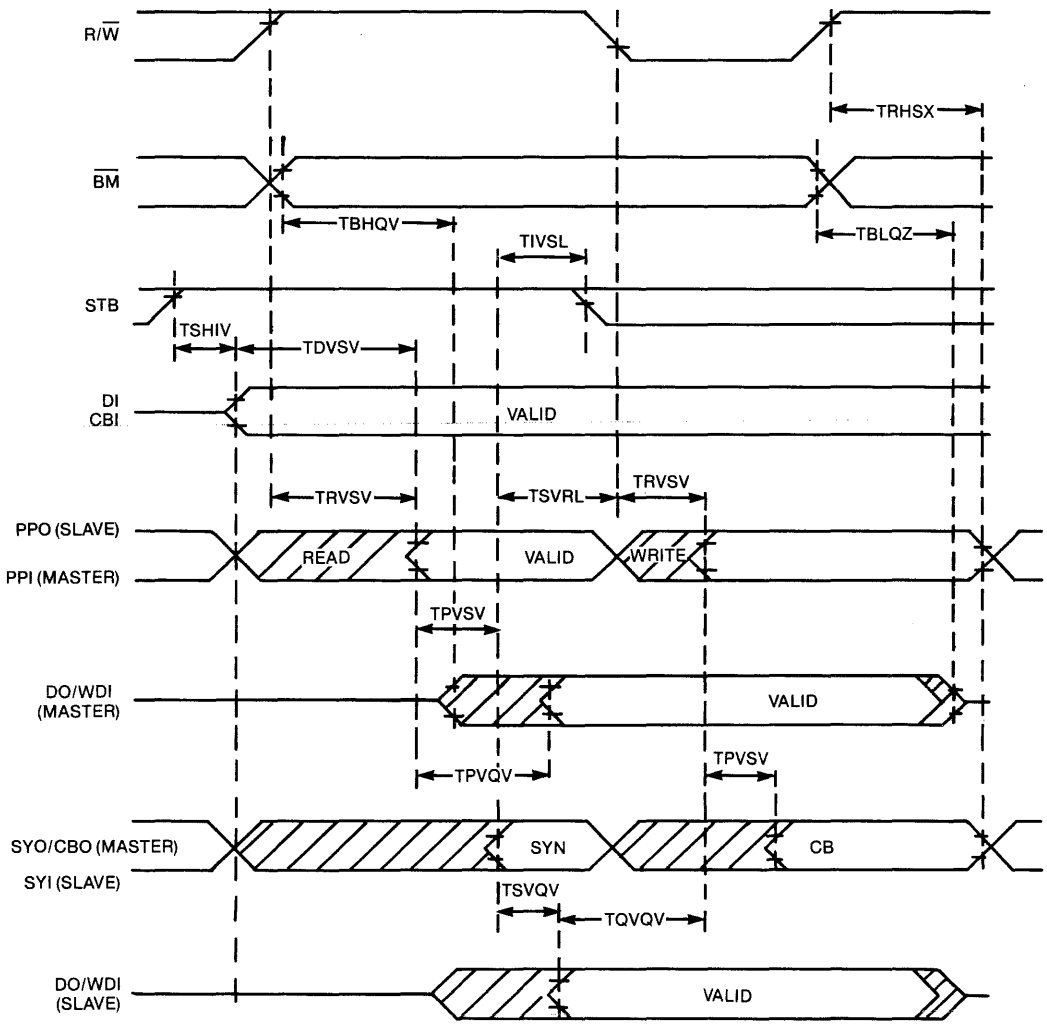
WAVEFORMS (Continued)

READ MODIFY WRITE — 16 BIT ONLY



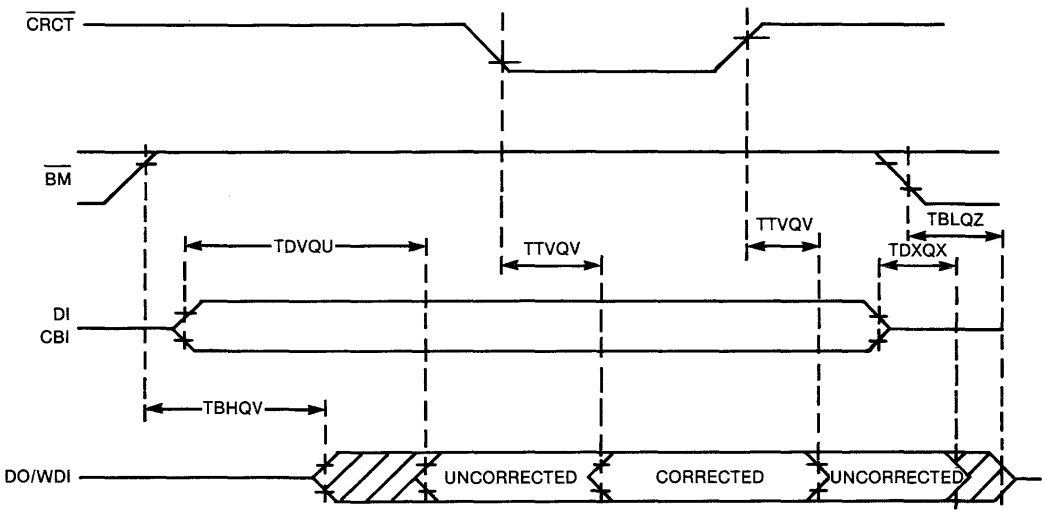
WAVEFORMS (Continued)

READ MODIFY WRITE — MASTER/SLAVE

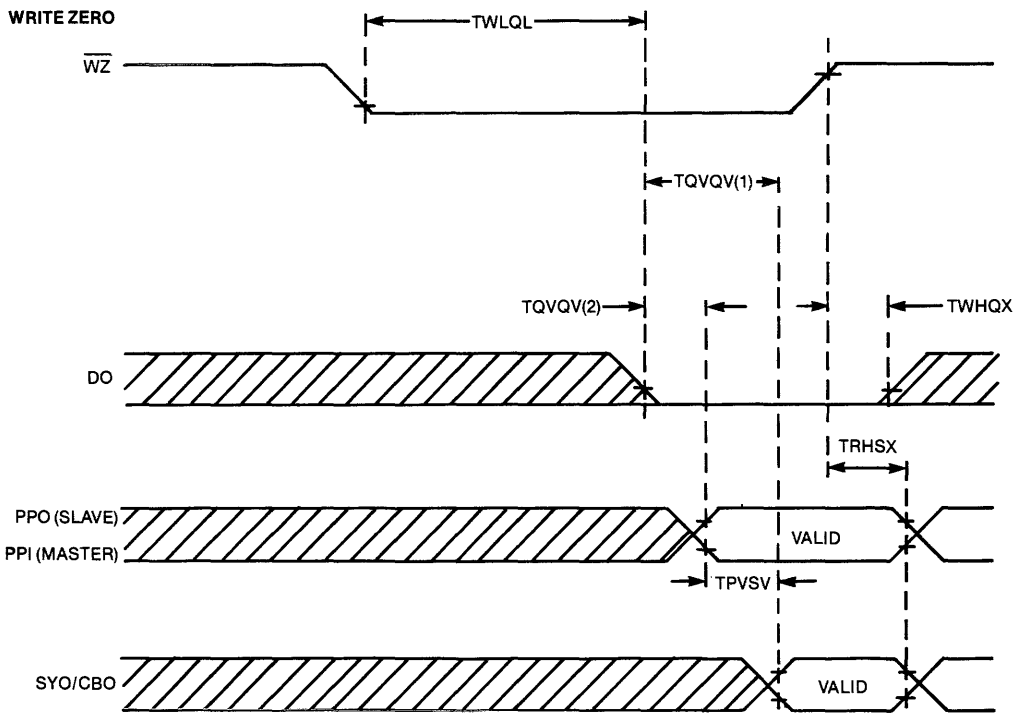


WAVEFORMS (Continued)

NON-CORRECTING READ



WRITE ZERO



NOTE:
(1): 16 BIT ONLY
(2): MASTER/SLAVE

See page 481 for ordering information.

Printed in U.S.A.

PRELIMINARY

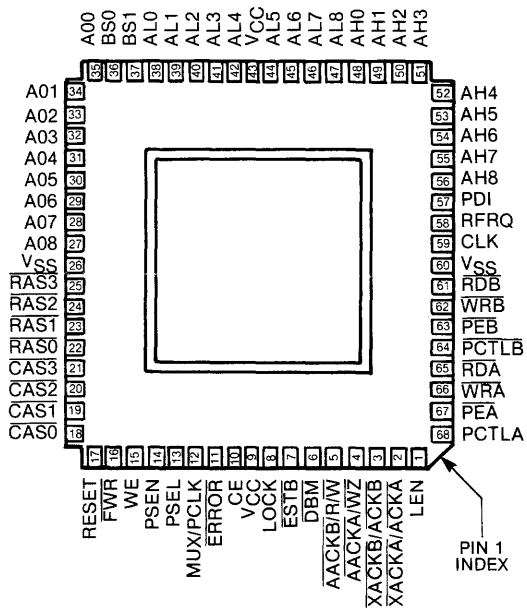
WD8207 Advance Dynamic RAM Controller

FEATURES

- PROVIDES ALL SIGNALS NECESSARY TO CONTROL 16K, 64K AND 256K DYNAMIC RAMS
- DIRECTLY ADDRESSES AND DRIVES UP TO 2 MEGABYTES WITHOUT EXTERNAL DRIVERS
- SUPPORTS SINGLE AND DUAL-PORT CONFIGURATIONS
- AUTOMATIC RAM INITIALIZATION IN ALL MODES
- FIVE PROGRAMMABLE REFRESH MODES
- TRANSPARENT MEMORY SCRUBBING IN ECC MODE
- DATA TRANSFER ACKNOWLEDGE SIGNALS FOR EACH PORT
- PROVIDES SIGNALS TO DIRECTLY CONTROL THE WD8206 ERROR DETECTION AND CORRECTION UNIT
- SUPPORTS SYNCHRONOUS OR ASYNCHRONOUS OPERATION ON EITHER PORT
- SINGLE +5V SUPPLY

DESCRIPTION

The WD8207 is a 68-pin leadless JEDEC type A hermetic chip carrier. The WD8207 Advanced Dynamic RAM Controller (ADRC) is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs microprocessor Systems. A dual-port interface allows two different busses to independently access memory. When configured with a WD8206 Error Detection and Correction Unit the WD8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.



PIN DESIGNATION

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
1	ADDRESS LATCH ENABLE	LEN	O	In two-port configurations, when port A is running with Status interface mode, this output replaces the ALE signal from the system bus controller and generates an address latch enable signal which provides optimum setup and hold timing for the WD8207.
2	TRANSFER ACKNOWLEDGE PORT A/ACKNOWLEDGE PORT A	$\overline{\text{XACK A}}$/ $\overline{\text{ACKA}}$	O	In non-ECC mode, this pin is $\overline{\text{XACKA}}$ and indicates that data on the bus is valid during a read cycle or that data may be removed from the bus during a write cycle for Port A. $\overline{\text{XACKA}}$ is a Multibus-compatible signal. In ECC mode, this pin is $\overline{\text{ACKA}}$ which can be configured, depending on the programming of the X program bit, as an XACK or AACK strobe. The SA programming bit determines whether AACK will be early or late.
3	TRANSFER ACKNOWLEDGE PORT B/ACKNOWLEDGE PORT B	$\overline{\text{XACKB}}$/ $\overline{\text{ACKB}}$	O	In non-ECC mode, this pin is $\overline{\text{XACKB}}$ and indicates that data on the bus is valid during a read cycle or that data may be removed from the bus during a write cycle for Port B. $\overline{\text{XACKB}}$ is a Multibus-compatible signal. In ECC mode, this pin is $\overline{\text{ACKB}}$ which can be configured, depending on the programming of the X program bit, as an XACK or AACK strobe. The SB programming bit determines whether AACK will be early or late.
4	ADVANCED ACKNOWLEDGE PORT A/WRITE ZERO	$\overline{\text{AACK A}}$/ WZ	O	In non-ECC mode, this pin is $\overline{\text{AACKA}}$ and indicates that the processor may continue processing and that data will be available when required. This signal is optimized for the system by programming the SA program bit for synchronous or asynchronous operation. After a RESET, this signal will cause the WD8206 to force the data to all zeros and generate the appropriate check bits.
5	ADVANCED ACKNOWLEDGE PORT B/READ/WRITE	$\overline{\text{AACKB}}$/ R/$\overline{\text{W}}$	O	In non-ECC mode, this pin is $\overline{\text{AACKB}}$ and indicates that the processor may continue processing and that data will be available when required. This signal is optimized for the system by programming the SB program bit for synchronous or asynchronous operation. This signal causes the WD8206 EDCU to latch the syndrome and error flags and generate check bits.
6	DISABLE BYTE MARKS	$\overline{\text{DBM}}$	O	This is an ECC control output signal indicating that a read or refresh cycle is occurring. This output forces the byte address decoding logic to enable all WD8206 data output buffers. In ECC mode, this output is also asserted during memory initialization and the 8-cycle dynamic RAM wake-up exercise. In non-ECC mode synchronous local bus systems this signal may be used as an early WE output.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
7	ERROR STROBE	$\overline{ESTB}$	O	In ECC mode, this strobe is activated when an error is detected and allows a negative-edge triggered flip-flop to latch the status of the WD8206 EDCU CE for systems with error logging capabilities.
8	LOCK	LOCK	I	This input instructs the WD8207 to lock out the port not being serviced at the time LOCK was issued.
9	LOGIC POWER	V_{CC}	I	+5 Volts ± 10%. Supplies V_{CC} for the internal logic circuits.
43	DRIVER POWER		I	+5 Volts ± 10%. Supplies V_{CC} for the output drivers.
10	CORRECTABLE ERROR	CE	I	This is an ECC input from the WD8206 EDCU which instructs the WD8207 whether a detected error is correctable or not. A high input indicates a correctable error. A low input inhibits the WD8207 from activating WE to write the data back into RAM. This should be connected to the CE output of the WD8206.
11	ERROR	$\overline{ERROR}$	I	This is an ECC input from the WD8206 EDCU and instructs the WD8207 that an error was detected. This pin should be connected to the ERROR output of the WD8206.
12	MULTIPLEXER CONTROL/ PROGRAMMING CLOCK	MUX/ PCLK	O	Immediately after a RESET this pin is used to clock serial programming data into the PDI pin. In normal two-port operation, this pin is used to select memory addresses from the appropriate port. When this signal is high, port A is selected and when it is low, port B is selected. This signal may change state before the completion of a RAM cycle, but the RAM address hold time is satisfied.
13	PORT SELECT	PSEL	O	This signal is used to select the appropriate port for data transfer.
14	PORT SELECT ENABLE	PSEN	O	This signal used in conjunction with PSEL provides contention-free port exchange. When PSEN is low, PSEL is allowed to change state.
15	WRITE ENABLE	WE	O	This signal provides the dynamic RAM array the write enable input for a write operation.
16	FULL WRITE	$\overline{FWR}$	I	This is an ECC input signal that instructs the WD8207, in an ECC configuration, whether the present write cycle is normal RAM write (full write) or a RAM partial write (read-modify-write) cycle.
17	RESET	RESET	I	This signal causes all internal counters and state flip-flops to be reset and upon release of RESET, data appearing at the PDI pin is clocked in by the PCLK output. The states of the PDI, PCTLA, PCTLB and RFRQ pins are sampled by RESET going inactive and are used to program the WD8207.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
18-21	COLUMN ADDRESS STROBE	$\overline{CAS0}$-$\overline{CAS3}$	O	These outputs are used by the dynamic RAM array to latch the column address, present on the AO0-8 pins. These outputs are selected by the BS0 and BS1 as programmed by program bits RB0 and RB1. These outputs drive the dynamic RAM array directly and need no external drivers.
22-25	ROW ADDRESS STROBE	$\overline{RAS0}$-$\overline{RAS3}$	O	These outputs are used by the dynamic RAM array to latch the row address, present on the AO0-8 pins. These outputs are selected by the BS0 and BS1 as programmed by program bits RB0 and RB1. These outputs drive the dynamic RAM array directly and need no external drivers.
26 60	DRIVER GROUND LOGIC GROUND	V_{SS}	I I	Provides a ground for the output drivers. Provides a ground for the remainder of the device.
35-27	ADDRESS OUTPUTS	AO0-AO8	O	These outputs are designed to provide the row and column addresses of the selected port to the dynamic RAM array. These outputs drive the dynamic RAM array directly and need no external drivers.
36, 37	BANK SELECT	BS0, BS1	I	These inputs are used to select one of four banks of the dynamic RAM array as defined by the program bits RB0 and RB1.
38-47	ADDRESS LOW	AL0-AL8	I	These lower-order address inputs are used to generate the row address for the internal address multiplexer.
48-56	ADDRESS HIGH	AH0-AH8	I	These higher-order address inputs are used to generate the column address for the internal address multiplexer.
57	PROGRAM DATA INPUT	PDI	I	This input programs the various user-selectable options in the WD8207. The PCLK pin shifts programming data into the PDI input from optional external shift registers. This pin may be strapped high or low to a default ECC (PCI = V_{CC}) or non-ECC (PDI = Ground) mode configuration.
58	REFRESH REQUEST	RFRQ	I	This input is sampled on the falling edge of RESET. If it is high at RESET, then the WD8207 is programmed for internal refresh request or external refresh request with failsafe protection. If it is low at RESET, then the WD8207 is programmed for external refresh without failsafe protection or burst refresh. Once programmed the RFRQ pin accepts signals to start an external refresh with failsafe protection or external refresh without failsafe protection or a burst refresh.
59	CLOCK	CLK	I	This input provides the basic timing for sequencing the internal logic.
61	READ FOR PORT B	$\overline{RDB}$	I	This pin is the read memory request command input for port B. This input also directly accepts the $\overline{S1}$ status line from processors.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
62	WRITE FOR PORT B	$\overline{WRB}$	I	This pin is the write memory request command input for port B. This input also directly accepts the $\overline{S0}$ status line from processors.
63	PORT ENABLE FOR PORT B	$\overline{PEB}$	I	This pin serves to enable a RAM cycle request for port B. It is generally decoded from the port address.
64	PORT CONTROL FOR PORT B	PCTLB	I	This pin is sampled on the falling edge of RESET. It configures port B to accept command inputs or processor status inputs. If low after RESET, the WD8207 is programmed to accept command, status inputs or Multibus commands. If high after RESET, the WD8207 is programmed to accept status inputs from compatible processors. The S2 status line should be connected to this input if programmed to accept specific status inputs. When programmed to accept commands it should be tied low or it may be used as a Multibus-compatible inhibit signal.
65	READ FOR PORT A	$\overline{RDA}$	I	This pin is the read memory request command input for port A. This input also directly accepts the $\overline{S1}$ status line from processors.
66	WRITE FOR PORT A	$\overline{WRA}$	I	This pin is the write memory request command input for port A. This input also directly accepts the $\overline{S0}$ status line from processors.
67	PORT ENABLE FOR PORT A	$\overline{PEA}$	I	This pin serves to enable a RAM cycle request for port A. It is generally decoded from the port address.
68	PORT CONTROL FOR PORT A	PCTLA	I	This pin is sampled on the falling edge of RESET. It configures port A to accept command inputs or processor status inputs. If low after RESET, the WD8207 is programmed to accept command inputs or Multibus commands. If high after RESET, the WD8207 is programmed to accept status inputs from processors. The $\overline{S2}$ status line should be connected to this input if programmed to accept status inputs. When programmed to accept commands or status, it should be tied low or it may be connected to INHIBIT when operating with Multibus.

GENERAL DESCRIPTION

The WD8207 Advanced Dynamic RAM Controller (ADRC) is a microcomputer peripheral device which provides the necessary signals to address, refresh and directly drive 16K, 64K and 256K dynamic RAMs. This controller also provides the necessary arbitration circuitry to support dual-port access of the dynamic RAM array.

The ADRC supports several microprocessor interface options including synchronous and asynchronous connection.

This device may be used with the WD8206 Error Detection and Correction Unit (EDCU). When used with the WD8206, the WD8207 is programmed in the Error Checking and Correction (ECC) mode. In this mode, the WD8207 provides all the necessary control signals for the WD8206 to perform memory initialization and transparent error scrubbing during refresh.

FUNCTIONAL DESCRIPTION

Processor Interface

The WD8207 has control circuitry for two ports each capable of supporting one of several possible bus structures. The ports are independently configurable allowing the dynamic RAM to serve as an interface between two different bus structures.

Each port of the WD8207 may be programmed to run synchronous or asynchronous to the processor clock. (See Synchronous/Asynchronous Mode) The WD8207 has been optimized to run synchronously with compatible microprocessors. When the WD8207 is programmed to run in asynchronous mode, the WD8207 inserts the necessary synchronization circuitry for the RD, WR, PE, and PCTL inputs.

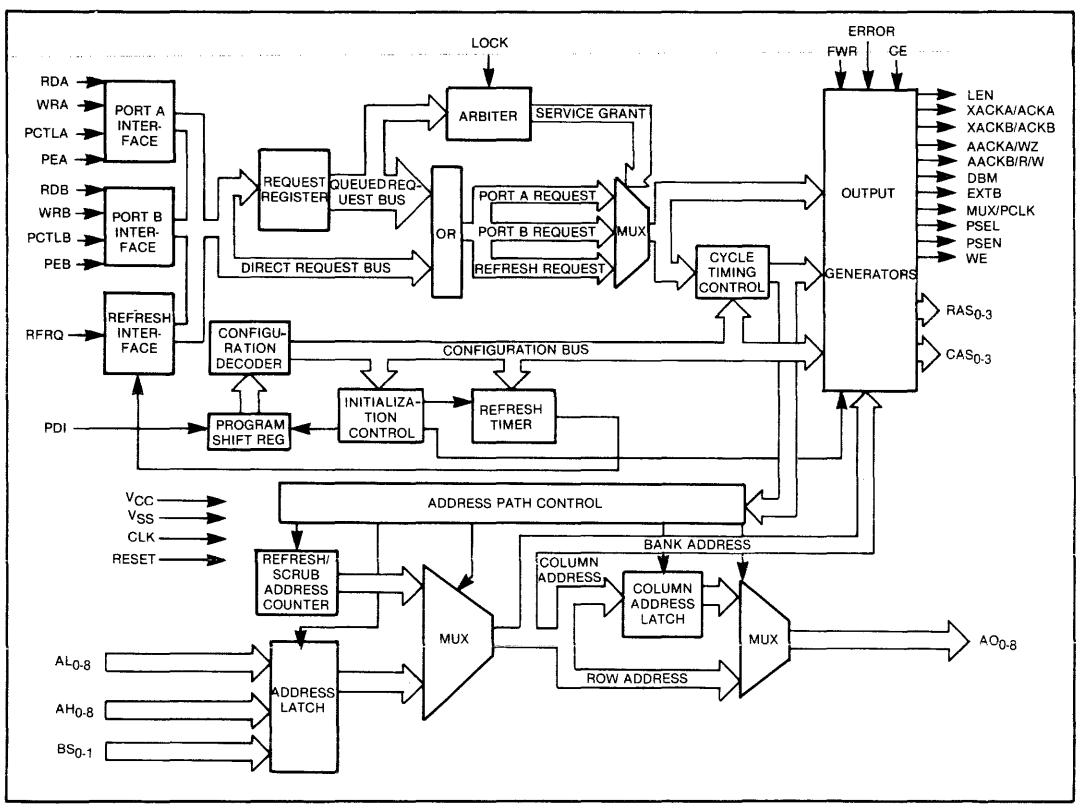
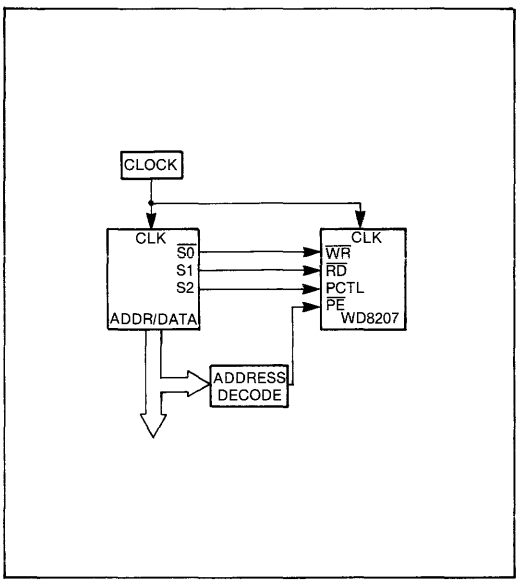


Figure 1. WD8207 BLOCK DIAGRAM

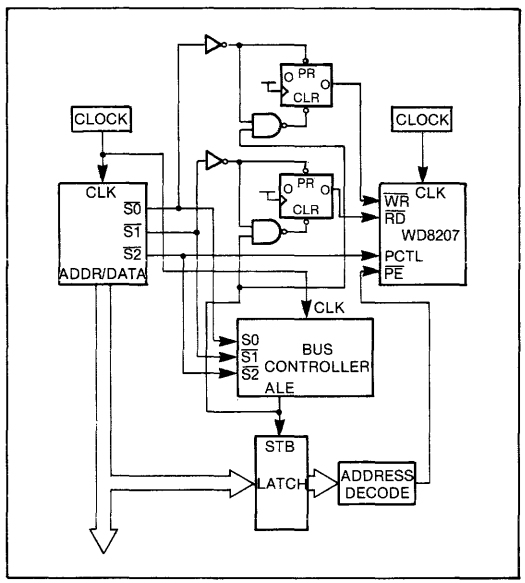
The WD8207 can also decode the status lines directly from various compatible microprocessors or can be programmed to receive read or write Multibus commands or commands from a bus controller. (See Status/Command Mode)

The WD8207 may be programmed to accept the clock of compatible microprocessors. The WD8207 adjusts its internal timing to allow for the different clock frequencies of these microprocessors. (See Microprocessor Clock Frequency Option)

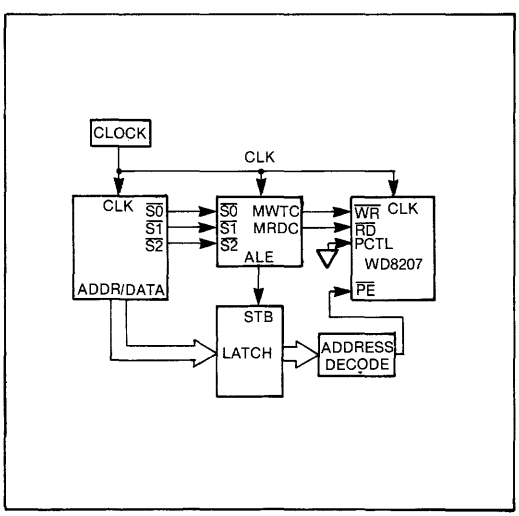
Figure 2 shows the different processor interfaces to the WD8207 using the synchronous or asynchronous mode and status or command interface.



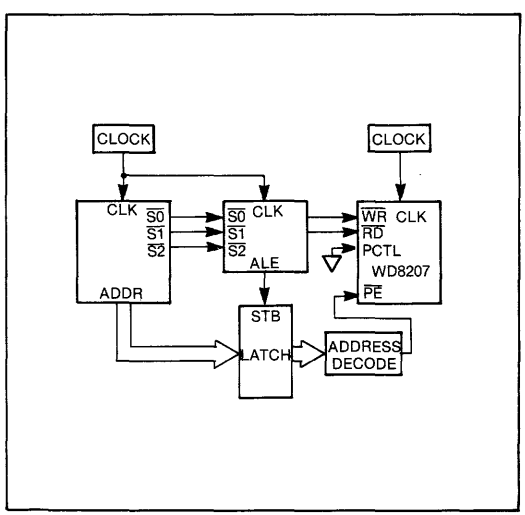
Slow-Cycle Synchronous-Status Interface



Slow-Cycle Asynchronous-Status Interface

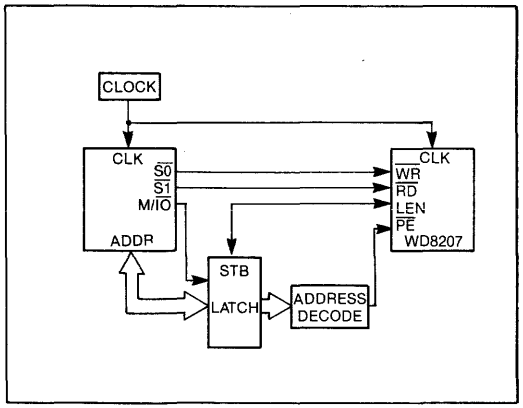


Slow-Cycle Synchronous-Command Interface

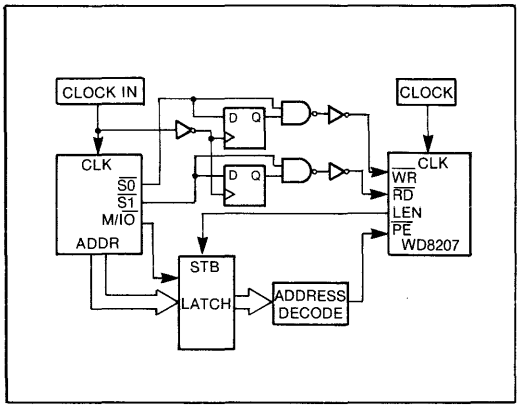


Slow-Cycle Asynchronous-Command Interface

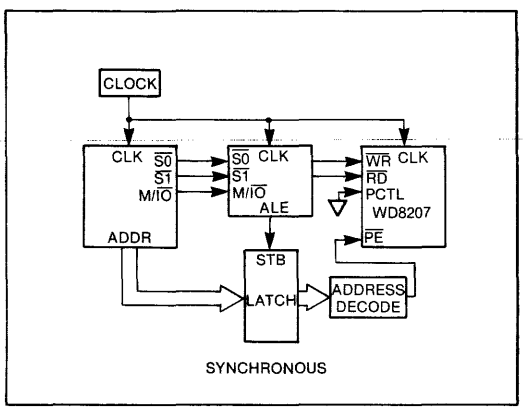
Figure 2A. SLOW-CYCLE PORT INTERFACES SUPPORTED BY THE WD8207



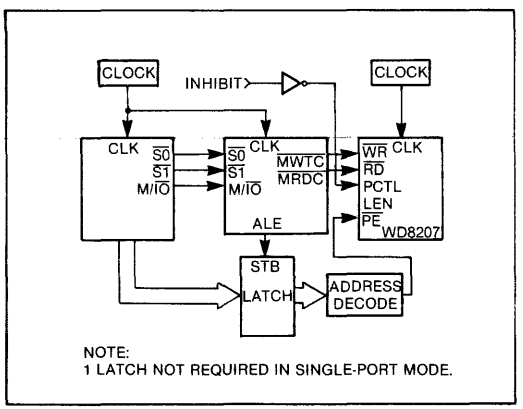
Fast-Cycle Synchronous-Status Interface



Fast-Cycle Asynchronous-Status Interface



Fast-Cycle Synchronous-Command Interface



Fast-Cycle Asynchronous-Command Interface

Figure 2B. FAST-CYCLE PORT INTERFACES SUPPORTED BY THE WD8207

Dual-Port Operation

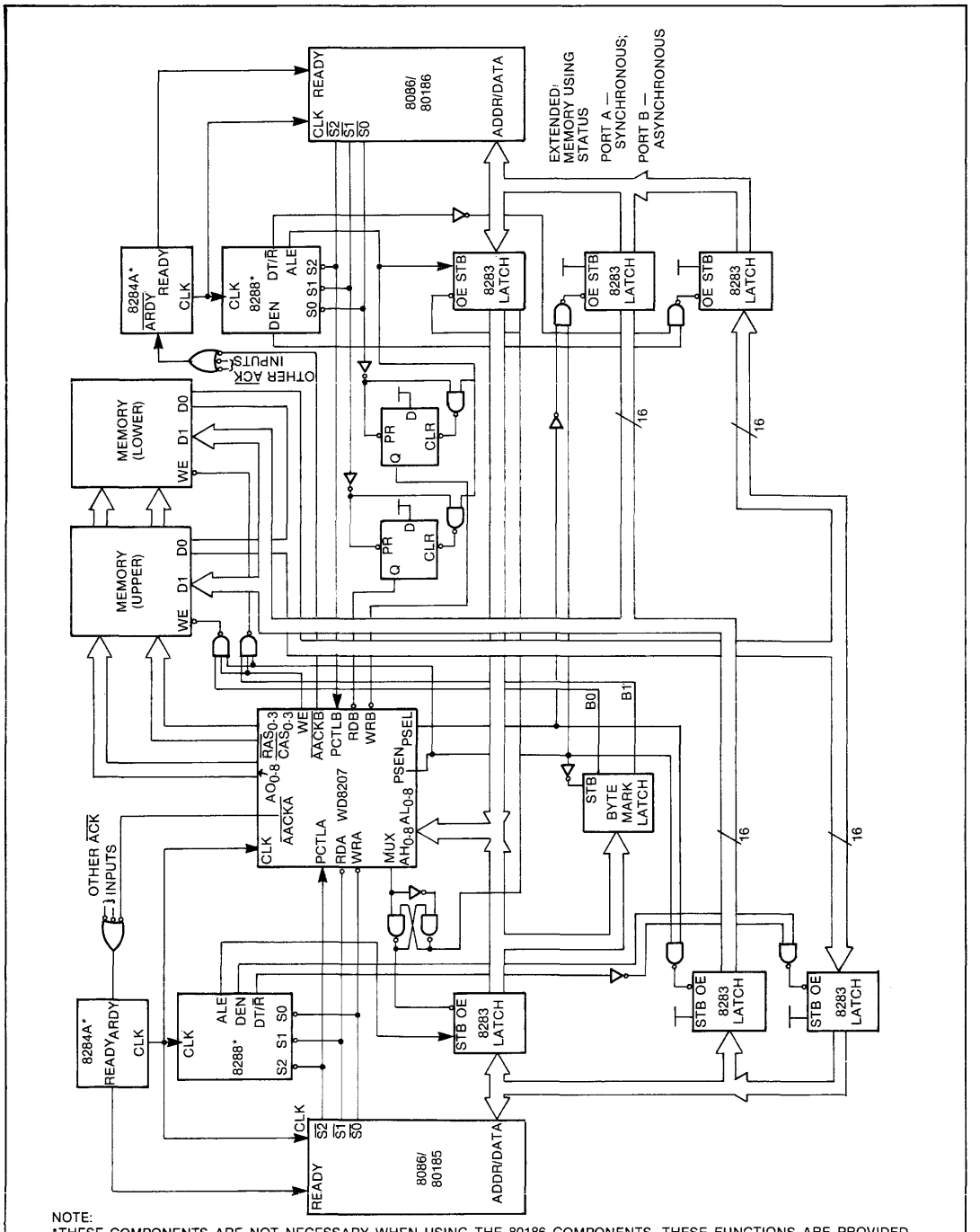
The WD8207 provides for two-port operation. Two independent processors may access memory controlled by the WD8207. The WD8207 arbitrates between each of the processor requests and directs data to or from the appropriate port. Selection is done on a priority concept that reassigns priorities based upon past history. Processor requests are internally queued.

Figure 3 shows a dual-port configuration with two systems interfacing to dynamic RAM. One of the processor systems is interfaced synchronously using the status interface and the other is interfaced asynchronously also using the status interface.

Dynamic RAM Interface

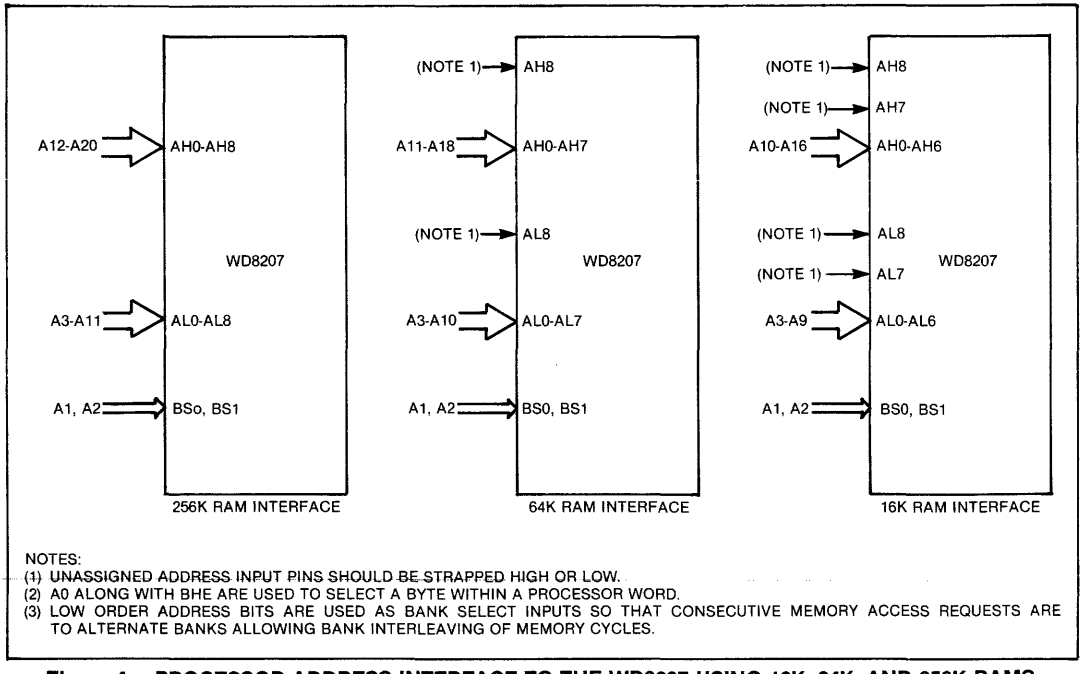
The WD8207 is capable of addressing 16K, 64K and 256K dynamic RAMs. Figure 4 shows the connection of the processor address bus to the WD8207 using the different RAMs. The WD8207 directly supports the 2118 RAM family or any RAM with similar timing requirements and responses including the 2164A RAM.

The WD8207 divides memory into four banks, each bank having its own Row ($\overline{RAS}$) and Column ($\overline{CAS}$) Address Strobe pair. This organization permits RAM cycle interleaving and permits error scrubbing during ECC refresh cycles. RAM cycle interleaving overlaps the start of the next RAM cycle with the RAM



NOTE:
*THESE COMPONENTS ARE NOT NECESSARY WHEN USING THE 80186 COMPONENTS. THESE FUNCTIONS ARE PROVIDED DIRECTLY BY THE 80186.

Figure 3. DUAL PORT SYSTEM



NOTES:
(1) UNASSIGNED ADDRESS INPUT PINS SHOULD BE STRAPPED HIGH OR LOW.
(2) A0 ALONG WITH BHE ARE USED TO SELECT A BYTE WITHIN A PROCESSOR WORD.
(3) LOW ORDER ADDRESS BITS ARE USED AS BANK SELECT INPUTS SO THAT CONSECUTIVE MEMORY ACCESS REQUESTS ARE TO ALTERNATE BANKS ALLOWING BANK INTERLEAVING OF MEMORY CYCLES.

Figure 4. PROCESSOR ADDRESS INTERFACE TO THE WD8207 USING 16K, 64K, AND 256K RAMS

Precharge period of the previous cycle. Hiding the precharge period of one RAM cycle behind the data access period of the next RAM cycle optimizes memory bandwidth and is effective as long as successive RAM cycles occur in alternate banks.

Successive data access to the same bank will cause the WD8207 to wait for the precharge time of the previous RAM cycle.

If not all RAM banks are occupied, the WD8207 reassigns the $\overline{RAS}$ and $\overline{CAS}$ strobes to allow using wider data words without increasing the loading on the $\overline{RAS}$ and $\overline{CAS}$ drivers. Table 2 shows the bank selection decoding and the word expansion, including $\overline{RAS}$ and $\overline{CAS}$ assignments. For example, if only two RAM banks are occupied, then two $\overline{RAS}$ and two $\overline{CAS}$ strobes are activated per bank.

The WD8207 can interface to fast or slow RAMs. The WD8207 adjusts and optimizes internal timings for either the fast or slow RAMs as programmed. (See RAM Speed Option)

Memory Initialization

After programming, the WD8207 performs eight RAM "warm-up" cycles to prepare the dynamic RAM for proper device operation and if configured for operation with error correction, the WD8207 and WD8206 EDCU will proceed to initialize all of memory (memory is written with zeros with corresponding check bits).

Table 2.
BANK SELECTION DECODING AND WORD EXPANSION

PROGRAM BITS		BANK INPUT		RAS/CAS
RB1	RB0	BS1	BS0	PAIR ALLOCATION
0	0	0	0	$RAS_{0\text{-}3}$, $CAS_{0\text{-}3}$ to Bank 0
0	0	0	1	Bank 1 unoccupied
0	0	1	0	Bank 2 unoccupied
0	0	1	1	Bank 3 unoccupied
0	1	0	0	$RAS_{0,1}$, $CAS_{0,1}$ to Bank 0
0	1	0	1	$RAS_{2,3}$, $CAS_{2,3}$ to Bank 1
0	1	1	0	Bank 2 unoccupied
0	1	1	1	Bank 3 unoccupied
1	0	0	0	RAS_0, CAS_0 to Bank 0
1	0	0	1	RAS_1, CAS_1 to Bank 1
1	0	1	0	RAS_2, CAS_2 to Bank 2
1	0	1	1	Bank 3 unoccupied
1	1	0	0	RAS_0, CAS_0 to Bank 0
1	1	0	1	RAS_1, CAS_1 to Bank 1
1	1	1	0	RAS_2, CAS_2 to Bank 2
1	1	1	1	RAS_3, CAS_3 to Bank 3

Because the time to initialize memory is fairly long, the WD8207 may be programmed to skip initialization in ECC mode. The time required to initialize all of memory is dependent on the clock cycle time to the WD8207 and can be calculated by the following equation:

Eq. 1 $T_{INIT} = (2^{23}) T_{CY}$

if T_{CY} = 125 ns then $T_{INIT} \approx 1$ sec.

WD8206 ECC Interface

For operation with Error Checking and Correction (ECC), the WD8207 adjusts its internal timing and changes some pin functions to optimize performance and provide a clean dual-port memory interface between the WD8206 EDCU and memory. The WD8207 directly supports a master-only (16-bit word plus 6 check bits) system. Under extended operation and reduced clock frequency, the WD8207 will support any ECC master-slave configuration up to 80 data bits, which is the maximum set by the WD8206 EDCU. (See Extend Option)

Correctable errors detected during memory read cycles are corrected immediately and then written back into memory.

In a synchronous bus environment, ECC system perfomance has been optimized to enhance processor throughput, while in an asynchronous bus environment (the Multibus), ECC performance has been optimized to get valid data onto the bus as quickly as possible. Performance optimization, processor throughput or quick data access may be selected via the Transfer Acknowledge Option.

The main difference between the two ECC implementations is that, when optimized for processor throughput, RAM data is always corrected and an advanced transfer acknowledge is issued at a point when, by knowing the processor characteristics, data is guaranteed to be valid by the time the processor needs it.

When optimized for quick data access, (valid for Multibus) the WD8206 is configured in the uncorrecting mode where the delay associated with error correction circuitry is transparent, and a transfer acknowledge is issued as soon as valid data is known to exist. If the $\overline{\text{ERROR}}$ flag is activated, then the transfer acknowledge is delayed until after the WD8207 has instructed the WD8206 to correct the data and the corrected data becomes available on the bus. Figure 5 illustrates a dual-port ECC system.

Figure 6 illustrates the interface required to drive the $\overline{\text{CRCT}}$ pin of the WD8206, in the case that one port (PORT A) receives an advanced acknowledge (not Multibus-compatible), while the other port (PORT B) receives $\overline{\text{XACK}}$ (which is Multibus-compatible).

Error Scrubbing

The WD8207/8206 performs error correction during refresh cycles (error scrubbing). Since the WD8207 must refresh RAM, performing error scrubbing during refresh allows it to be accomplished without additional performance penalties.

Upon detection of a correctable error during refresh, the RAM refresh cycle is lengthened slightly to permit the WD8206 to correct the error and for the corrected word to be rewritten into memory. Uncorrectable errors detected during scrubbing are ignored.

Refresh

The WD8207 provides an internal refresh interval counter and a refresh address counter to allow the WD8207 to refresh memory. The WD8207 will refresh 128 rows every 2 milliseconds or 256 rows every 4 milliseconds, which allows all RAM refresh options to be supported. In addition, there exists the ability to refresh 256 row address locations every 2 milliseconds via the Refresh Period programming option.

The WD8207 may be programmed for any of five different refresh options: Internal refresh only, External refresh with failsafe protection, External refresh without failsafe protection, Burst Refresh mode, or no refresh. (See Refresh Options)

It is possible to decrease the refresh time interval by 10%, 20% or 30%. This option allows the WD8207 to compensate for reduced clock frequencies. Note that an additional 5% interval shortening is built-in in all refresh interval options to compensate for clock variations and non-immediate response to the internally generated refresh request. (See Refresh Period Options)

External Refresh Requests after RESET

External refresh requests are not recognized by the WD8207 until after it is finished programming and preparing memory for access. Memory preparation includes 8 RAM cycles to prepare and ensure proper dynamic RAM operation, and memory initialization if error correction is used. Many dynamic RAMs require this warm-up period for proper operation. The time it takes for the WD8207 to recognize a request is shown below.

Eq. 2 Non-ECC Systems: $T_{RESP} = T_{PROG} + T_{PREP}$

Eq. 3 where: T_{PROG} = (66) (T_{CY}) which is programming time

Eq. 4 T_{PREP} = (8) (32) (T_{CY}) which is the RAM warm-up time

if T_{CY} = 125 ns then $T_{RESP} \approx 41$ us

Eq. 5 ECC Systems: $T_{RESP} = T_{PROG} + T_{PREP} + T_{INIT}$

if T_{CY} = 125 ns then $T_{RESP} \approx 1$ sec

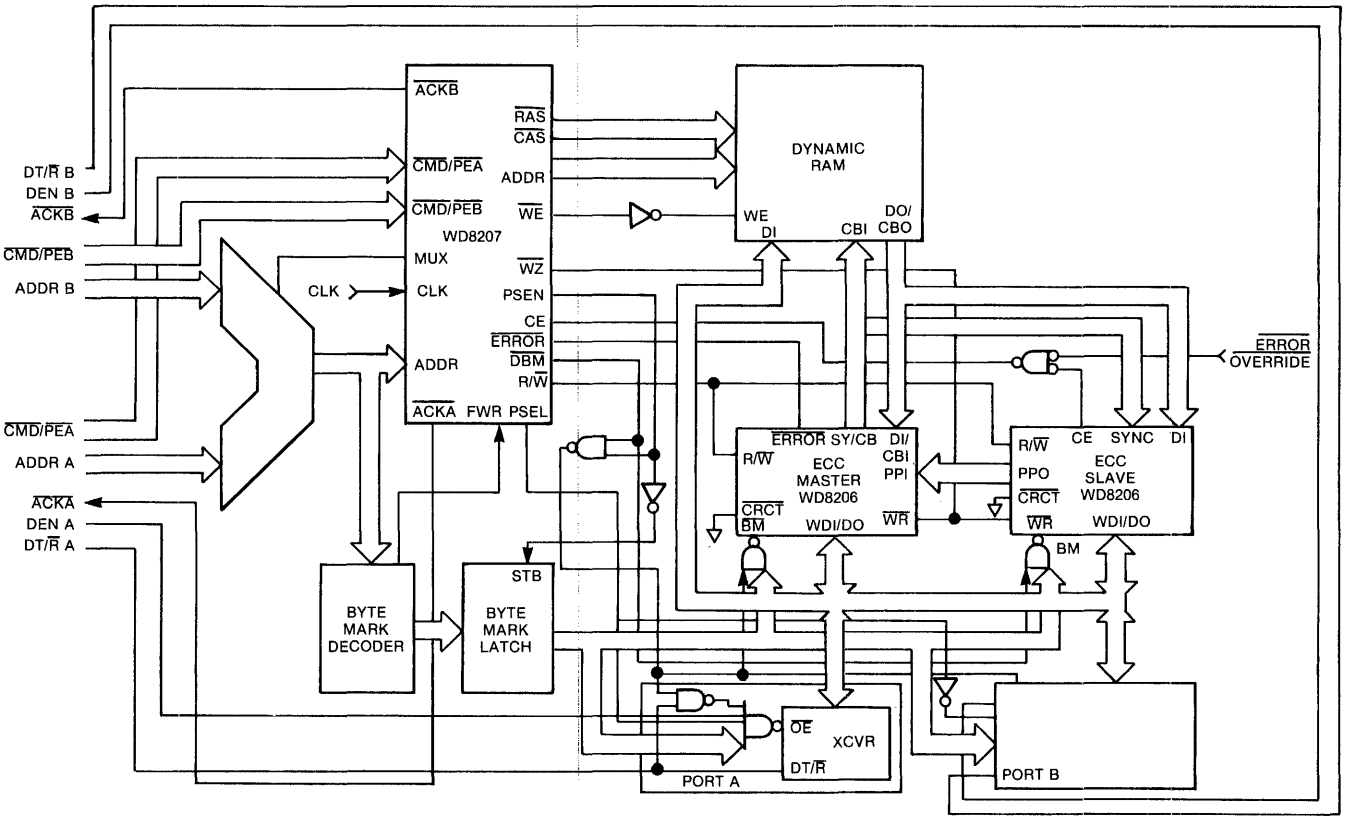


Figure 5. TWO-PORT ECC IMPLEMENTATION USING THE WD8207 AND THE WD8206

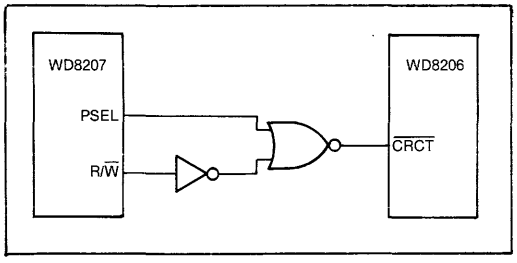


Figure 6.
INTERFACE TO WD8206 CRCT INPUT WHEN PORT A RECEIVES AACK AND PORT B RECEIVES XACK

RESET

RESET is an asynchronous input, the falling edge of which is used by the 20 to directly sample the logic levels of the PCTLA, PCTLB, RFRQ, and PDI inputs. The internally synchronized falling edge of RESET is used to begin programming operations (shifting in the contents of the external shift register into the PDI input).

Until programming is complete the WD8207 registers but does not respond to command or status inputs. A simple means of preventing commands or status from occurring during this period is to differentiate the system reset pulse to obtain a smaller reset pulse for the WD8207. The total time of the reset pulse and the WD8207 programming time must be less than the time before the first command in systems that alter the default port synchronization programming bits (default is Port A synchronous, Port B asynchronous). Differentiated reset is unnecessary when the default port synchronization programming is used.

The differentiated reset pulse would be shorter than the system reset pulse by at least the programming period required by the WD8207. The differentiated reset pulse first resets the WD8207, and system reset would reset the rest of the system. While the rest of the system is still in reset, the WD8207 completes its programming. Figure 7 illustrates a circuit to accomplish this task.

Within four clocks after RESET goes active, all the WD8207 outputs will go high, except for PSEN, WE, and AO0-8, which will go low.

OPERATIONAL DESCRITION

Programming the WD8207

The WD8207 is programmed after reset. On the falling edge of RESET, the logic states of several input pins are latched internally. The falling edge of RESET actually performs the latching, which means that the logic levels on these inputs must be stable prior to that time. The inputs whose logic levels are latched at the end of reset are the PCTLA, PCTLB, REFRQ, and PDI pins. Figure 8 shows the necessary timing for programming the WD8207.

Refresh Options

Immediately after system reset, the state of the REFRQ input pin is examined. If REFRQ is high, the WD8207 provides the user with the choice between self-refresh or user-generated refresh with failsafe protection. Failsafe protection guarantees that if the user does not come back with another refresh request before the internal refresh interval counter times out, a refresh request will be automatically generated. If the REFRQ pin is low immediately after a reset, then the user has the choice of a single external refresh cycle without failsafe, burst refresh or no refresh.

Internal Refresh Only

For the WD8207 to generate internal refresh requests, it is necessary only to strap the REFRQ input pin high.

External Refresh with Failsafe

To allow user-generated refresh requests with failsafe protection, it is necessary to hold the REFRQ input high until after reset. Thereafter, a low-to-high transition on this input causes a refresh request to be generated and the internal refresh interval counter to be reset. A high-to-low transition has no effect on the WD8207. A refresh request is not reconized until a previous request has been serviced.

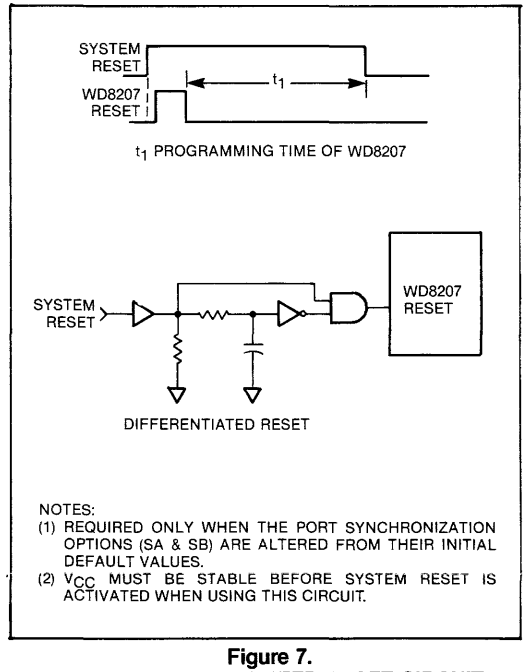


Figure 7.
WD8207 DIFFERENTIATED RESET CIRCUIT

External Refresh without Failsafe

To generate single external refresh requests without failsafe protection, it is necessary to hold REFRQ low until after reset. Thereafter, bringing REFRQ high for one clock period causes a refresh request to be generated. A refresh request is not recognized until a previous request has been serviced.

Burst Refresh

Burst refresh is implemented through the same procedure as a single external refresh without failsafe (i.e., REFRQ is kept low until after reset). Thereafter, bringing REFRQ high for at least two clock periods causes a burst of 128 row address locations to be refreshed.

In ECC-configured systems, 128 locations are scrubbed. A burst refresh request is not recognized until a previous request has been serviced.

No Refresh

It is necessary to hold REFRQ low until after reset. This is the same as programming External Refresh without Failsafe. No refresh is accomplished by keeping REFRQ low.

Option Program Data Word

The program data word consists of 16 program data bits, PD0-PD15. If the first program data bit PD0 is set to logic 1, the WD8207 is configured to support ECC. If it is logic 0, the WD8207 is configured to support a non-ECC system. The remaining bits, PD1-PD15, may then be programmed to optimize a selected configuration. Figures 8 and 9 show the Program word for non-ECC and ECC operation.

Using an External Shift Register

The WD8207 may be configured to use an external shift register with asynchronous load capability such as a 74LS165. The reset pulse serves to parallel load the shift register and the WD8207 supplies the clocking signal to shift the data in. Figure 10 shows a sample circuit diagram of an external shift register circuit. Serial data is shifted into the WD8207 via the PDI pin (57), and clock is provided by the MUX/PCLK pin (12), which generates a total of 16 clock pulses. After programming is complete, data appearing at the input of the PDI pin is ignored. MUX/PCLK is a dual-function pin. during programming, it serves to clock the external shift register, and after programming is completed, it reverts to a MUX control pin. As the pin changes state to select different port addresses, it continues to clock the shift register. This does not present a problem because data at the PDI pin is ignored after programming.

ECC Mode (ECC Program Bit)

The state of PDI (Program Data In) pin at reset determines whether the system is an ECC or non-ECC configuration. It is used internally by the WD8207 to begin configuring timing circuits, even before programming is completely finished. The WD8207 then begins programming the rest of the options.

Default Programming Options

After reset, the WD8207 serially shifts in a program data word via the PDI pin. This pin may be strapped either high or low, or connected to an external shift register. Strapping PDI high causes the WD8207 to default to a particular system configuration with error correction, and strapping it low causes the WD8207 to default to a particular system configuration without error correction. Table 4 shows the default configurations.

If further system flexibility is needed, one or two external shift registers can be used to tailor the WD8207 to its operating environment.

Synchronous/Asynchronous Mode (SA and SB Program Bits)

Each port of the WD8207 may be independently configured to accept synchronous or asynchronous port commands (RD, WR, PCTL) and Port Enable (PE) via the program bits SA and SB. The state of the SA and SB programming bits determine whether their associated ports are synchronous or asynchronous.

While a port may be configured with either the Status or Command interface in the synchronous mode, certain restrictions exist in the asynchronous mode. An asynchronous Command interface using the control lines of the Multibus is supported, and an asynchronous WD8086 interface using the control lines of the WD8086 is supported, with the use of TTL gates as illustrated in Figure 2. In the WD8086 case, the TTL gates are needed to guarantee that status does not appear at the WD8207 inputs too much before address, so that a cycle would start before address was valid.

Microprocessor Clock Frequency Option (CFS and FFS Program Bits)

The WD8207 can be programmed to interface with slow-cycle microprocessors or fast-cycle microprocessors. The CFS bit configures the microprocessor interface to accept slow or fast cycle signals from either microprocessor group.

This option is used to select the speed of the microprocessor clock. Table 5 shows the various microprocessor clock frequency options that can be programmed.

The external clock frequency must be programmed so that the failsafe refresh repetition circuitry can adjust its internal timing accordingly to produce a refresh request as programmed.

RAM Speed Option (RFS Program Bit)

The RAM Speed programming option determines whether RAM timing will be optimized for a fast or

PD15							PD8 PD7								PD0
0	0	TM1	$\overline{PPR}$	$\overline{FFS}$	EXT	$\overline{PLS}$	CI0	CI2	$\overline{RB1}$	$\overline{RB0}$	$\overline{RFS}$	$\overline{CFS}$	SB	$\overline{SA}$	0

PROGRAM DATA BIT	NAME	POLARITY/FUNCTION	
PD0	ECC	ECC = 0	For non-ECC mode
PD1	$\overline{SA}$	$\overline{SA}$ = 0 $\overline{SA}$ = 1	Port A is synchronous Port A is asynchronous
PD2	SB	SB = 0 SB = 1	Port B is asynchronous Port B is synchronous
PD3	$\overline{CFS}$	$\overline{CFS}$ = 0 $\overline{CFS}$ = 1	Fast-cycle IAPX 286 mode Slow-cycle IAPX 86 mode
PD4	$\overline{RFS}$	$\overline{RFS}$ = 0 $\overline{RFS}$ = 1	Fast RAM Slow RAM
PD5 PD6	$\overline{RB0}$ $\overline{RB1}$	RAM bank occupancy See Table 2	
PD7	CI1	Count interval bit 1; see Table 6	
PD8	CI0	Count interval bit 0; see Table 6	
PD9	$\overline{PLS}$	$\overline{PLS}$ = 0 $\overline{PLS}$ = 1	Long refresh period Short refresh period
PD10	EMT EXT	EXT = 0 gext71	Not extended Extended
PD11	$\overline{FFS}$	$\overline{FFS}$ = 0 $\overline{FFS}$ = 1	Fast CPU frequency Slow CPU frequency
PD12	$\overline{PPR}$	$\overline{PPR}$ = 0 $\overline{PPR}$ = 1	Most recently used port priority Port A preferred priority
PD13	TM1	TM1 = 0 TM1 = 1	Test mode 1 off Test mode 1 enabled
PD14	0	Reserved must be zero	
PD15	0	Reserved must be zero	

Figure 8. NON-ECC MODE PROGRAM DATA WORD

slow RAM. Whether a RAM is fast or slow is measured relative to the 2118-10 (Fast) or the 2118-15 (Slow) RAM specifications.

Refresh Period Options (CI0, CI1, and PLS Program Bits)

The WD8207 refreshes with either 128 rows every 2 milliseconds or 256 rows every 4 milliseconds. This translates to one refresh cycle being executed approximately once every 15.6 microseconds. This rate can be changed to 256 rows every 2 milliseconds or a refresh approximately once every 7.8 microseconds via the Period Long/Short, program bit PLS, programming option. The 7.8 microsecond refresh request rate is intended for those RAMs, 64K and above, which may require a faster refresh rate.

In addition to PLS program option, two other programming bits for refresh exist: Count Interval 0 (CI0) and Count Interval 1 (CI1). These two programming bits allow the rate at which refresh requests are generated to be increased in order to permit refresh requests to be generated close to the same 15.6 or 7.8 microsecond period when the WD8207 is operating at reduced frequencies. The interval between refreshes is decreased by 0%, 10%, 20%, or 30% as a function of how the count interval bits are programmed. A 5% guardband is built-in to allow for any clock frequency variations. Table 6 shows the refresh period options available.

The numbers tabulated under Count Interval represent the number of clock periods between internal refresh requests. The percentages in parentheses represent the decrease in interval between refresh requests. Note that all intervals have a built-in 5% (approximately) safety factor to compensate for minor clock frequency deviations and non-immediate response to internal refresh requests.

PD15							PD8 PD7								PD0
$\overline{TM2}$	RB1	RB0	PPR	FFS	$\overline{EXT}$	PLS	$\overline{CI0}$	$\overline{CI1}$	XB	$\overline{XA}$	RFS	CFS	$\overline{SB}$	SA	1

PROGRAM DATA BIT	NAME	POLARITY/FUNCTION
PD0	ECC	ECC = 1 ECC mode
PD1	SA	SA = 0 Port A is asynchronous SA = 1 Port A is synchronous
PD2	$\overline{SB}$	$\overline{SB}$ = 0 Port B is synchronous $\overline{SB}$ = 1 Port B is asynchronous
PD3	CFS	CFS = 0 Slow-cycle IAPX 86 mode CFS = 1 Fast-cycle IAPX 286 mode
PD4	RFS	RFS = 0 Slow RAM RFS = 1 Fast RAM
PD5	$\overline{XA}$	$\overline{XA}$ = 0 Multibus-compatible ACKA $\overline{XA}$ = 1 Advanced ACKA not multibus-compatible
PD6	XB	XB = 0 Advanced ACKB not multibus compatible XB = 1 Multibus-compatible ACKB
PD7	$\overline{CI1}$	Count interval bit 1; see Table 6
PD8	$\overline{CI0}$	Count interval bit 0; see Table 6
PD9	PLS	PLS = 0 Short refresh period PLS = 1 Long refresh period
PD10	$\overline{EXT}$	$\overline{EXT}$ = 0 Master and slave EDCU $\overline{EXT}$ = 1 Master EDCU only
PD11	FFS	FFS = 0 Slow CPU frequency FFS = 1 Fast CPU frequency
PD12	PPR	PPR = 0 Port A preferred priority PPR = 1 Most recently used port priority
PD13	RB0	RAM bank occupancy
PD14	RB1	See Table 2
PD15	$\overline{TM2}$	$\overline{TM2}$ = 0 Test mode 2 enabled $\overline{TM2}$ = 1 Test mode 2 off

Figure 9. ECC MODE PROGRAM DATA WORD

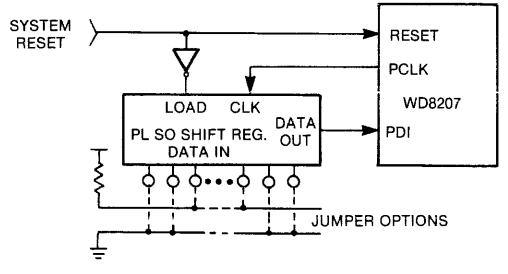


Figure 10.
EXTERNAL SHIFT REGISTER INTERFACE

Table 4A.
DEFAULT NON-ECC PROGRAMMING, PDI PIN (57) TIED TO GROUND

Port A is Synchronous
Port B is Asynchronous
Fast-cycle Processor Interface
Fast RAM
Refresh Interval uses 236 clocks
128 Row refresh in 2 ms; 256 Row refresh in 4 ms
Fast Processor Clock Frequency (16 MHz)
"Most Recently Used" Priority Scheme
4 RAM banks occupied

Table 4B.
DEFAULT NON-ECC PROGRAMMING, PDI PIN (57) TIED TO V_{CC}

Port A is Synchronous
Port B is Asynchronous
Fast-cycle Processor Interface
Fast RAM
Port A has Advanced ACKA strobe (non-multibus)
Port B has Non-advance ACKB strobe (multibus)
Refresh Interval uses 236 clocks
128 Row refresh in 2 ms; 256 Row refresh in 4 ms
Master EDCU only (16-bit system)
Fast Processor Clock Frequency (16 MHz)
"Most Recently Used" Priority Scheme
4 RAM banks occupied

Table 5.
MICROPROCESSOR CLOCK FREQUENCY OPTIONS

PROGRAM BITS			
CFS	FFS	PROCESSOR	CLOCK FREQUENCY
0	0	Slow Cycle	5 MHz
0	1	Slow Cycle	8 MHz
1	0	Fast Cycle	10 MHz
1	1	Fast Cycle	16 MHz

Extend Option (EXT Program Bit)

The Extend option lengthens the memory cycle to allow longer access time which may be required by the system. Extend alters the RAM timing to compensate for increased loading on the Row and Column Address Strobes, and in the multiplexed Address Out lines.

Port Priority Option and Arbitration (PPR Program Bit)

The WD8207 has to internally arbitrate among three ports: Port A, Port B and Port C — the refresh port. Port C is an internal port dedicated to servicing refresh requests, whether they are generated internally by the refresh interval counter, or externally by the user. Two arbitration approaches are available via the Port Priority programming option, program bit PPR. PPR determines whether the most recently used port will remain selected (PPR = 1) or whether Port A will be favored or preferred over Port B (PPR = 0).

A port is selected if the arbiter has given the selected port direct access to the timing generators. The front-end logic, which includes the arbiter, is designed to operate in parallel with the selected port. Thus a request on the selected port is serviced immediately. In contrast, an unselected port only has access to the timing generators through the front- end logic. Before a RAM cycle can start for an unselected port, that port must first become selected (i.e., the MUX output now gates that port's address into the WD8207 in the case of Port A or B). Also, in order to allow its address to stabilize, a newly selected port's first RAM cycle is started by the front- end logic. Therefore, the selected port has direct access to the timing generators. What all this means is that a request on a selected port is started immediately, while a request on an unselected port is started two to three clock periods after the request, assuming that the other two ports are idle. Under normal operating conditions, this arbitration time is hidden behind the RAM cycle of the selected port so that as soon as the present cycle is over a new cycle is started. Table 7 lists the arbitration rules for both options.

Port LOCK Function

The LOCK function provides each port with the ability to obtain uninterrupted access to a critical region of memory and, thereby, to guarantee that the opposite port cannot "sneak in" and read from or write to the critical region prematurely.

Only one LOCK pin is present and is multiplexed between the two ports as follows: when MUX is high, the WD8207 treats the LOCK input as originating at PORT A, while when MUX is low, the WD8207 treats LOCK as originating at PORT B. When the WD8207 recognizes a LOCK, the MUX output will remain pointed to the locking port until LOCK is deactivated. Refresh is not affected by LOCK and can occur during a locked memory cycle.

Table 6. REFRESH COUNT INTERVAL TABLE

FREQ. (MHz)	REF. PERIOD (μS)	CFS	PLS	FFS	COUNT INTERVAL CI1, CI0 (WD8207 CLOCK PERIODS)			
					00 (0%)	01 (10%)	10 (20%)	11 (30%)
16	15.6	1	1	1	236	212	188	164
	7.8	1	0	1	118	106	94	82
10	15.6	1	1	0	148	132	116	100
	7.8	1	0	0	74	66	58	50
8	15.6	0	1	1	118	106	94	82
	7.8	0	0	1	59	53	47	41
5	15.6	0	1	0	74	66	58	50
	7.8	0	0	0	37	33	29	25

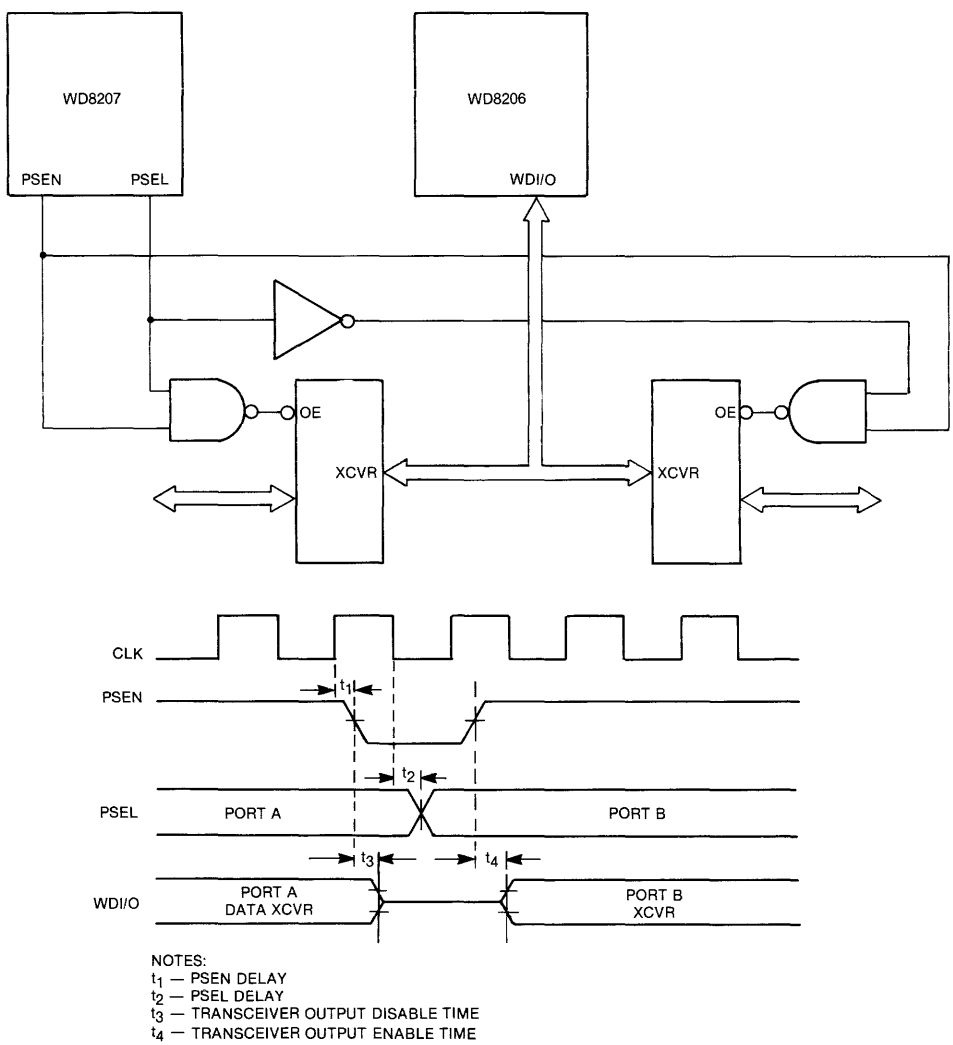
Table 7.
THE ARBITRATION RULES FOR THE MOST RECENTLY USED PORT PRIORITY AND FOR PORT A PRIORITY OPTIONS

1.	If only one port requests service, then that port — if not already selected — becomes selected.
2a.	When no service requests are pending, the last selected processor port (Port A or B) will remain selected. (Most Recently Used Port Priority Option)
2b.	When no service requests are pending, Port A is selected whether it requests service or not. (Port A Priority Option)
3.	During reset initialization only Port C, the refresh port, is selected.
4.	If no processor requests are pending after reset initialization, Port A will be selected.
5a.	If Ports A and B simultaneously(*) request service while Port C is being serviced, then the next port to be selected is the one which was not selected prior to servicing Port C. (Most Recently Used Port Priority Option)
5b.	If Ports A and B simultaneously(*) request service while Port C is selected, then the next port to be selected is Port A. (Port A Priority Option)
6.	If a port simultaneously requests service with the currently selected port, service is granted to the selected port.
7.	The MUX output remains in its last state whenever Port C is selected.
8.	If Port C and either Port A or Port B (or both) simultaneously request service, then service is granted to the requester whose port is already selected. If the selected port is not requesting service, then service is granted to Port C.
9.	If during the servicing of one port, the other port requests service before or simultaneously with the refresh port, the refresh port is selected. A new port is not selected before the presently selected port is deactivated.
10.	Activating LOCK will mask off service requests from Port B if the MUX output is high, or from Port A if the MUX output is low.
*By "simultaneous" it is meant that two or more requests are valid at the clock edge at which the internal arbiter samples them.	

Dual-Port Considerations

For both ports to be operated synchronously, several conditions must be met. The processors must be the same type (Fast or Slow Cycle) as defined by Table 8 and they must have synchronized clocks. Also when processor types are mixed, even though the clocks may be in phase, one frequency may be twice that of the other. So to run both ports synchronous using the status interface, the processors must have related timings (both phase and frequency). If these conditions cannot be met, then one port must run synchronous and the other asynchronous.

Figure 3 illustrates an example of dual-port operation using the processors in the slow cycle group. Note the use of cross-coupled NAND gates at the MUX output for minimizing contention between the two latches, and the use of flip flops on the status lines of the synchronous processor for delaying the status and thereby guaranteeing RAS will not be issued, even in the worst case, until address is valid. Figure 11 shows the timing associated with Port switching.



NOTES:
t_1 — PSEN DELAY
t_2 — PSEL DELAY
t_3 — TRANSCEIVER OUTPUT DISABLE TIME
t_4 — TRANSCEIVER OUTPUT ENABLE TIME

Figure 11.

Table 8. PROCESSOR INTERFACE/ACKNOWLEDGE SUMMARY

CYCLE	REQUEST TYPE	SYNC/ASYNC INTERFACE	ACKNOWLEDGE TYPE
Fast Cycle CFS = 1	Status	SYNC	$\overline{EAACK}$
	Status	ASYNC	$\overline{LAACK}$
	Command	SYNC	$\overline{EAACK}$
	Command	ASYNC	$\overline{LAACK}$
	Status	ASYNC	$\overline{LAACK}$
	Command	ASYNC	$\overline{LAACK}$
	Command	ASYNC	$\overline{XACK}$
Slow Cycle CFS = 0	Status	SYNC	$\overline{EAACK}$
	Status	ASYNC	$\overline{LAACK}$
	Command	SYNC	$\overline{EAACK}$
	Command	ASYNC	$\overline{LAACK}$
	Command	ASYNC	$\overline{XACK}$

Table 9. MEMORY ACKNOWLEDGE OPTION SUMMARY

	SYNCHRONOUS	ASYNCHRONOUS	XACK
Fast Cycle	AACK Optimized	AACK Optimized	Multibus Compatible
Slow Cycle	AACK Optimized	AACK Optimized	Multibus Compatible

Test Modes

Two special test modes exist in the WD8207 to facilitate testing. Test Mode 1 (non-ECC mode) splits the refresh address counter into two separate counters and Test Mode 2 (ECC mode) presets the refresh address counter to a value slightly less than rollover.

Test Mode 1 splits the address counter into two, and increments both counters simultaneously with each refresh address update. By generating external refresh requests, the tester is able to check for proper operation of both counters. Once proper individual counter operation has been established, the WD8207 must be returned to normal mode and a second test performed to check that the carry from the first counter increments the second counter. The outputs of the counters are presented-on the address out bus with the same timing as the row and column addresses of a normal scrubbing operation. During Test Mode 1, memory initialization is inhibited, since the WD8207, by definition, is in non-ECC mode.

Test Mode 2 sets the internal refresh counter to a value slightly less than rollover. During functional testing other than that covered in Test Mode 1, the WD8207 will normally be set in Test Mode 2. Test Mode 2 eliminates memory initialization in ECC mode. This allows quick examination of the circuitry which brings the WD8207 out of memory initialization and into normal operation. Test Mode 2 is also useful for quick reset response in ECC systems.

General System Considerations

The RAS_{0-3}, CAS_{0-3}, AO_{0-8}, output buffers were designed to directly drive the heavy capacitive loads associated with dynamic RAM arrays. To keep the RAM driver outputs from ringing excessively in the system environment it is necessary to match the output impedance with the RAM array by using series resistors. Each application may have different impedance characteristics and may require different series resistance values. The series resistance values should be determined for each application.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin With
Respect to Ground ..... −3.5V to +7V
Power Dissipation ..... 2.5 Watts

NOTICE:
Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, V_{SS} = GND)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	COMMENTS
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 1
V_{ROL}	RAM Output Low Voltage		0.45	V	Note 1
V_{ROH}	RAM Output High Voltage	2.6		V	Note 1
I_{CC}	Supply Current		400	mA	T_A = 0°C
I_{LI}	Input Leakage Current		+10	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Input Capacitance		20	pF	fc = 1 MHz

NOTES:
1. I_{OL} = 16 mA and I_{OH} = −0.4 mA for WE.
   I_{OL} = 8 mA and I_{OH} = −0.2 mA for all other outputs.

AC CHARACTERISTICS

Clock and Programming

REF.	SYMBOL	PARAMETER	WD8207 & WD8207-2 MIN.	WD8207 & WD8207-2 MAX.	WD8207-5 MIN.	WD8207-5 MAX.	UTS.	NOTES
1	TCLCL	Clock Period WD8207 WD8207 WD8207-2	62.5 125 125	500 500 500	 200	 500	ns ns ns	1 2 3
2	TCL	Clock Low Time	TCLCL/2-12		TCLCL/2-12		ns	
3	TCH	Clock High Time	TCLCL/3-3		TCLCL/3-3		ns	
4	TRTVCL	Reset to CLK↓ Setup	40		65		ns	4
5	TRTH	Reset Pulse Width	4TCLCL		4TCLCL		ns	
6	TPGVCL	PCTL, PDI, RFRQ to CLK↓ Setup	125		200		ns	5
7	TCLPGX	PCTL, PDI, RFRQ to CLK↓ Hold	0		0		ns	
8	TCLPC	PCLK from CLK↓ Delay		45		65	ns	
9	TPDVCL	PDIN to CLK↓ Setup	60		100		ns	
10	TCLPDX	PDIN to CLK↓ Hold	40		65		ns	6
RAM Warm-Up and Initialization								
64	TCLWZL	$\overline{WZ}$ from CLK↓ Delay		40		65	ns	7
μP Port Interface								
11	TPEVCL	$\overline{PE}$ to CLK↓ Setup	30		50			2
12	TKVCL	$\overline{RD}$, $\overline{WR}$, $\overline{PE}$, PCTL to CLK↓ Setup	20		30		ns	1,8
13	TCLKX	$\overline{RD}$, $\overline{WR}$, $\overline{PE}$, PCTL to CLK↓ Hold	0		0		ns	
14	TKVCH	$\overline{RD}$, $\overline{WR}$, PCTL to CLK↑ Setup	20		30		ns	2,8
15	TRWVCL	$\overline{RD}$, $\overline{WR}$ to CLK↓ Setup	20		30		ns	9
16	T R W L	$\overline{RD}$, $\overline{WR}$ Pulse Width	2TCLCL+20		2TCLCL+30		ns	
17	TRWLPEV	$\overline{PE}$ from $\overline{RD}$, $\overline{WR}$↓ Delay WD8207 WD8207 WD8207-2		TCLCL – 20 TCLCL – 30 TCLCL – 30		 TCLCL – 50	ns ns ns	1 2 3
18	TRWLPEX	$\overline{PE}$ to $\overline{RD}$, $\overline{WR}$↓ Hold	2TCLCL+20		2TCLCL+30		ns	6
19	TRWLPT	PCTL from $\overline{RD}$, $\overline{WR}$↓ Delay		TCLCL – 20		TCLCL – 30	ns	2
20	TRWLPTX	PCTL to $\overline{RD}$, $\overline{WR}$↓ Hold	2TCLCL+20		2TCLCL+30		ns	2
21	TRWLPT	PCTL from $\overline{RD}$, $\overline{WR}$↓ Delay		2tp – 20			ns	1
22	TRWLPTX	PCTL to $\overline{RD}$, $\overline{WR}$↓ Hold	2tp + 20				ns	1

AC CHARACTERISTICS (Continued)

RAM Interface

REF.	SYMBOL	PARAMETER	WD8207 & WD8207-2 MIN.	WD8207 & WD8207-2 MAX.	WD8207-5 MIN.	WD8207-5 MAX.	UTS.	NOTES
23	TAVCL	AL, AH, BS to CLK↓ Setup	35 + tASR		55 + tASR		ns	10
24	TCLAX	AL, AH, BS to CLK↓Hold	0		0		ns	
25	TCLLN	LEN from CLK↓ Delay		35		55	ns	
26	TCLRSL	$\overline{RAS}$↑ from CLK↓ Delay		35		55	ns	
28	TCLRSH	$\overline{RAS}$↑ from CLK↓ Delay		50		70	ns	
27	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	TCLCL/2 – 25 75 TCLCL – 25		 60 TCLCL – 40		ns ns ns	11 12 1
29	tRAH	Row AO to $\overline{RAS}$↓ Hold	TCLCL/4 – 10 40 TCLCL/2 – 10 90		 35		ns ns ns ns	11,13 12,13 13,14 13,15
30	tASR	Row AO to $\overline{RAS}$↓ Setup						10
31	tASC	Column AO to $\overline{CAS}$↓ Setup	TCLCL/4 – 25 25 TCLCL/2 – 25		 10		ns ns ns	11,16 12,16 1,16
32	tCAH	Column AO to $\overline{CAS}$Hold	(See RAM Timing Tables)					
33	TCLCSL	$\overline{CAS}$↓ from CLK↓ Delay		TCLCL/2 + 45		TCLCL/2 + 70	ns ns	11 12
34	TCLCSL	$\overline{CAS}$↓ from CLK↓ Delay		35			ns	1
35	TCLCSH	$\overline{CAS}$↑ from CLK↓ Delay		50		70	ns	
36	TCLW	WE from CLK↓ Delay		35		55	ns	
37	TCLTKL	$\overline{XACK}$↓ from CLK↓ Delay		35		55	ns	
38	TCLTKH	$\overline{XACK}$↑ from CLK↓ Delay		50		60	ns	
39	TCLAKL	$\overline{AACK}$↓ from CLK↓ Delay		35		55	ns	
40	TCLAKH	$\overline{AACK}$↑ from CLK↓ Delay		50		70	ns	
41	TCLDL	$\overline{DBM}$ from CLK↓ Delay		35		55	ns	

ECC Interface

42	TWRLFV	$\overline{FWR}$ from $\overline{WR}$↓ Delay WD8207 WD8207-2		2TCLCL – 40 TCLCL + TCL – 40		 TCLCL + TCL – 65	ns ns	1,17 2,17
43	TFVCL	$\overline{FWR}$ to CLK↓ Setup	40		65		ns	18
44	TCLFX	$\overline{FWR}$ to CLK↓ Hold	0		0		ns	19
45	TEVCL	$\overline{ERROR}$ to CLK↓ Setup	20		30		ns	20
46	TCLEX	$\overline{ERROR}$ to CLK↓ Hold	0		0		ns	
47	TCLRL	R/$\overline{W}$↓ from CLK↓ Delay		35		55	ns	
48	TCLRH	R/$\overline{W}$↑ from CLK↓ Delay		50		70	ns	
49	TCEVCL	CE to CLK↓ Setup	20		30		ns	20
50	TCLCEX	CE to CLK↓ Hold	0		0		ns	
51	TCLESV	ESTB from CLK↓ Delay		35		55	ns	

AC CHARACTERISTICS (Continued)

Port Switching and Lock

REF.	SYMBOL	PARAMETER	WD8207 & WD8207-2		WD8207-5		UTS.	NOTES
			MIN.	MAX.	MIN.	MAX.		
52	TCLMV	MUX from CLK↓ Delay		45		65	ns	
53	TCHPNV	PSEN from CLK↓ Delay		35		55	ns	
54	TCLPSV	PSEL from CLK↓ Delay		35		55	ns	
55	TLKVCL	LOCK to CLK↓ Setup	30		50		ns	21,22
56	TCLLKX	LOCK to CLK↓ Hold	0		0		ns	21,22
57	TRWLLKV	LOCK from $\overline{RD}$↓, $\overline{WR}$↓ Delay		2TCLCL − 30		2TCLCL − 50	ns	22,23
58	TRWHLKX	LOCK to $\overline{RD}$↑, $\overline{WR}$↑ Hold	3TCLCL+ 20		3TCLCL+ 20		ns	22,23

Refresh Request

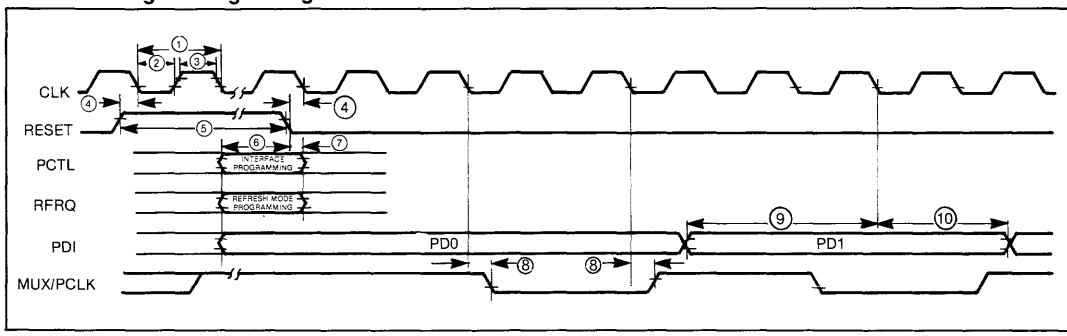
59	TRFVCL	RFRQ to CLK↓ Setup	20		30		ns	
60	TCLRFX	RFRQ to CLK↓ Hold	10		10		ns	
61	TFRFH	Failsafe RFRQ Pulse Width	TCLCL+ 20		TCLCL+ 30		ns	24
62	TRFXCL	Single RFRQ Inactive to CLK↓ Setup	20		30		ns	25
63	TBRFH	Burst RFRQ Pulse Width	2TCLCL+ 20		2TCLCL+ 30		ns	24

NOTES:

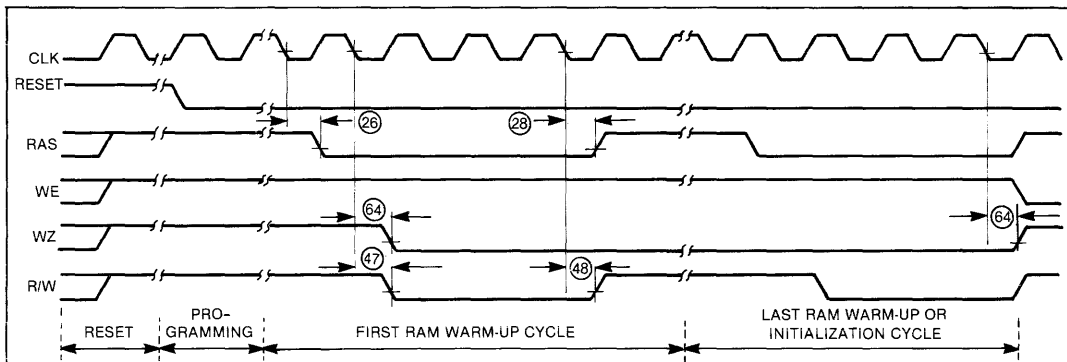
1. Specification when programmed in the Fast Cycle processor mode (iAPX 286 mode).
2. Specification when programmed in the Slow Cycle processor mode (iAPX 186 mode).
3. Must be programmed in Slow Cycle processor mode.
4. RESET is internally synchronized to CLK. Hence, a set-up time is required only to guarantee its recognition at a particular clock edge.
5. The first programming bit (PD0) is also sampled by RESET going low.
6. TCLPDX is guaranteed if programming data is shifted using PCLK.
7. WZ is issued only in ECC mode.
8. TKLCL and TKLCH are not required for an asynchronous command except to guarantee its recognition at a particular clock edge.
9. Valid when programmed in either Fast or Slow Cycle mode.
10. Minimum delay from address inputs to row address outputs is TAVCL − tASR, where tASR ≥ 0 ns; tASR should be specified by user.
11. When programmed in Slow Cycle mode and 125 ns ≤ TCLCL < 200 ns.
12. When programmed in Slow Cycle mode and 200 ns ≤ TCLCL.
13. $C_{AO}/C_{RAS} \geq 0.9$, where C_{AO} is the capacitive load on the address output ($AO_{0\text{-}8}$) pin and C_{RAS} is the capacitive loading of the $\overline{RAS}$ output ($\overline{RAS}_{0\text{-}3}$) pin.
14. When programmed in Fast Cycle mode (WD8207 only) and 62.5 ns ≤ TCLCL < 200 ns.
15. When programmed in Fast Cycle mode (WD8207 only) and 200 ns ≤ TCLCL.
16. $C_{AO}/C_{CAS} \leq 6.5$, where C_{AO} is the capacitive load on the address output ($AO_{0\text{-}8}$) pin and C_{CAS} is the capacitive load on the $\overline{CAS}$ output ($\overline{CAS}_{0\text{-}3}$) pin.
17. TWRLFV is defined for asynchronous $\overline{FWR}$.
18. TFVCL is defined for synchronous $\overline{FWR}$.
19. TCLFV is defined for both synchronous and asynchronous $\overline{FWR}$. In systems in which $\overline{FWR}$ is decoded directly from the address inputs to the WD8207. TCLFV is automatically guaranteed by TCLAV.
20. READ, REFRESH, or PARTIAL WRITE CYCLES: refer to Table 13, to rows marked 'RMW,' for exact clock edges R/$\overline{W}$, $\overline{XACK}$, $\overline{ESTB}$, and WE occur.
21. Synchronous operation only. Must arrive by the second clock falling edge after the clock edge which recognizes the command in order to be effective.
22. LOCK must be held active for the entire period the opposite port must be locked out. Upon release of LOCK the opposite port will be able to obtain access to memory.
23. Asynchronous mode only. In this mode a synchronizer stage is used internally in the WD8207 to synchronize up LOCK. TRWLLKV and TRWHLKX are only required for guaranteeing that LOCK will be recognized for the requesting port, but these parameters are not required for correct WD8207 operation.
24. TFRFH and TBRFH pertain to asynchronous operation only.
25. Single RFRQ cannot by supplied asynchronously.

WAVEFORMS

Clock and Programming Timings



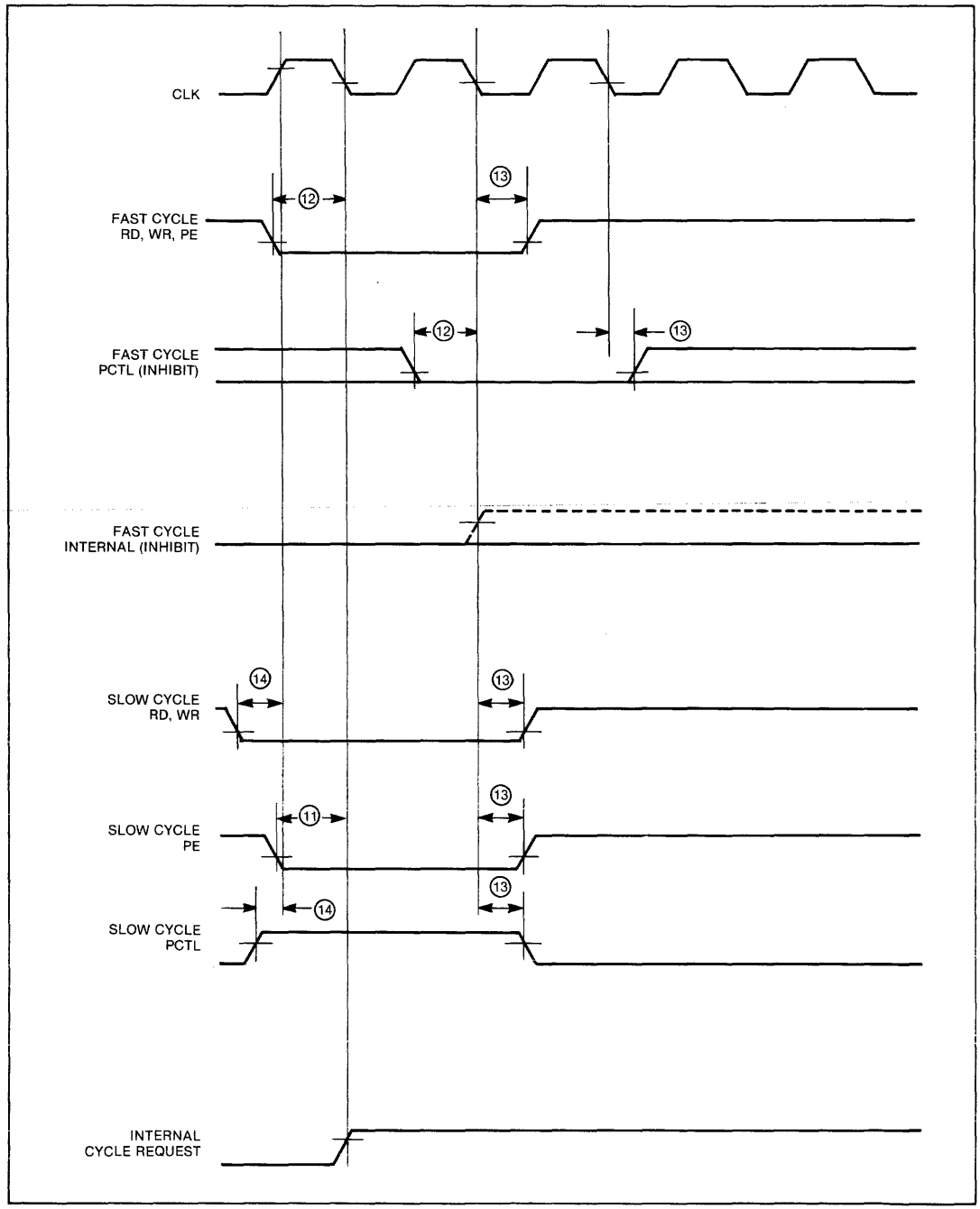
RAM Warm-up and Memory Initialization Cycles



NOTES:
(1) WHEN IN NON-ECC MODE, OR IN ECC MODE WITH THE TM2 PROGRAMMING BIT ON, THERE ARE NO INITIALIZATION CYCLES; WHEN IN ECC MODE WITH TM2 OFF, THE DUMMY CYCLES ARE FOLLOWED BY INITIALIZATION CYCLES.
(2) THE PRESENT EXAMPLE ASSUMES A RAS FOUR CLOCKS LONG.

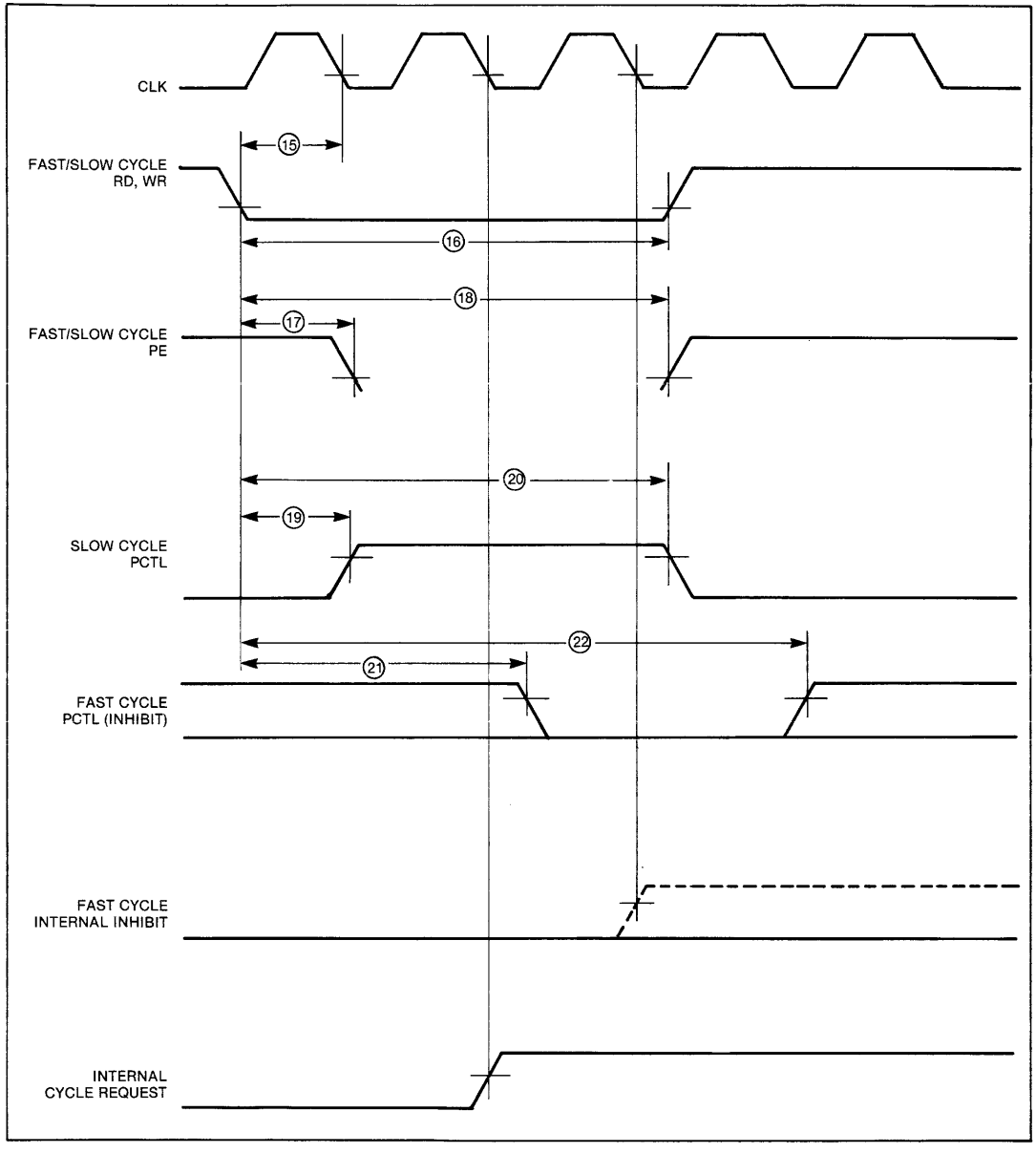
WAVEFORMS (Continued)

Synchronous Port Interface



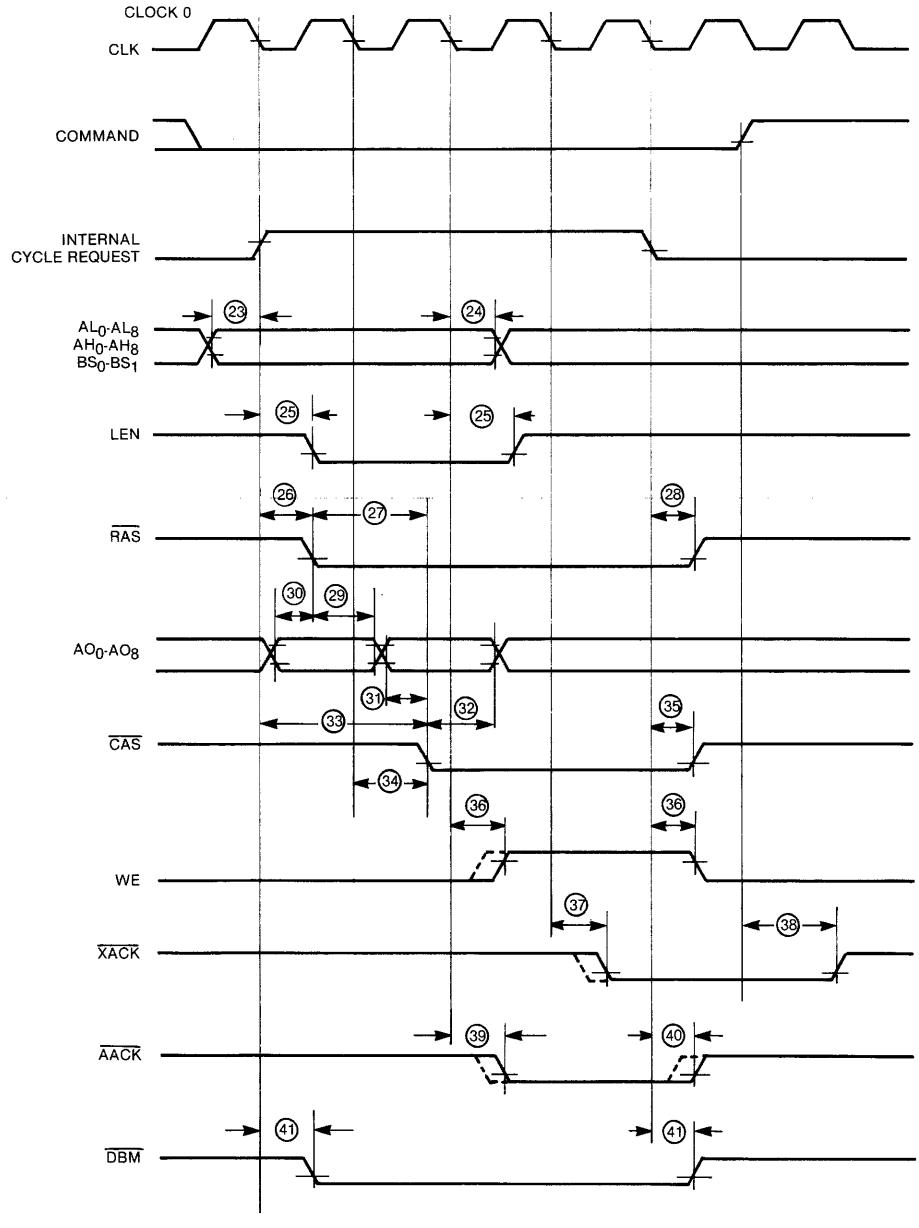
WAVEFORMS (Continued)

Asynchronous Port Interface



WAVEFORMS (Continued)

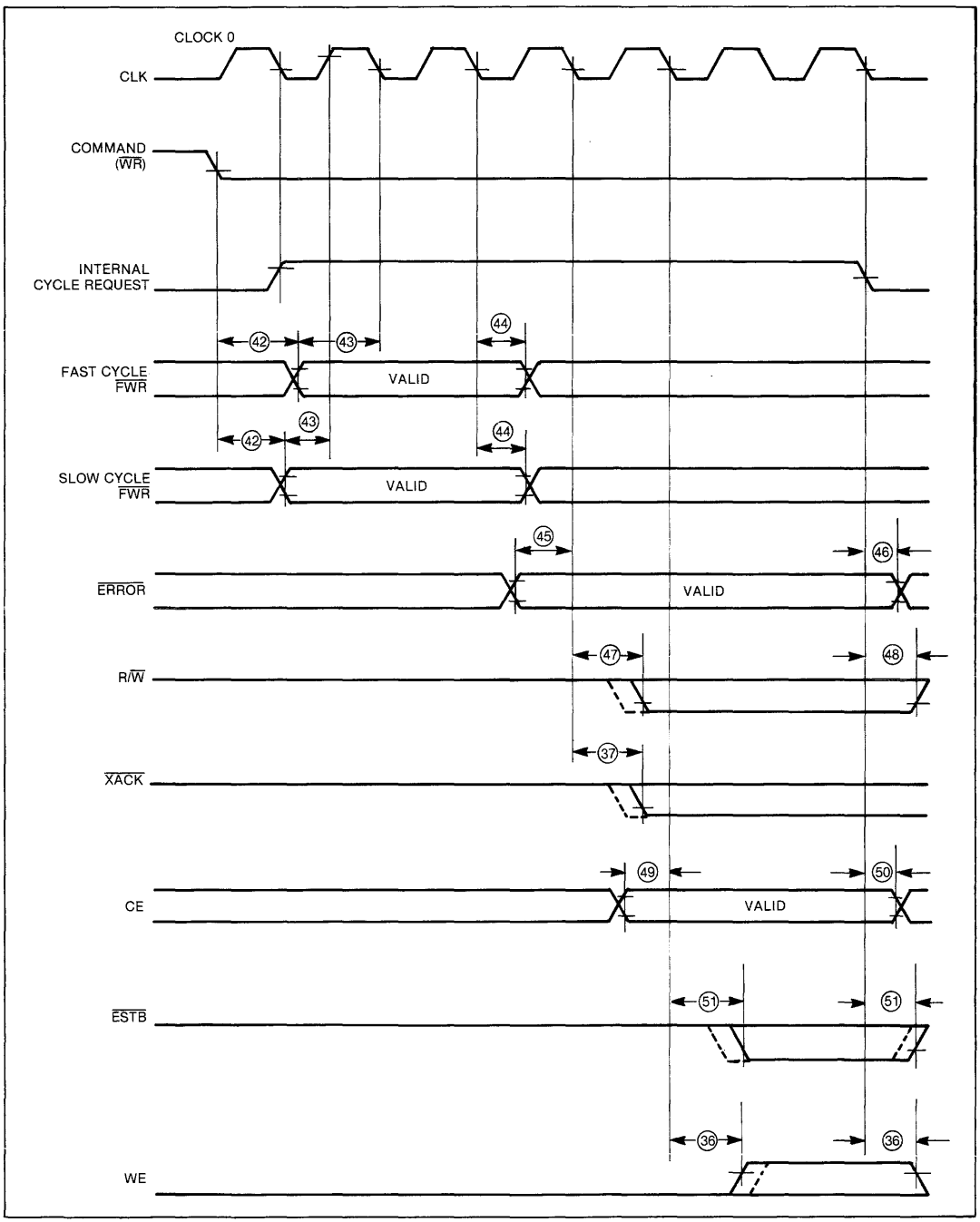
RAM Interface Timing
ECC and Non-ECC Mode



NOTE:
DASHED WAVEFORM INDICATES THAT EITHER CLOCK EDGE MAY CAUSE THE SIGNAL TRANSITION.

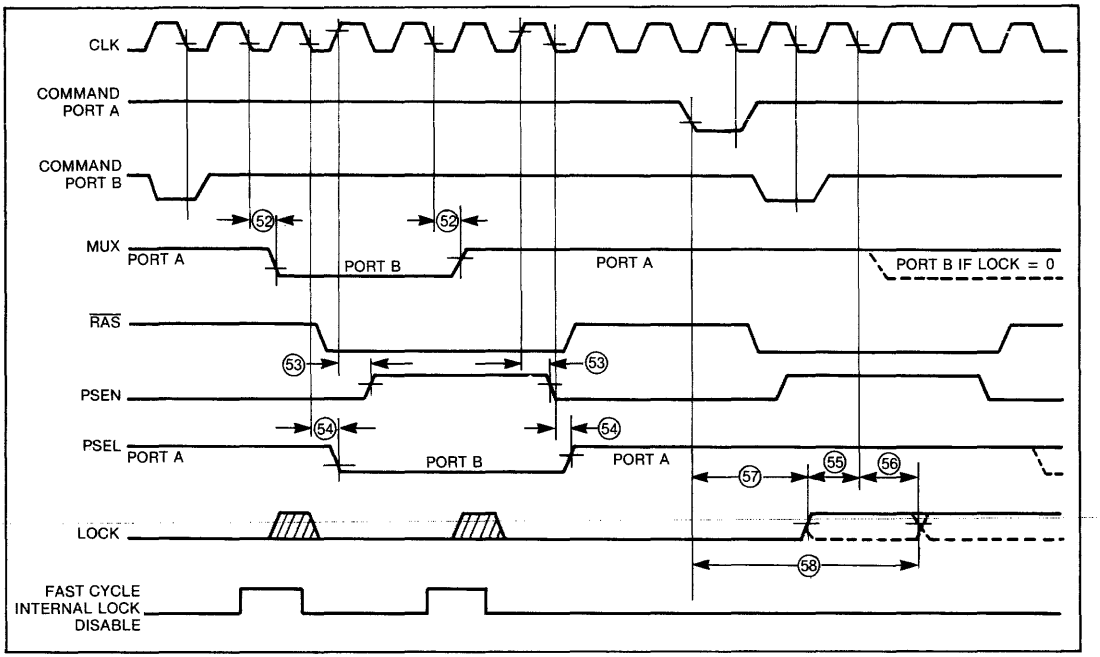
WAVEFORMS (Continued)

ECC Interface Timing

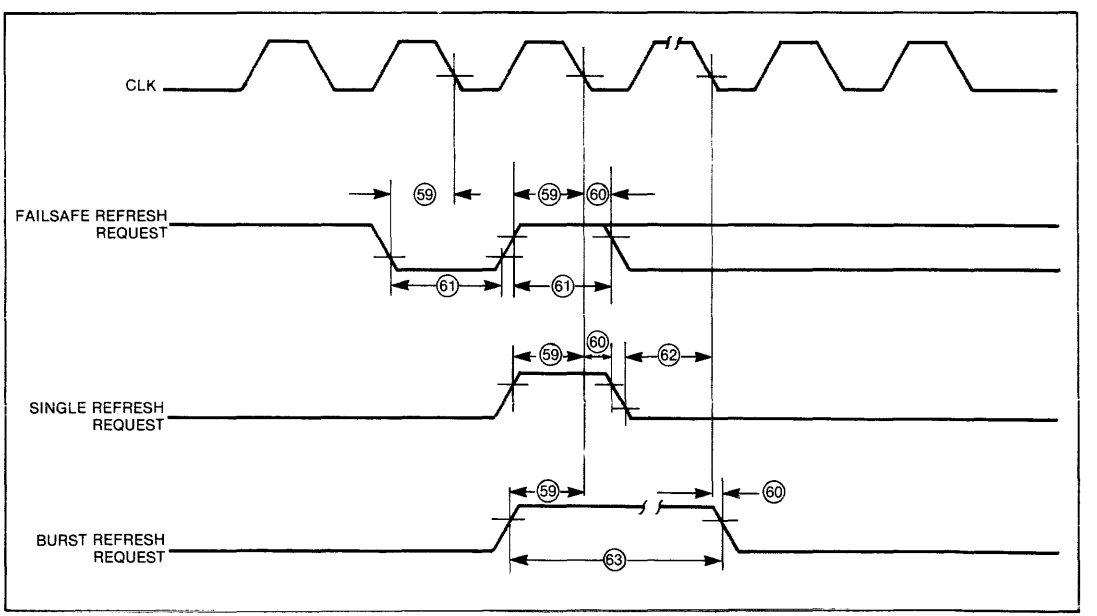


WAVEFORMS (Continued)

Port Switching and Lock Timing



Refresh Request Timing



CONFIGURATION TIMING CHARTS

The timing charts that follow are based on 8 basic system configurations where the WD8207 operates.

Tables 10 and 11 give a description of non-ECC and ECC system configurations based on the WD8207's PD0, PD3, PD4, PD10 and PD11 programming bits.

Table 10. NON-ECC SYSTEM CONFIGURATIONS

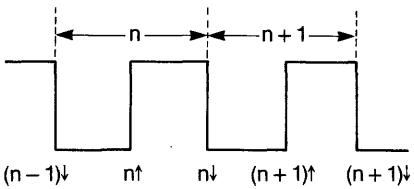
NON-ECC MODE: PD0 = 0				
TIMING CONF.	$\overline{CFS}$ (PD3)	$\overline{RFS}$ (PD4)	EXT (PD10)	$\overline{FFS}$ (PD11)
C_0	(0)	Fast RAM (0)	Not EXT (0)	10 MHz (1)
C_0	(0)	Fast RAM (0)	EXT (1)	10 MHz (1)
C_0	(0)	Slow RAM (1)	Not EXT (0)	10 MHz (1)
C_0	(0)	Slow RAM (1)	EXT (1)	10 MHz (1)
C_0	(0)	Fast RAM (0)	Not EXT (0)	16 MHz (0)
C_1	(0)	Slow RAM (1)	Not EXT (0)	16 MHz (0)
C_1	(0)	Fast RAM (0)	EXT (1)	16 MHz (0)
C_2	(0)	Slow RAM (1)	EXT (1)	16 MHz (0)
C_3	(1)	Fast RAM (0)	Not EXT (0)	8 MHz (0)
C_3	(1)	Slow RAM (1)	Not EXT (0)	8 MHz (0)
C_3	(1)	Fast RAM (0)	EXT (1)	8 MHz (0)
C_3	(1)	Fast RAM (0)	Not EXT (0)	5 MHz (1)
C_3	(1)	Fast RAM (0)	EXT (1)	5 MHz (1)
C_3	(1)	Slow RAM (1)	Not EXT (0)	5 MHz (1)
C_3	(1)	Slow RAM (1)	EXT (1)	5 MHz (1)
C_4	(1)	Slow RAM (1)	EXT (1)	8 MHz (0)

Table 11. ECC SYSTEM CONFIGURATIONS

ECC MODE: PD0 = 1				
TIMING CONF.	CFS (PD3)	RFS (PD4)	$\overline{EXT}$ (PD10)	FFS (PD11)
C_0	(1)	Slow RAM (0)	M/S EDCU (0)	10 MHz (0)
C_0	(1)	Slow RAM (0)	M EDCU (1)	10 MHz (0)
C_0	(1)	Fast RAM (1)	M/S EDCU (0)	10 MHz (0)
C_0	(1)	Fast RAM (1)	M EDCU (1)	10 MHz (0)
C_0	(1)	Fast RAM (1)	M EDCU (1)	16 MHz (1)
C_1	(1)	Slow RAM (0)	M EDCU (1)	16 MHz (1)
C_2	(1)	Fast RAM (1)	M/S EDCU (0)	16 MHz (1)
C_3	(1)	Slow RAM (0)	M/S EDCU (0)	16 MHz (1)
C_4	(0)	Slow RAM (0)	M/S EDCU (0)	5 MHz (0)
C_4	(0)	Fast RAM (1)	M/S EDCU (0)	5 MHz (0)
C_4	(0)	Slow RAM (0)	M EDCU (1)	8 MHz (1)
C_4	(0)	Fast RAM (1)	M EDCU (1)	8 MHz (1)
C_5	(0)	Slow RAM (0)	M/S EDCU (0)	8 MHz (1)
C_5	(0)	Fast RAM (1)	M/S EDCU (0)	8 MHz (1)
C_6	(0)	Slow RAM (0)	M EDCU (1)	5 MHz (0)
C_6	(0)	Fast RAM (1)	M EDCU (1)	5 MHz (0)

Using the Timing Charts

The notation used to indicate which clock edge triggers an output transition is "n↑" or "n↓", where "n" is the number of clock periods that have passed since clock 0, the reference clock, and "↑" refers to rising edge and "↓" to falling edge. A clock period is defined as the interval from a clock falling edge to the following falling edge. Clock edges are defined as shown below.



The clock edges which trigger transitions on each WD8207 output are tabulated in Table 12 for non-ECC mode, and Table 13 for ECC mode. "H" refers to the high-going transition, and "L" to low-going transition; "V" refers to valid, and "$\overline{V}$" to non-valid.

Clock 0 is defined as the clock in which the WD8207 begins a memory cycle, either as a result of a port request which has just arrived, or of a port request which was stored previously but could not be serviced at the time of its arrival because the WD8207 was performing another memory cycle. Clock 0 may be identified externally by the leading edge of RAS, which is always triggered on 0↓.

Notes for interpreting the timing charts.

1. **PSEL — valid** is given as the latest time it can occur. It is entirely possible for PSEL to become valid before the time given. In a refresh cycle, PSEL can switch as defined in the chart, but it has no bearing on the refresh cycle itself, but only on a subsequent cycle for one of the external ports.
2. **LEN — low** is given as the latest time it can occur. LEN is only activated by port A configured in Fast Cycle, and thus it is not activated by a refresh cycle, although it may be activated by port A during a refresh cycle.
3. In non-ECC mode the $\overline{CAS}$, $\overline{EAACK}$, $\overline{LAACK}$ and $\overline{XACK}$ outputs are not issued during refresh.
4. In ECC mode there are really seven types of cycles: Read without error, read with error, full write, partial write without error, partial write with error, refresh without error, and refresh with error. These cycles may be derived from the timing chart as follows:
   A. Read without error: Use row marked 'RD, RF.'
   B. Read with error: Use row marked 'RMW,' except for $\overline{EAACK}$ and $\overline{LAACK}$, which should be taken from 'RD, RF.' If the error is uncorrectable, WE will not be issued.
   C. Full write: Use row marked 'WR.'
   D. Partial write without error: Use row marked 'RMW,' except that $\overline{DBM}$ and $\overline{ESTB}$ will not be issued.
   E. Partial write with error: Use row marked 'RMW,' except that $\overline{DBM}$ will not be issued. If the error is uncorrectable, WE will not be issued.
   F. Refresh without error: Use row marked 'RD, RF.' except that $\overline{ESTB}$, $\overline{EAACK}$, $\overline{LAACK}$, and $\overline{XACK}$ will not be issued.
   G. Refresh with error: Use row marked 'RMW' except that $\overline{EAACK}$, $\overline{LAACK}$, $\overline{ESTB}$, and $\overline{XACK}$ will not be issued. If the error is uncorrectable WE will not be issued.
5. **XACK — high** is reset asynchronously by command going inactive and not by a clock edge.
6. **MUX — valid** is given as the latest time it can occur.

Table 12A. TIMING CHART — NON-ECC MODE

		PSEN		PSEL		$\overline{DBM}$		LEN		$\overline{RAS}$		CAS		WE	
C_n	CYCLE	H	L	V	$\overline{V}$	L	H	L	H	L	H	L	H	H	L
C_0	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	1↓	4↓		
C_0	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	1↓	5↓	2↓	5↓
C_1	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓		
C_1	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	1↓	5↓	2↑	5↓
C_2	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓		
C_2	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	1↓	5↓	2↓	5↓
C_3	RD, RF	1↑	2↑	0↓	3↓	0↓	3↓	0↓	2↓	0↓	3↓	0↓	3↓		
C_3	WR	1↑	4↑	0↓	4↓			0↓	2↓	0↓	4↓	0↓	4↓	2↑	4↓
C_4	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	4↓	0↓	4↓		
C_4	WR	1↑	4↑	0↓	4↓			0↓	2↓	0↓	4↓	0↓	4↓	2↑	4↓

Table 12B. TIMING CHART — NON-ECC MODE

		$\overline{EAACK}$		$\overline{LAACK}$		$\overline{XACK}$		MUX	
C_n	CYCLE	L	H	L	H	L	H	V	V
C_0	RD, RF	1↓	4↓	2↓	5↓	3↓	RD	−2↓	2↓
C_0	WR	1↓	4↓	1↓	4↓	3↓	WR	−2↓	2↓
C_1	RD, RF	2↓	5↓	2↓	5↓	4↓	RD	−2↓	2↓
C_1	WR	1↓	4↓	1↓	4↓	3↓	WR	−2↓	2↓
C_2	RD, RF	2↓	5↓	3↓	6↓	4↓	RD	−2↓	2↓
C_2	WR	1↓	4↓	1↓	4↓	3↓	WR	−2↓	2↓
C_3	RD, RF	0↓	3↓	1↓	3↓	2↓	RD	−1↓	2↓
C_3	WR	0↓	2↓	1↑	3↑	2↓	WR	−1↓	2↓
C_4	RD, RF	1↓	3↓	1↓	3↓	3↑	RD	−1↓	2↓
C_4	WR	0↓	2↓	1↑	3↑	2↓	WR	−1↓	2↓

Table 13A. TIMING CHART — ECC MODE

		PSEN		PSEL		DBM		LEN		RAS		CAS		R/W		WE	
C_n	CYCLE	H	L	V	V	L	H	L	H	L	H	L	H	L	H	H	L
C_0	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓				
C_0	WR	1↑	6↑	0↓	6↓			0↓	2↓	0↓	6↓	1↓	6↓	1↓	6↓	3↓	6↓
C_0	RMW	1↑	9↑	0↓	9↓	0↓	9↓	0↓	2↓	0↓	9↓	1↓	9↓	4↓	9↓	6↓	9↓
C_1	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓				
C_1	WR	1↑	6↑	0↓	6↓			0↓	2↓	0↓	6↓	1↓	6↓	1↓	6↓	3↓	6↓
C_1	RMW	1↑	9↑	0↓	9↓	0↓	9↓	0↓	2↓	0↓	9↓	1↓	9↓	4↓	9↓	6↓	9↓
C_2	RD, RF	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	5↓	1↓	7↓				
C_2	WR	1↑	7↑	0↓	7↓			0↓	2↓	0↓	7↓	1↓	7↓	1↓	7↓	4↓	7↓
C_2	RMW	1↑	11↑	0↓	11↓	0↓	11↓	0↓	2↓	0↓	11↓	1↓	11↓	5↓	11↓	8↓	11↓
C_3	RD, RF	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	5↓	1↓	7↓				
C_3	WR	1↑	7↑	0↓	7↓			0↓	2↓	0↓	7↓	1↓	7↓	1↓	7↓	4↓	7↓
C_3	RMW	1↑	11↑	0↓	11↓	0↓	11↓	0↓	2↓	0↓	11↓	1↓	11↓	5↓	11↓	8↓	11↓
C_4	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	0↓	4↓				
C_4	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	0↓	5↓	1↓	5↓	3↓	5↓
C_4	RMW	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	7↓	0↓	7↓	3↓	7↓	5↓	7↓
C_5	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	0↓	4↓				
C_5	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	0↓	5↓	1↓	5↓	3↓	5↓
C_5	RMW	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	7↓	0↓	7↓	3↓	7↓	5↓	7↓
C_6	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	0↓	4↓				
C_6	WR	1↑	4↑	0↓	4↓			0↓	2↓	0↓	4↓	0↓	4↓	1↓	4↓	2↓	4↓
C_6	RMW	1↑	5↑	0↓	5↓	0↓	5↓	0↓	2↓	0↓	5↓	0↓	5↓	2↑	5↓	3↑	5↓

WD8207 — DRAM Interface Parameter Equations

Several DRAM parameters, but not all, are a direct function of WD8207 timings, and the equations for these parameters are given in the following tables. The following is a list of those DRAM parameters which have NOT been included in the following tables, with an explanation for their exclusion.

READ, WRITE, READ-MODIFY-WRITE & REFRESH CYCLES

tRAC: response parameter.
tCAC: response parameter.
tREF: See "Refresh Period Options"
tCRP: must be met only if CAS-only cycles, which do not occur with WD8207, exist.
tRAH: See "AC Characteristics"
tRCD: See "AC Characteristics"
tASC: See "AC Characteristics"
tASR: See "AC Characteristics"
tOFF: response parameter.

READ & REFRESH CYCLES

tRCH: WE always goes active after $\overline{CAS}$ goes active, hence tRCH is guaranteed by tCPN.

WRITE CYCLE

tRC: guaranteed by tRWC.
tRAS: guaranteed by tRRW.
tCAS: guaranteed by tCRW.
tWCS: WE always activated after $\overline{CAS}$ is activated, except in memory initialization, hence tWCS is always negative (this is important for RMW only) except in memory initialization; in memory initialization tWCS is positive and has several clocks of margin.
tDS: system-dependent parameter.
tDH: system-dependent parameter.
tDHR: system-dependent parameter.

READ-MODIFY-WRITE CYCLE

tRWD: don't care in WD8207 write cycles, but tabulated for WD8207 RMW cycles.
tCWD: don't care in WD8207 write cycles, but tabulated for WD8207 RMW cycles.

Table 13B. TIMING CHART — ECC MODE

C_n	CYCLE	$\overline{ESTB}$		$\overline{EAACK}$		$\overline{LAACK}$		$\overline{XACK}$		MUX	
		L	H	L	H	L	H	L	H	V	$\overline{V}$
C_0	RD, RF			2↓	5↓	3↓	6↓	4↓	$\overline{RD}$	−2↓	2↓
C_0	WR			2↓	5↓	2↓	5↓	4↓	$\overline{WR}$	−2↓	2↓
C_0	RMW	6↓	8↓	5↓	8↓	5↓	8↓	7↓	$\overline{WR}$	−2↓	2↓
C_1	RD, RF			3↓	6↓	3↓	6↓	4↓	$\overline{RD}$	−2↓	2↓
C_1	WR			2↓	5↓	2↓	5↓	4↓	$\overline{WR}$	−2↓	2↓
C_1	RMW	6↓	8↓	5↓	8↓	5↓	8↓	7↓	$\overline{WR}$	−2↓	2↓
C_2	RD, RF			4↓	7↓	4↓	7↓	5↓	$\overline{RD}$	−2↓	2↓
C_2	WR			3↓	6↓	3↓	6↓	5↓	$\overline{WR}$	−2↓	2↓
C_2	RMW	8↓	10↓	7↓	10↓	7↓	10↓	9↓	$\overline{WR}$	−2↓	2↓
C_3	RD, RF			4↓	7↓	5↓	8↓	5↓	$\overline{RD}$	−2↓	2↓
C_3	WR			3↓	6↑	3↓	6↓	5↓	$\overline{WR}$	−2↓	2↓
C_3	RMW	8↓	10↓	7↓	10↓	7↓	10↓	9↓	$\overline{WR}$	−2↓	2↓
C_4	RD, RF			1↓	3↓	2↑	4↑	3↑	$\overline{RD}$	−1↓	2↓
C_4	WR			1↓	3↓	2↑	4↑	3↓	$\overline{WR}$	−1↓	2↓
C_4	RMW	5↑	6↑	3↓	5↓	4↑	6↑	5↓	$\overline{WR}$	−1↓	2↓
C_5	RD, RF			2↓	4↓	3↑	5↑	3↑	$\overline{RD}$	−1↓	2↓
C_5	WR			1↓	3↓	2↑	4↑	3↓	$\overline{WR}$	−1↓	2↓
C_5	RMW	5↑	6↑	3↓	5↓	4↑	6↑	5↓	$\overline{WR}$	−1↓	2↓
C_6	RD, RF			1↓	3↓	1↑	3↑	2↑	$\overline{RD}$	−1↓	2↓
C_6	WR			1↓	3↓	1↑	3↑	2↓	$\overline{WR}$	−1↓	2↓
C_6	RMW	3↑	4↑	1↓	3↓	2↑	4↑	3↓	$\overline{WR}$	−1↓	2↓

Table 14. NON-ECC MODE — RD, RF CYCLES

PARAMETER	FAST CYCLE CONFIGURATIONS			SLOW CYCLE CONFIGURATIONS		NOTES
	C_0	C_1	C_2	C_3	C_4	
tRP	3TCLCL—T26	4TCLCL—T26	4TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	3TCLCL—T35	3TCLCL—T35	3TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	2TCLCL—T34	3TCLCL—T34	3TCLCL—T34	3TCLCL—T34	4TCLCL—T34	1
tCSH	4TCLCL—T26	6TCLCL—T26	6TCLCL—T26	3TCLCL—T26	4TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	3/30	2
tRC	6TCLCL	8TCLCL	8TCLCL	5TCLCL	6TCLCL	1
tRAS	3TCLCL—T26	4TCLCL—T26	4TCLCL—T26	3TCLCL—T26	4TCLCL—T26	1
tCAS	3TCLCL—T34	5TCLCL—T34	5TCLCL—T34	3TCLCL—T34	4TCLCL—T34	1
tRCS	2TCLCL—TCL —T36—TBUF	2TCLCL—TCL —T36—TBUF	2TCLCL—TCL —T36—TBUF	1.5TCLCL—TCL —T36—TBUF	1.5TCLCL—TCL —T36—TBUF	1

Table 15. NON-ECC MODE — WR CYCLE

PARAMETER	FAST CYCLE CONFIGURATIONS			SLOW CYCLE CONFIGURATIONS		NOTES
	C_0	C_1	C_2	C_3	C_4	
tRP	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tCSH	5TCLCL—T26	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	3/30	2
tRWC	8TCLCL	8TCLCL	8TCLCL	6TCLCL	6TCLCL	1
tRRW	5TCLCL—T26	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCRW	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tWCH	3TCLCL + TCL —T34	3TCLCL + TCL —T34	3TCLCL + TCL —T34	3TCLCL + TCL —T34	3TCLCL + TCL —T34	1,3
tWCR	4TCLCL + TCL —T26	4TCLCL + TCL —T26	4TCLCL + TCL —T26	3TCLCL + TCL —T26	3TCLCL + TCL —T26	1,3
tWP	2TCLCL + TCL —T36—TBUF	2TCLCL + TCL —T36—TBUF	2TCLCL + TCL —T36—TBUF	2TCLCL—TCL —TBUF	2TCLCL—T36 —TBUF	1
tRWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—TCL —TBUF	3TCLCL—TCL —TBUF	1
tCWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1

Table 16A. ECC MODE — RD, RF CYCLES

PARAMETER	FAST CYCLE MODE				NOTES
	C_0	C_1	C_2	C_3	
tRP	4TCLCL—T26	4TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCPN	3TCLCL—T35	3TCLCL—T35	3TCLCL—T35	3TCLCL—T35	1
tRSH	3TCLCL—T34	3TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tCSH	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	2
tRC	8TCLCL	8TCLCL	9TCLCL	9TCLCL	1
tRAS	4TCLCL—T26	4TCLCL—T26	5TCLCL—T26	5TCLCL—T26	1
tCAS	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1
tRCS	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	1

Table 16B. ECC MODE — RD, RF CYCLES

PARAMETER	SLOW CYCLE MODE			
	C_4	C_5	C_6	NOTES
tRP	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	1.5TCLCL—T35	1.5TCLCL—T35	1.5TCLCL—T35	1
tRSH	3TCLCL—T34	3TCLCL—T34	3TCLCL—T34	1
tCSH	4TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCAH	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	2
tRC	5TCLCL	5TCLCL	5TCLCL	1
tRAS	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tCAS	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tRCS	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	1

Table 17A. ECC MODE — WR CYCLE

PARAMETER	FAST CYCLE MODE				
	C_0	C_1	C_2	C_3	NOTES
tRP	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tCPN	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	1
tRSH	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1
tCSH	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	2
tRWC	9TCLCL	9TCLCL	10TCLCL	10TCLCL	1
tRRW	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1
tCRW	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1
tWCH	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1,4
tWCR	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1,4
tWP	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tRWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tCWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1

Table 17B. ECC MODE — WR CYCLE

PARAMETER	SLOW CYCLE MODE			
	C_4	C_5	C_6	NOTES
tRP	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	2.5TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	5TCLCL—T34	5TCLCL—T34	4TCLCL—T34	1
tCSH	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	1
tCAH	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	2
tRWC	7TCLCL	7TCLCL	6TCLCL	1
tRRW	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	1
tCRW	5TCLCL—T34	5TCLCL—T34	4TCLCL—T34	1
tWCH	5TCLCL—T34	5TCLCL—T34	4TCLCL—T34	1,4
tWCR	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	1,4
tWP	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tRWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tCWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1

Table 18A. ECC MODE — RMW

PARAMETER	FAST CYCLE MODE				
	C_0	C_1	C_2	C_3	NOTES
tRP	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tCPN	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	1
tRSH	8TCLCL—T34	8TCLCL—T34	10TCLCL—T34	10TCLCL—T34	1
tCSH	9TCLCL—T26	9TCLCL—T26	11TCLCL—T26	11TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	2
tRWC	12TCLCL	12TCLCL	14TCLCL	14TCLCL	1
tRRW	9TCLCL—T26	9TCLCL—T26	11TCLCL—T26	11TCLCL—T26	1
tCRW	8TCLCL—T34	8TCLCL—T34	10TCLCL—T34	10TCLCL—T34	1
tRCS	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	1
tRWD	6TCLCL—T26	6TCLCL—T26	8TCLCL—T26	8TCLCL—T26	1
tCWD	5TCLCL—T34	5TCLCL—T34	7TCLCL—T34	7TCLCL—T34	1
tWP	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tRWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tCWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1

Table 18B. ECC MODE — RMW

PARAMETER	SLOW CYCLE MODE			
	C_4	C_5	C_6	NOTES
tRP	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	2.5TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	7TCLCL—T34	7TCLCL—T34	5TCLCL—T34	1
tCSH	7TCLCL—T26	7TCLCL—T26	5TCLCL—T26	1
tCAH	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	2
tRWC	9TCLCL	9TCLCL	7TCLCL	1
tRRW	7TCLCL—T26	7TCLCL—T26	5TCLCL—T26	1
tCRW	7TCLCL—T34	7TCLCL—T34	5TCLCL—T34	1
tRCS	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	1
tRWD	4TCLCL + TCL —T26	4TCLCL + TCL —T26	2TCLCL + TCL —T26	1
tCWD	4TCLCL + TCL —T34	4TCLCL + TCL —T34	2TCLCL + TCL —T34	1
tWP	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tRWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tCWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1

NOTES:
1. Minimum.
2. Value on right is maximum; value on left is minimum.
3. Applies to the eight warm-up cycles during initialization only.
4. Applies to the eight warm-up cycles and to the memory initialization cycles during initialization only.
5. TP = TCLCL
   T26 = TCLRSL
   T34 = TCLCSL
   T35 = TCLCSH
   T36 = TCLW
   TBUF = TTL Buffer delay

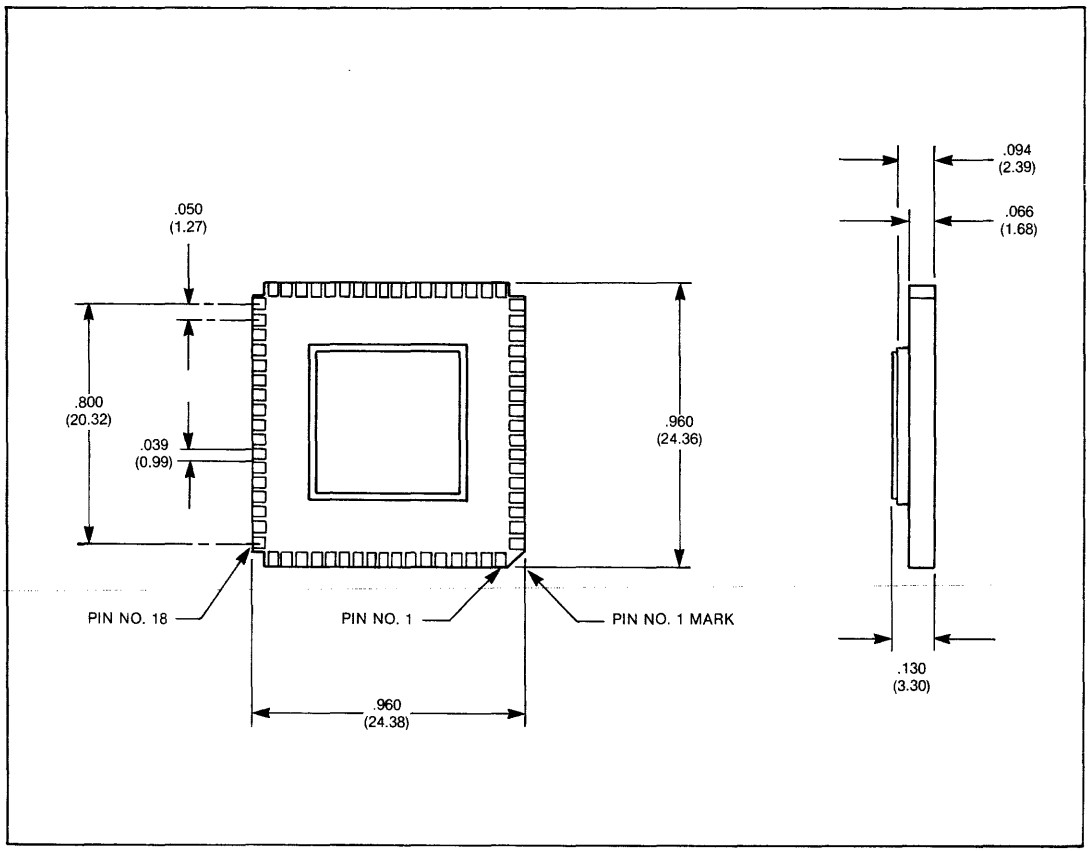


Figure 18. WD8207 JEDEC TYPE A PACKAGE

See page 481 for ordering information.

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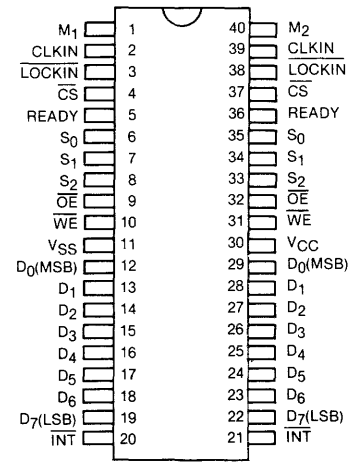
PRELIMINARY

WD99650 Multiprocessor Interface Device

FEATURES

- TWO FULLY INDEPENDENT, ASYNCHRONOUS PORTS
- EIGHT PROGRAMMABLE 8-BIT REGISTERS PER PORT
- STATUS AND CONTROL REGISTERS
- INTERRUPT REQUEST CONTROL AT EACH PORT
- POINTER REGISTERS INCREMENTABLE FOLLOWING RAM ACCESS
- MESSAGE REGISTERS TO PASS DATA BETWEEN PORTS INDEPENDENT OF RAM ARBITRATION LOGIC
- 256 BYTES OF RAM ADDRESSED INDIRECTLY USING POINTER REGISTERS
- HARDWARE SUPPORT FOR UTILIZATION OF RAM AS FIRST-IN FIRST-OUT (FIFO) BUFFER BETWEEN PORTS
- WIDTH OF DATA PATH EXPANDABLE IN 8-BIT INCREMENTS
- INTERNAL ARBITRATION OF ASYNCHRONOUS RAM-ACCESS CONFLICTS
- OPTIONAL READY SIGNAL FOR CONCURRENT USE OF THE MEMORY BY BOTH PORTS
- READY SYNCHRONIZED ON CHIP; CLKIN REQUIRED ONLY IF READY IS USED
- HARDWARE LOCKOUT CAPABILITY PROVIDED TO SUPPORT TEST-AND-SET, TEST-AND-CLEAR OPERATIONS
- SOFTWARE LOCKOUT FACILITY WITH INTERRUPT FOR CONFIRMATION
- SINGLE +5V SUPPLY
- 40-PIN DIP PACKAGE
- N-CHANNEL SILICON-GATE TECHNOLOGY



PIN DESIGNATION

DESCRIPTION

The WD99650 Multiprocessor Interface device (MPIF) provides a bit-parallel, asynchronous communications interface for passing messages and data between two processors or processor systems. It represents a standard peripheral interface consisting of eight programmable registers at each of its two ports and furnishes access to 256 bytes of random-access (RAM) used to buffer data transmitted between ports. The WD99650 supplies arbitration logic to resolve RAM-access conflicts between the two processor systems. The WD99650 can be used to connect virtually any 8-bit or 16-bit microprocessor to any other 8-bit or 16-bit microprocessor having the capability of interfacing to standard memory or peripheral devices.

PIN DESCRIPTION

SYMBOL	PIN NUMBER PORT A	PIN NUMBER PORT B	TYPE I/O	DESCRIPTION
M_1 M_2	1 40			MODE PINS: Reset the MPIF and establish whether it is to work in master, slave, or stand-alone mode.
CLKIN	2	39	I	CLOCK-IN: Allows READY to be presented synchronously to the host system.
$\overline{\text{LOCKIN}}$	3	38	I	LOCKOUT IN: Indicates to the MPIF that the opposite port should be denied access to the RAM.
$\overline{CS}$	4	37	I	CHIP SELECT: Indicates that the host system requires access to one of the MPIF internal registers.
READY	5	36	O	READY: Indicates to the host system that the memory operation in progress may be completed.
S_0	6	35	I	REGISTER SELECT LINES: Indicate to the MPIF which internal register is accessed by the host system.
S_1	7	34	I	
S_2	8	33	I	
$\overline{OE}$	9	32	I	OUTPUT ENABLE: Indicates that the host system is performing a read operation.
$\overline{WE}$	10	31	I	WRITE ENABLE: Indicates that the host is performing a write operation.
V_{CC}	30			POWER SUPPLY
V_{SS}	11			GROUND REFERENCE
D_0(MSB)	12	29	I/O	DATA BUS: Provides for bidirectional data transfer between the MPIF port and the host system.
D_1	13	28	I/O	
D_2	14	27	I/O	
D_3	15	26	I/O	
D_4	16	25	I/O	
D_5	17	24	I/O	
D_6	18	23	I/O	
D_7(LSB)	19	22	I/O	
$\overline{INT}$	20	21	O(o/d)*	INTERRUPT: Indicates to the host system that it should branch to a service routine.

*o/d = open drain output: all others are push/pull outputs.

ARCHITECTURE

The WD99650 Multiprocessor Interface, shown in Figure 1 as a block diagram, is built around a 256 x 8-bit static random-access memory and includes two complete microprocessor interfaces and two complete data paths. Each data path connects the microprocessor interface to the appropriate on-chip registers under the control of the external interface control signals, register select lines, and the arbitration latch.

Both interfaces have access to the RAM via data registers, which are simple bidirectional buffers between the RAM and the data paths and involve no storage.

Each data register has associated with it an address pointer register that supplies the address to the RAM when the corresponding data register is used. The address registers can be written to and read from both microprocessor interfaces.

Two message registers are provided, one assigned to each port. Each interface can read and write its own message register but only read that of the other interface.

The control register provides for the configuration and control of the WD99650. It includes the various Interrupt enable bits.

The status register shows the condition of the various interrupt sources.

The RAM can only be used by one host microprocessor, via its data register, at one time. The two outputs of the arbitration latch, ACTA and ACTB, control access to the RAM. These outputs select the RAM data and address buses from either the DATA A and ADDR A registers or the DATA B and ADDR B registers respectively. ACTA becomes true when the data register of port A is addressed, but only if ACTB is not already true and port B has not asserted a lockout. A corresponding definition applies for ACTB. Hence, the two signals are mutually exclusive, which ensures that both interfaces cannot use the RAM at once: The WD99650 provides its host microprocessors with continuous access to all the other registers.

If both interfaces try to gain access to the RAM concurrently, the first to address its data register will exclude the other. The RAM is assigned on a first-come, first-serve basis unless a lockout is in effect (see Lockout Capability).

Occasionally, both ports may address their data registers at exactly the same time. This can put the arbitration latch into an indeterminate state for some time. Due to the cross-coupled nature of ACTA and ACTB, the indeterminate state will be unstable. Eventually the conflict will resolve itself, the outcome being essentially random. ACTA and ACTB pass through threshold circuits to ensure that the unstable state is interpreted as an inactive state for both bits.

Each interface can request exclusive use of the RAM using the lockout feature. This is asserted by means of a software-accessible bit or with a dedicated input pin. In situations where both ports assert a lockout, the RAM is assigned on a first-come, first-serve basis.

A memory cycle cannot be allowed to proceed if the port concerned does not succeed in getting access to the RAM or there is uncertainty in the arbitration latch. The problem of sharing the RAM between two ports may be approached in three ways:

1. Ensure in software that both host ports do not try to use the RAM at the same time. Thus any attempt to gain access to the RAM is guaranteed to be successful. This involves the two systems passing messages between themselves regarding their status and intentions, for which the message registers may be used.
2. Use the READY signal provided by the WD99650 to put the system into a wait state if it is not successful in gaining access to the RAM or if uncertainty exists in the arbitration latch.
3. Use the software-accessible lockout bit to request exclusive use of the RAM. Wait until this is acknowledged before attempting access to the RAM.

It is possible to use method 2 on one port and 3 on the other port.

REGISTER DESCRIPTION

The WD99650 occupies eight locations in the memory map of each host system. It is so arranged that the registers accessible at the same location of each port serve the same function. The ports of the WD99650 are therefore completely identical and can be reversed without software or hardware changes. For the purpose of naming the locations in the memory map, the port under consideration is referred to as the local port and the other is referred to as the remote port. The location and function of each register is shown in Table 1.

DATA REGISTERS

Each port can read and write its own data register at the two memory locations designated as Data and Data/Increment. If a memory operation is performed to the RAM via the data/increment location, the corresponding address pointer register will be incremented on completion of the memory cycle. This will not happen if the Data location is used.

ADDRESS POINTER REGISTERS

Each port can read and write its own address pointer register at the location designated as the Local Address Pointer and can read and write the other port's pointer at the Remote Address Pointer location. This enables each port to determine where in the RAM it will operate by setting up its own address pointer register. Alternatively, the management of the RAM can be under the control of only one port, which sets up both address pointers. Each pointer register will cycle through the value FF_{16} increments to OO_{16}. The following limitations apply to the use of these locations:

1. If either address pointer is read while its value is being changed by a write operation from the other port, an erroneous value may be read.
2. A port should not write to its remote address pointer location while there is a possibility that the other port could perform a memory operation to the RAM. This can result in the address pointer being changed during a memory operation and data in the RAM being corrupted.

Figure 1.
WD99650
BLOCK DIAGRAM

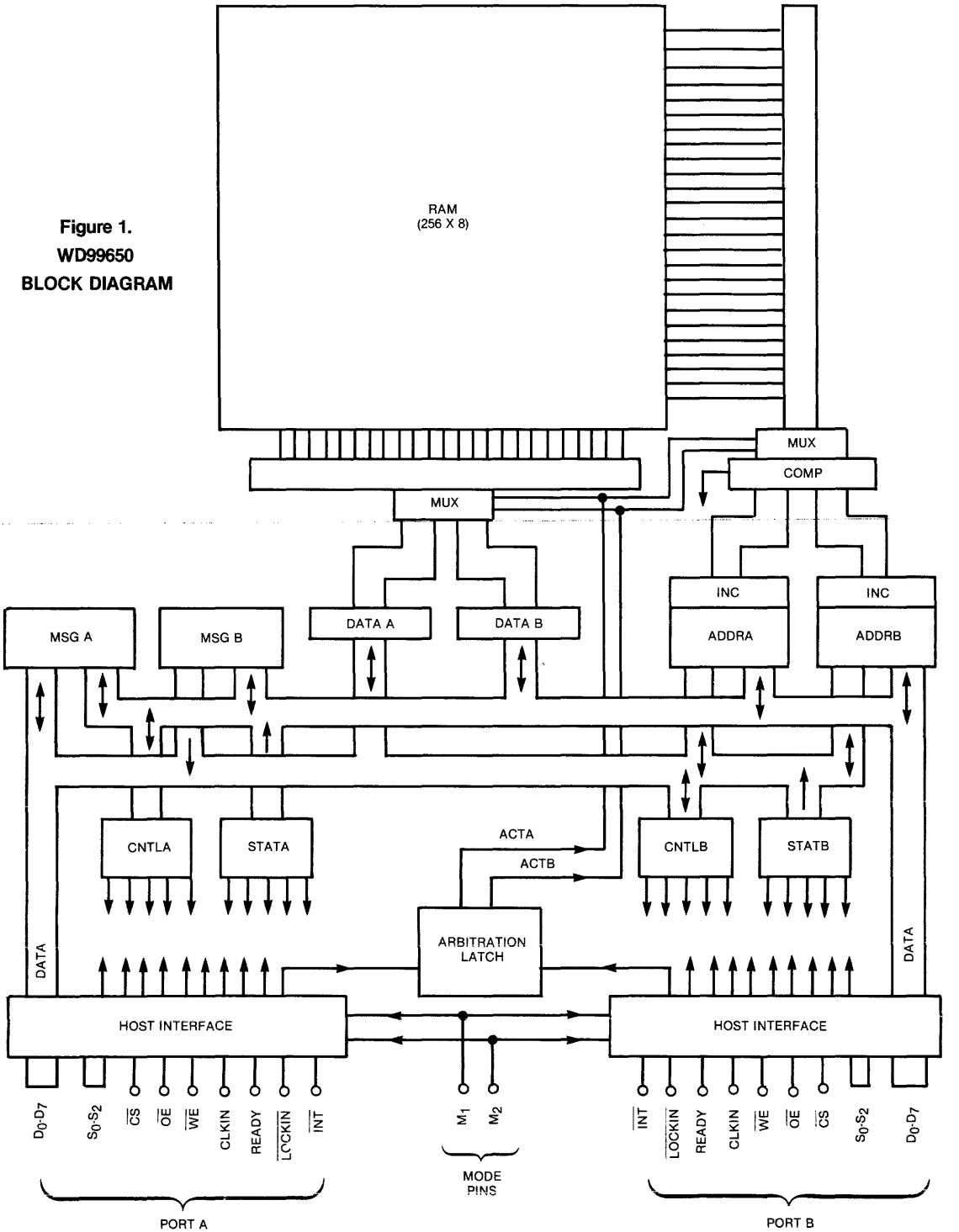


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Table 1. WD99650 REGISTER MAP

REGISTER SELECT LINES S_0, S_1, S_2	REGISTER FUNCTION	REGISTER SELECTED		READ/WRITE
		PORT A	PORT B	
000	DATA/INCREMENT	DATA A	DATA B	R/W
001	DATA	DATA A	DATA B	R/W
010	MESSAGE IN	MESSAGE B	MESSAGE A	R
011	MESSAGE OUT	MESSAGE A	MESSAGE B	R/W
100	CONTROL	CONTROL A	CONTROL B	R/W
101	LOCAL ADDRESS POINTER	ADDRESS A	ADDRESS B	R/W
110	STATUS	STATUS A	STATUS B	R
111	REMOTE ADDRESS POINTER	ADDRESS B	ADDRESS A	R/W

MESSAGE REGISTERS

Each port can read and write its own message register at the location designated as Message Out. In addition, it only reads that of the other port at the Message In Location. The message registers are implemented as two 8-bit registers, which can be written to at any time from their corresponding interface. During a write operation, the previous value of the register is held in a latch so that if a read operation occurs concurrently with the write, the previous value of the status register will be read. This means that the hosts may poll their remote status registers at any time without fear of reading an invalid code:

Interrupts are provided to support passing messages (see Status Registers).

CONTROL REGISTERS

Control registers can be written to and read by their respective hosts at any time. The bit assignment is shown in Figure 2.

IEN_1-IEN_5 Interrupt Enable Bits: When set to 1, these allow their respective interrupt status bits to set the INT status bit and pull low the INT line.

LEA Lockout On Equal Addresses Pointer: If this feature is set from either port, it is active for the entire device. When this feature is enabled and the address pointer registers become equal, the port corresponding to the last address pointer register to change will be locked out of the RAM. This will occur regardless of whether the change was due to incrementing or loading from either port. The lockout will persist as long as the above condition remains true.

SLOC Software Lockout Bit: This provides a software-accessible means of requesting that the remote port be locked out of the RAM.

All bits of the control register are cleared by the reset function of the mode pins, M_1 and M_2.

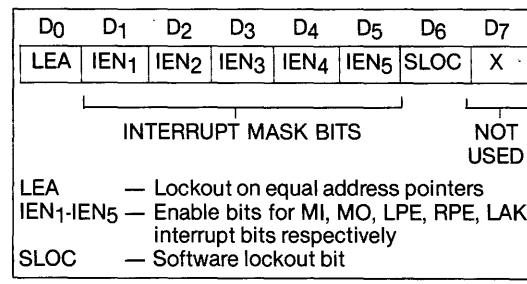


Figure 2.
WD99650 CONTROL REGISTER BIT ASSIGNMENT

STATUS REGISTERS

Each status register is read only and allows its corresponding host to inspect the status of various parameters on-chip. All may cause an interrupt if the appropriate interrupt enable bit is set to a 1. The bit assignment is shown in Figure 3.

INT Interrupt Asserted: An interrupt status bit has been set, and the INT line is pulled low.

MI Message In Interrupt: A byte should be read from the Message In register. It is set when the remote port loads its Message Out register and is cleared when the local port reads its Message In register. It is cleared by the reset function.

MO Message Out Interrupt: The local message register is available for use. It is cleared when a byte is written to the local Message Out register and set when the remote Message In register is read. It is set by the reset function.

LPE Local Pointer Equal to Remote Pointer: The address pointer registers are equal, and the local pointer was the last one to change, whether by incrementing or by loading from either port. It remains true as long as the condition persists.

RPE Remote Pointer Equal to Local Pointer: The address pointer registers are equal, and the remote address pointer was the last one to change, whether by incrementing or loading from either port. It remains true as long as the condition persists.

LAK Lockout Acknowledge: This is set following the assertion of SLOC by the local port when the lockout of the remote port from the RAM becomes effective. It is cleared when SLOC is cleared.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
INT	MI	MO	LPE	RPE	LAK	X	X
INTERRUPT STATUS BITS						NOT USED	

INT — Interrupt occurred
MI — Message in
MO — Message out
LPE — Local address pointer equal to remote address pointer
RPE — Remote address pointer equal to local address pointer
LAK — Lockout acknowledge

Figure 3.
WD99650 STATUS REGISTER BIT ASSIGNMENT

HOST INTERFACES

The simplest read and write operations for the WD99650 are shown in Figure 4A & 4B. READY and CLKIN are not shown since the memory cycles here apply to all registers except the data register. They will apply to the data register only if READY is not used. As with the register map, the host interfaces are identical, both electrically and functionally.

The desired register is selected by putting the appropriate code (see Pin Description) on the register select lines (S_0-S_2) and by putting chip select ($\overline{CS}$) low. If a write operation is desired, a negative-going pulse is applied to the write enable pin ($\overline{WE}$), and valid data is set up on the data lines (D_0-D_7) sooner than the required setup time before the rising edge of the write enable. If a read operation is desired, the output enable ($\overline{OE}$) signal is set low, which brings the WD99650 data lines out of a high impedance state. The data that they display will only be valid after the appropriate access time has elapsed from the register being selected. The required setup times, access times, etc. are given in ARBITRATION AND SYNCHRONIZATION.

READY AND CLKIN

Although the WD99650 host interfaces can function without the READY and CLKIN signals, both signals are required if concurrent access to the RAM is desired by both host systems. Under these conditions, the selection of one interface or the other on to the RAM is done by the arbitration latch. The host interface logic is responsible for putting into a wait state the host which is unsuccessful in gaining access.

When a host system addresses the data register of the WD99650 (chip select low and the appropriate code on the register select lines), READY is immediately set low regardless of whether or not access is actually gained to the RAM. READY will then stay low, and the interface will remain in a wait state until any uncertainty in the arbitration latch has resolved itself and access has been clearly gained.

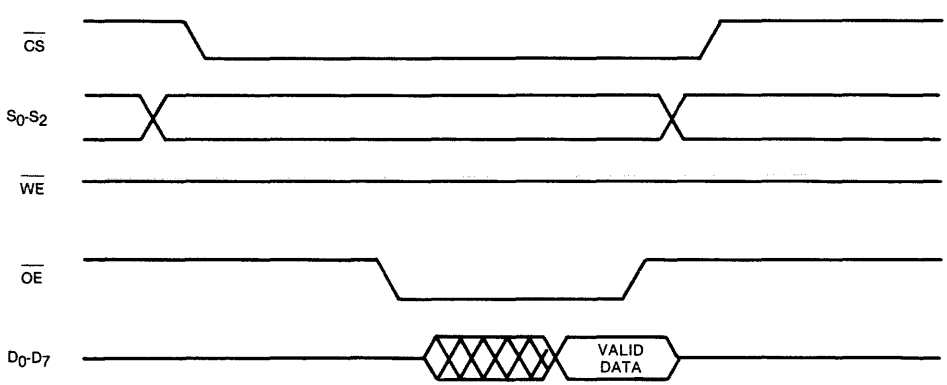


Figure 4A. READ OPERATIONS

Since the majority of systems will not accept an asynchronous READY signal, synchronization is provided on the WD99650. The falling edge of READY is generated by the CPU addressing its data register, so it is already synchronous. The rising edge, however, is not and must be synchronized to the system clock. CLKIN is provided for this purpose alone.

Each output of the arbitration latch is monitored by a threshold detector. which tests for a level in excess of the metastable level. ACTA or ACTB reaching this level indicates any conflict has resolved itself, and the corresponding port has gained access to the RAM. During the CLKIN high period, the output of the threshold detector is sampled as shown in Figure 5. When CLKIN is low, the feedback is applied to consolidate the sampled value so that any indeterminate sample will go to a valid 1 or 0 level. If a 1 is detected indicating that the memory cycle can proceed, then READY is set high on the next rising edge of CLKIN.

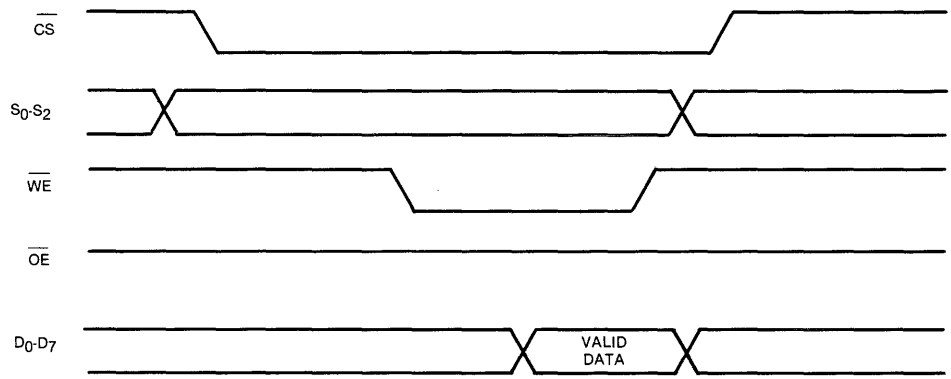


Figure 4B. WD99650 WRITE OPERATIONS

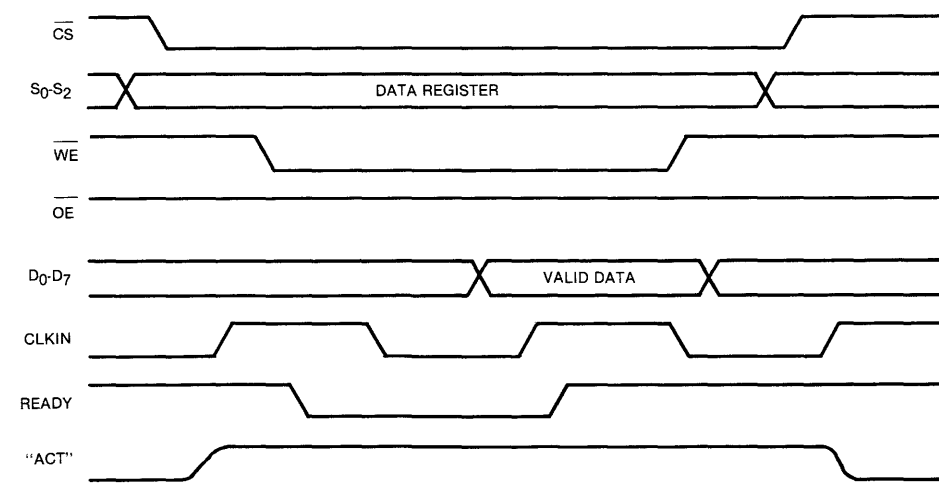
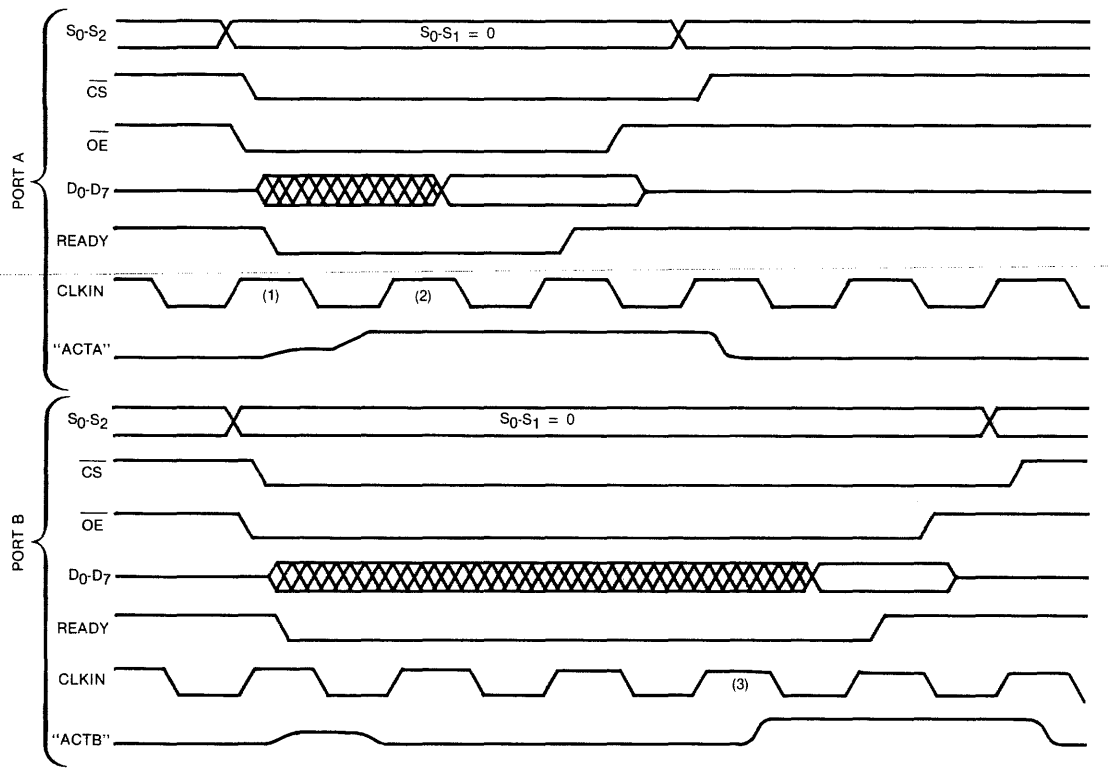


Figure 5. OPERATION OF READY AND CLKIN

Figure 6 shows the result of two read cycles beginning at the same time. When the data registers are addressed, the ACTA and ACTB bits both begin to rise. As they are both mutually exclusive, a metastable condition is reached. It is significantly later that a result is seen from this conflict when, in this case, port A gains access and port B does not. READY is taken low on both ports as soon as the data registers are addressed. At port A during the first subsequent CLKIN high period (1), ACTA is not seen as having a VALID high level. Therefore, it is the value sampled in the second CLKIN high period (2) that results in READY being set high on the next rising edge of CLKIN. Note that ACTA selects the data and local address pointer registers of port A on to the data and address lines of the RAM. It is not until after ACTA reaches a good 1 level that valid data is seen on the port A data lines. Port A then completes its memory cycle and ceases to address its data register. ACTA, therefore, goes low again, which allows ACTB to rise to a 1 level. This fact is detected in the CLKIN high period of port B (3), and READY goes high on the next rising edge. Up to this point, the data lines of port B have been displaying invalid data. This becomes valid after ACTB reaches a good 1 level. The memory cycle port B can then be completed.



NOTE: ACTA AND ACTB ARE INTERNAL SIGNALS.

Figure 6. SIMULTANEOUS READ CYCLES FROM BOTH PORTS

LOCKOUT CAPABILITY

Both ports have a lockout feature that can be asserted by either one of two means: (1) by putting a low level on the $\overline{LOCKIN}$ input of the host interface, or (2) by writing a 1 to the SLOC bit of the control register. If a lockout is asserted by the local port, then the ACT bit of the remote port is held low. Thus if the remote port addresses its data register, it will not get access to the RAM. If CLKIN and READY are used on the remote port, it will enter a wait state until the lockout is removed.

The assertion of a lockout will not guarantee immediate exclusive use of the RAM. A lockout asserted by the local port will only become effective after any memory operation to the RAM by the remote port has been completed. It will also not be effective until any lockout asserted by the remote port has been cleared. Lockouts, therefore, are mutually exclusive in a similar way to ACTA and ACTB, and concurrent lockout requests from both ports are assigned on a first-come, first-serve basis.

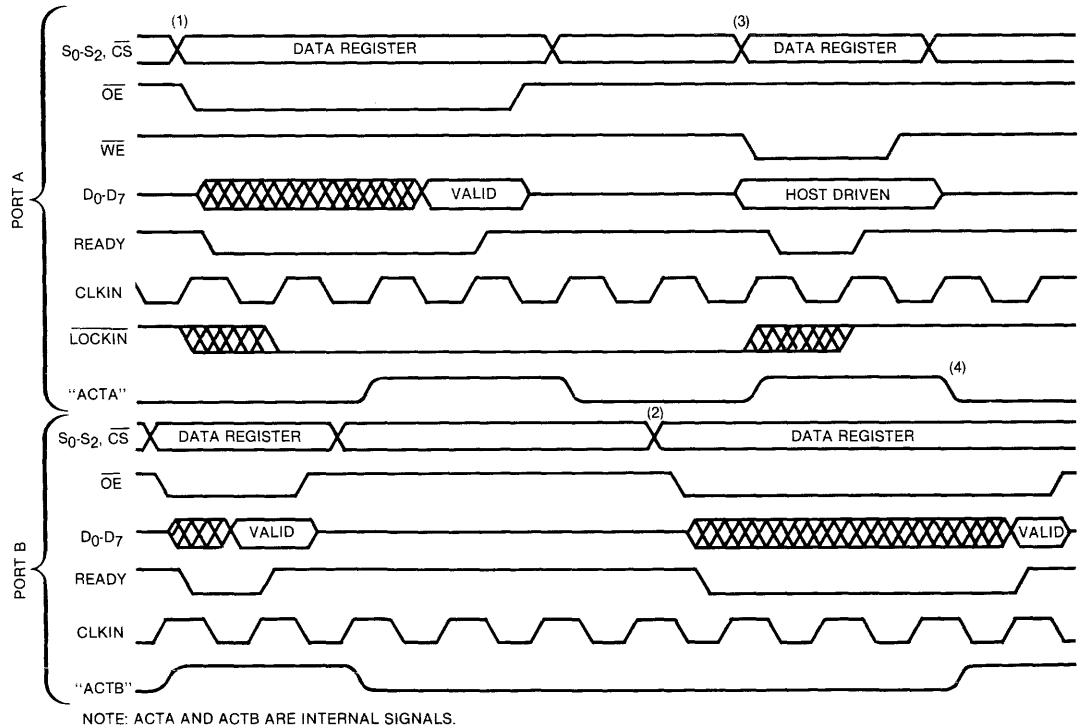
Figure 7 shows an example of the lockout facility being used to implement an indivisible read-modify-write operation. Port A performs the read and write operations with a lockout asserted between them by means of the LOCKIN input. At the time when port A tries to do a read from the RAM (1), there is already a read cycle in progress on port B. Port A, therefore, enters a wait state until this operation is complete even though the LOCKIN input is asserted. When the read cycle at port B is complete, the memory operation at port A can proceed and, in addition, the lockout of port B becomes effective. Consequently, when the next memory operation is initiated to port B (2), it enters a wait state even though there is no activity on port A. Port A then enters a write cycle (3), during which the LOCKIN is removed. When the write cycle ends and ACTA goes low (4), ACTB can rise in the absence of the lockout and the memory operation can also be completed here. Therefore, the read and write operations at port A cannot be interfered with from port B. LOCKIN would be derived from a multiprocessor interlock-type signal in host system B.

In a system where the user does not wish to use the READY and CLKIN signals on a particular port, the SLOC bit can be used to guarantee that access is gained to the RAM. The LAK interrupt status bit will be set in response to SLOC as soon as the lockout becomes effective. Thus LAK will not be set until any current memory cycle to the RAM from the remote port has been completed and any lockout that the remote port may have asserted has been cleared. After this, the local port has exclusive use of the RAM until it clears SLOC.

ADDRESS POINTER EQUAL INTERRUPTS AND LOCKOUT

If it is desired to move data blocks of greater than 256 bytes between systems, the WD99650 can be used to implement a circular buffer to absorb any data transfer rate mismatch between systems. Consider the case of system A (connected to port A) sending a block of data to system B. Both systems implement the MPIF READY signal.

To begin the transfer, the address pointer registers of both ports are set the same. This is done by either host system if the address pointer of port B is set up last. This generates an RPE interrupt to system A and an LPE interrupt to system B, these serving as buffer empty interrupts. Normally, system B should then avoid reading the RAM until the LPE interrupt has gone. However, if the LEA feature is enabled, system B can begin its first read. It will enter a wait state until the first byte is written into the buffer. When system A starts loading data via its data/increment register, the equality of pointers is removed, and the receiving



NOTE: ACTA AND ACTB ARE INTERNAL SIGNALS.

Figure 7. TYPICAL READ-MODIFY-WRITE OPERATION USING LOCKIN

system can sequentially read the data via its data/increment register. If the reading pointer succeeds in catching up with the writing pointer, then system A will again receive an RPE and system B an LPE and a lockout (assuming LEA is set) indicating that the buffer is empty.

If the sending system succeeds in getting 256 bytes ahead of the receiving system, then the address pointers again become equal. This time, system A gets the lockout and an LPE interrupt, and system B gets an RPE interrupt. This corresponds to a buffer full interrupt, and the sending system will be prevented from writing more data until there is room for it.

Another possible method of buffering large data streams is as follows: If the sending interface in the above example fills the buffer and receives an LPE interrupt, then it may subtract a certain number from that in its local address pointer and reload it with the result. It will be interrupted when there is this certain number of bytes left in the buffer and may return the original value to the address pointer and refill the buffer. However, the sending system should return the original value to its local address pointer if it enters a condition where it is unable to respond to an interrupt before the remaining bytes in the buffer are read.

An equivalent procedure can be undertaken by the receiving host system. This time, a certain number is added to the pointer register and an RPE interrupt received when there is that number of bytes in the buffer.

MODE PINS

The mode pins, M_1 and M_2, are used to reset the WD99650 and to enable several WD99650s to be used in parallel on memory buses of greater than 8 bits. There are four modes encoded on these pins: reset ($M_1 = M_2 = 0$), standalone ($M_1 = M_2 = 1$), master ($M_1 = 0$, $M_2 = 1$), and slave ($M_1 = 1$, $M_2 = 0$). Schmitt triggers are provided on both inputs to permit the use of a resistor and capacitor arrangement to implement reset.

Reset ($M_1 = M_2 = 0$)

The reset function establishes the following conditions on-chip:

1. All bits of the control register cleared
2. The MI interrupt status bit cleared
3. The MO interrupt status bit set
4. The data lines (D_0-D_7) of the host interfaces held in a high impedance state
5. The READY output of each port held in a high impedance state.

The other three combinations of the mode pins are operating modes.

Standalone Mode ($M_1 = M_2 = 1$)

The standalone mode is the operating mode of a single WD99650. To implement reset with this mode of operation, both M_1 and M_2 should be connected to an active-low system $\overline{\text{RESET}}$ signal.

Master ($M_1 = 0$, $M_2 = 1$) and Slave ($M_1 = 1$, $M_2 = 0$) Modes

The master and slave modes are included to avoid the possibility of problems occurring in multiple WD99650 arrangements. During simultaneous attempts at getting access to the RAM by both ports, it is possible for the arbitration latches of different devices in standalone mode to fall in opposite directions with consequent system malfunction. Master and slave modes allow the arbitration latch in only one WD99650 to decide which port should have access. This decision is then passed on to the remainder. Figure 8 shows an example of a multiple WD99650 system.

To implement the reset function on the master device, M_2 should be connected to the system $\overline{\text{RESET}}$ signal, and M_1 should be grounded. In normal operation, the timing of the READY line of each port is changed to provide an unclocked, active-high indication of when that port has gained access to the RAM. A CLKIN input is, therefore, not required by the master device.

On the slave devices, M_1 is connected to the system $\overline{\text{RESET}}$ line, and M_2 is grounded. In this mode, the $\overline{\text{LOCKIN}}$ signals of each port become enable inputs, which are connected directly to the modified READY outputs of the corresponding port of the master device. The slave has no arbitration and responds to a high level on the READY output of the master by granting access to the appropriate port immediately. At this time, it also begins the procedure of releasing its own READY line which is synchronized in the same way as on the standalone device. Hence, a CLKIN must be supplied to the slave devices. In dual WD99650 arrangements, the READY outputs of the slave may be taken directly to the READY input of the host systems. With more than one slave, the READY outputs of each port should be ANDed together to ensure that all WD99650s give access to the port before READY is released.

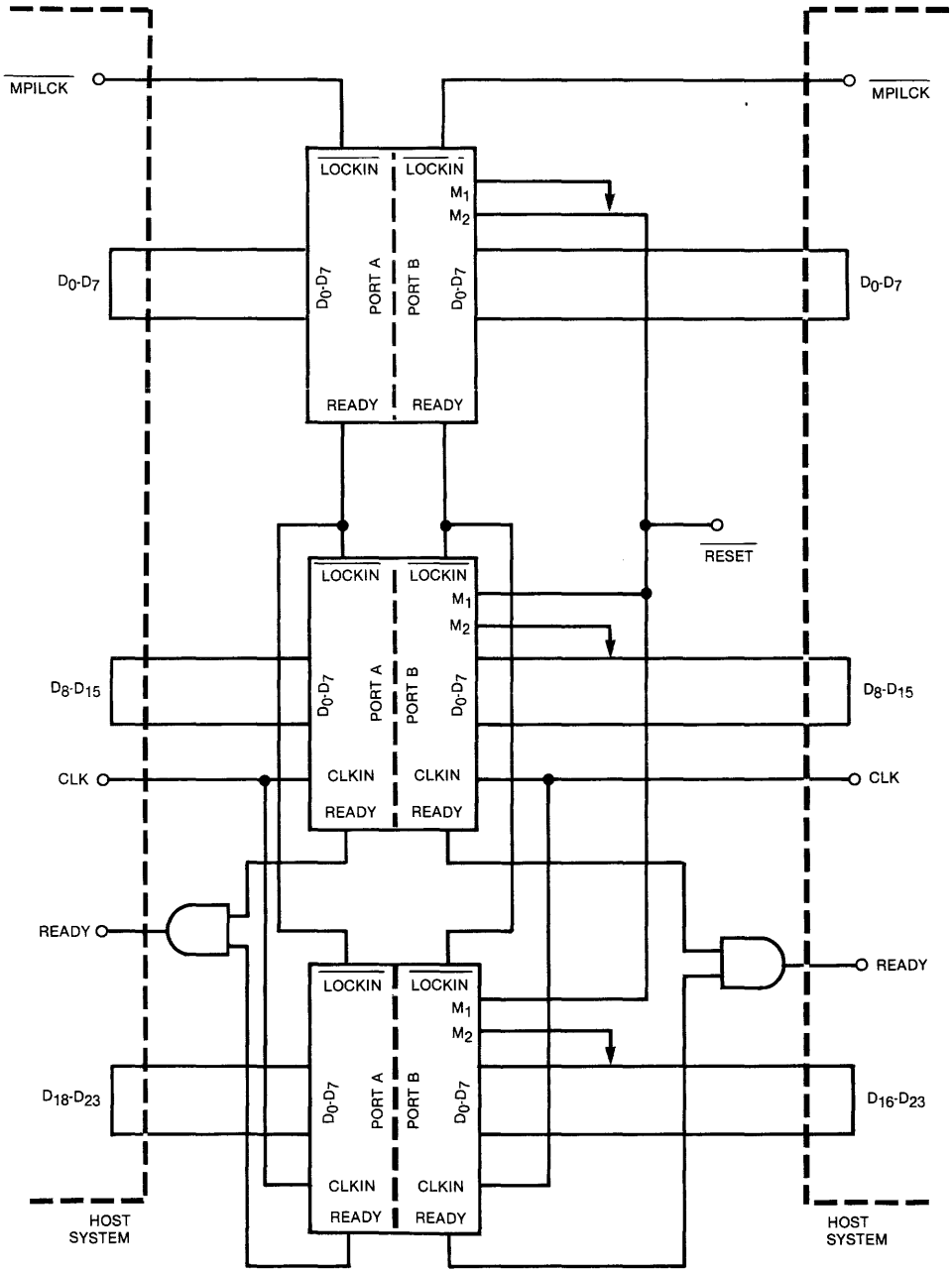


Figure 8. MULTIPLE WD99650 CONFIGURATION

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage ..... −0.3 to 20V
Off-state output voltage ..... −0.3 to 7V
Continuous power dissipation ..... 1 W
Operating free-air temperature range ... 0°C to 70°C
Storage temperature range ..... −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:
Voltage values are with respect to network ground terminal, V_{SS}.

RECOMMENDED OPERATING CONDITIONS

	MIN.	NOM.	MAX.	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage (All inputs), V_{IH}	2			V
Low-level input voltage (All inputs), V_{IL}			0.8	V
High-level output current, I_{OH} (All outputs except $\overline{INT}$)			100	μA
Low-level output current, I_{OL}				
All except $\overline{INT}$			2	mA
$\overline{INT}$ output only			2.5	mA
Operating free-air temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED FREE-AIR TEMPERATURE RANGE

	PARAMETER	TEST CONDITIONS†	MIN.	TYP.‡	MAX.	UNIT
V_{OH}	High-level output voltage	V_{CC} = min, I_{OL} = max	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = min, I_{OL} = max			0.4	V
I_O	Off-state (high-impedance state) output current	V_{CC} = max, V_O = 2.4 V			20	μA
		V_{CC} = max, V_O = 0.4 V			−20	μA
I_I	Input current	V_I = V_{SS} to V_{CC}			±50	μA
I_{OS}	Short-circuit output current§	V_{CC} = max				μA
I_{OC}	Supply current	V_{CC} = max				
C_i	Input capacitance (except data bus)	f = 1 MHz, all other pins at 0 V		15		pF
C_{DB}	Data bus capacitance			25		pF
C_o	Output capacitance (except data bus)			10		pF

† For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

TIMING REQUIREMENTS AND CHARACTERISTICS

	PARAMETER	CONDITION	SEE NOTE	SEE FIGURE	MIN.	TYP.	MAX.	UNIT
t_{SU1}	Register select setup time for write	Data register		9	205			ns
		$S_0 = S_1 = 0$ Otherwise		9	150			ns
t_{SU2}	Chip select setup time for write	Data register		9	195			ns
		$S_0 = S_1 = 0$ Otherwise		9	140			ns
t_{SU3}	Data setup time for write	Data register		9	150			ns
		$S_0 = S_1 = 0$ Otherwise		9	50			ns
t_{WL2}	Write enable low pulse width	Data register		9	200			ns
		$S_0 = S_1 = 0$ Otherwise		9	70			ns
t_{H1}	Data hold time for write			9	0			ns
t_{H2}	Chip select hold time for write			9	0			ns
t_{H3}	Register select hold time for write			9	0			ns
t_{H4}	Hold time of write enable after CLKIN rising edge during concurrent RAM accesses	Data register	7	12	140			ns
t_{AC1}	Access time from register select for read	Data register	1, 2	10			185	ns
		$S_0 = S_1 = 0$ Otherwise	1	10		85		ns
t_{AC2}	Access time from chip enable for read	Data register	1, 2	10			175	ns
		Otherwise	1	10		75		ns
t_{AC3}	Access time from output enable for read	Data register	1, 2	10			100	ns
		$S_0 = S_1 = 0$ Otherwise	1	10		40		ns
t_{P1}	Chip select to data bus Hi-Z		1	10		40		ns
t_{P2}	Output enable to data bus Hi-Z		1	10			30	ns
t_{AC4}	Access time from CLKIN low during concurrent RAM accesses	Data register	1, 7	12			120	ns
		Data register $C_L = 25$ pF	1, 7	12			100	ns
t_{H5}	Chip select hold time after valid data	Data register	3	10			2	μs
t_{H6}	Output enable hold time after valid data	Data register	3	10			2	μs
t_{P3}	Chip select to ready low	Data register	1	11		40		ns
t_{P4}	Register select to ready low	Data register	1	11		50		ns
t_{P5}	CLKIN to ready high	Data register	1	11		40		ns
		Data register $C_L = 25$ pF	1	11			20	ns
t_{SU4}	Chip select setup time to CLKIN	Data register	4	11	55			ns

TIMING REQUIREMENTS AND CHARACTERISTICS (Concluded)

	PARAMETER	CONDITION	SEE NOTE	SEE FIGURE	MIN.	TYP.	MAX.	UNIT
t_{SU5}	Register select setup to CLKIN	Data register	4	11	60			ns
t_{SU6}	$\overline{\text{LOCKIN}}$ setup to end of access	Data register	5	11	100			ns
t_{WL1}	CLKIN low pulse width			11	60			ns
t_{WH1}	CLKIN high pulse width			11	45			ns
t_{P6}, t_{P7}	End of memory cycle to interrupt		1, 6	13			200	ns

NOTES:

1. Figure 14 shows the load circuit used to measure the timing characteristics of output and I/O pins. A value of C_L = 100 pF is used except where otherwise stated. R_1 is only included for open drain outputs.
2. These times only apply when the port in question gets immediate access to the RAM. Otherwise, the access time is determined by t_{AC4}.
3. Only one of the time t_{H5} or t_{H6} need be satisfied. These specify the maximum length of a RAM read operation after access has been gained.
4. These setup times need to be met if READY is to be set high on the next rising edge of CLKIN. If this is not the case, then READY will not be released until one CLKIN cycle later.
5. This setup time is required if $\overline{\text{LOCKIN}}$ is to be effective immediately after the termination of the memory access to the RAM. The memory access may be terminated either by $\overline{\text{CS}}$ going high or the address lines changing.
6. This is the delay of the interrupt line from the termination of the memory cycle that causes it. The cycle is terminated when $\overline{\text{CS}}$ goes high or when either $\overline{\text{OE}}$ or $\overline{\text{WE}}$ goes high.
7. These parameters describe the access time and required WE hold times when access to the RAM is not immediately achieved and the host system enters more than one wait state. The parameters are measured from the falling edge of CLKIN on which the corresponding ACT bit is first sampled as being high. This sampled value indicates that access to the RAM has started and results in READY are being released on the next rising edge of CLKIN.

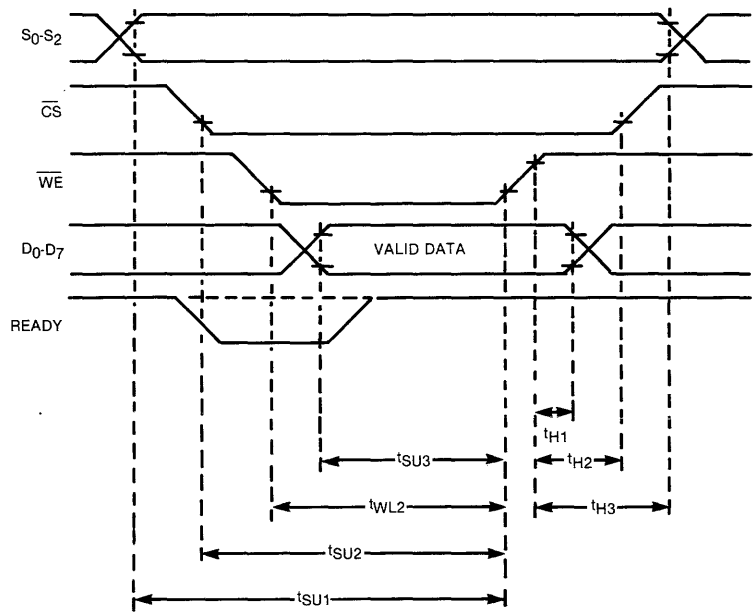


Figure 9. WRITE CYCLE TIMING CHARACTERISTICS

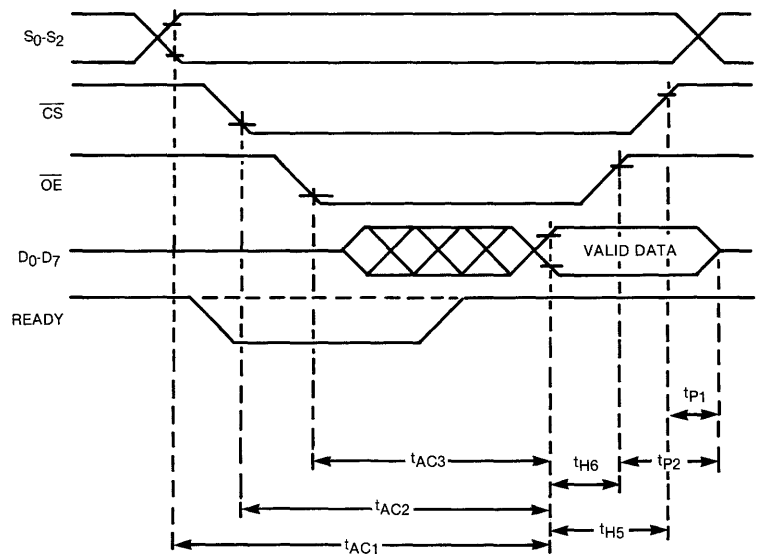


Figure 10. READ CYCLE TIMING CHARACTERISTICS

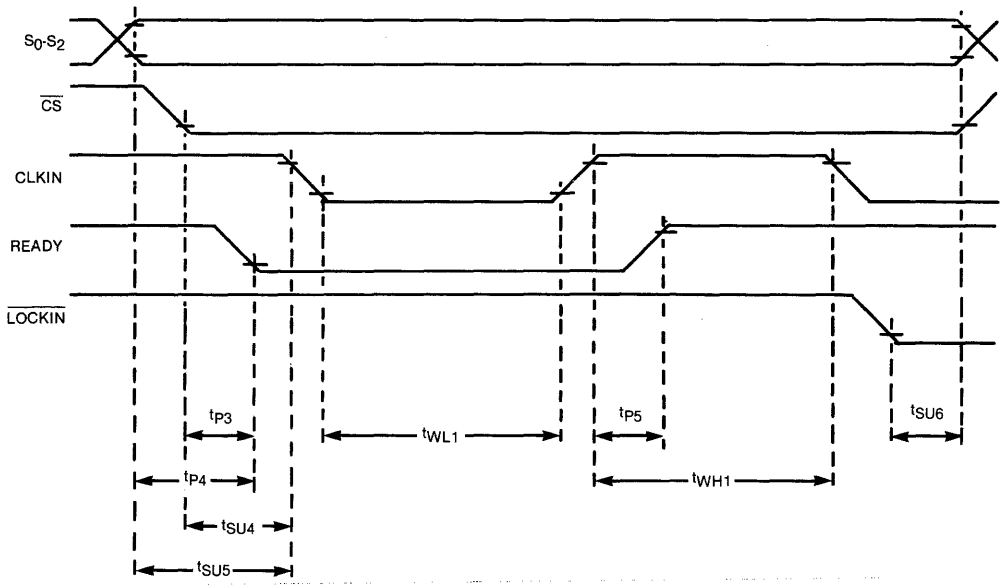


Figure 11. READY, CLKIN AND LOCKIN TIMING CHARACTERISTICS

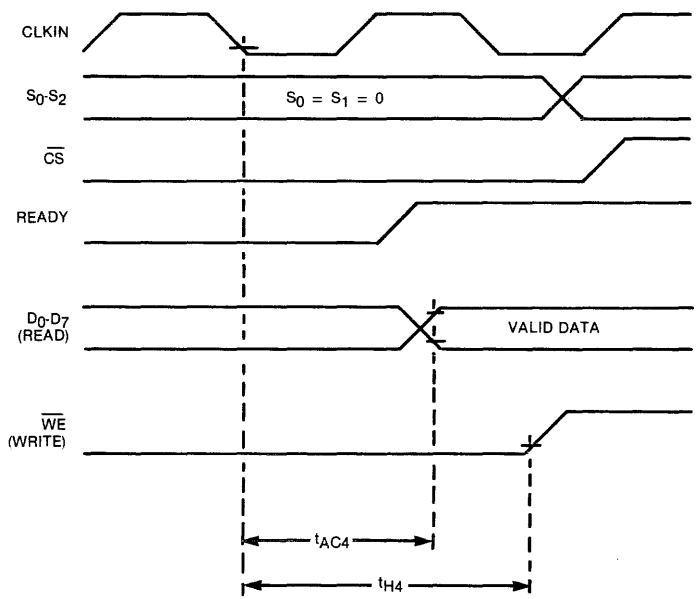


Figure 12. DATA WRITE CHARACTERISTICS

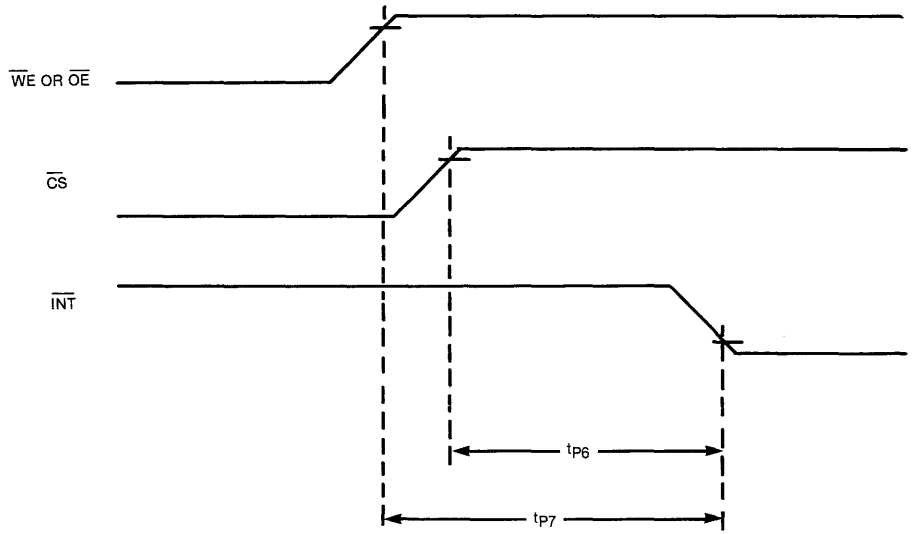


Figure 13. INTERRUPT TIMING CHARACTERISTICS

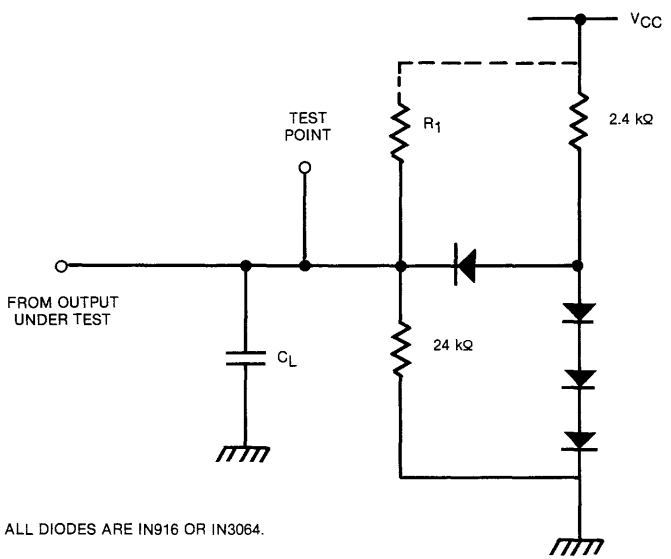


Figure 14. TEST LOAD CIRCUIT

See page 481 for ordering information.

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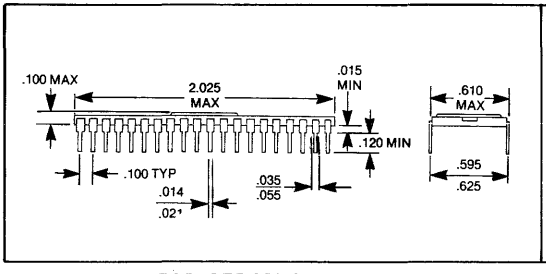
ORDERING INFORMATION

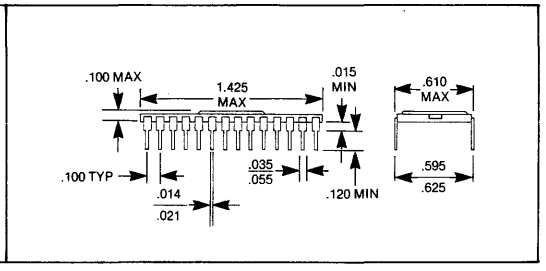
The following listing indicates the available packages for each product. The letter designation refers to the package diagrams, beginning on page 531.

Product	Plastic	Ceramic	CER-DIP
WD1010-00/01/05/08	PL	AL	CL
WD1011	P		C
WD1012	P		C
WD1014-00, 01	PL	AL	CL
WD1015-00, 01, 02			CL
WD1050			
WD1100-01	PE		CE
WD1100-02	PE		CE
WD1100-03	PE		CE
WD1100-04	PE		CE
WD1100-05	PE		CE
WD1100-06	PE		CE
WD1100-07	PE		CE
WD1100-09	PE		CE
WD1100-10	PE		CE
WD1100-11	PL		CL
WD1100-12	PE		CE
WD1100-13	PE		CE
WD1100-14	PE		CE
WD1691	V	U	CE
FD176X-02	PL	AL	CL
WD1770/72/73	PH	AH	CH
WD1771-01	PL	AL	CL
FD1781	PL	AL	
FD179X-02	PL	AL	CL
DM1883-A/B	PL	AL	CL
WD2010			
WD2143-03	M	L	CD
WD279X-02	PL	AL	CL
WD8206		DT	
WD8207		DT	
WD9216-00, 01	PA		
WD99650	PL	AL	CL

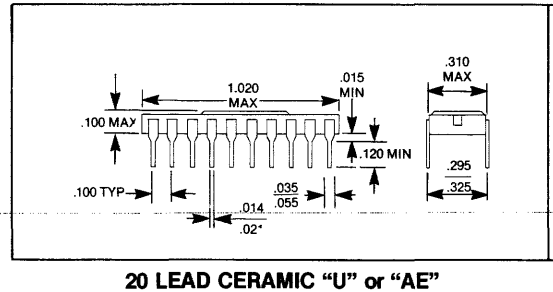
Package Diagrams



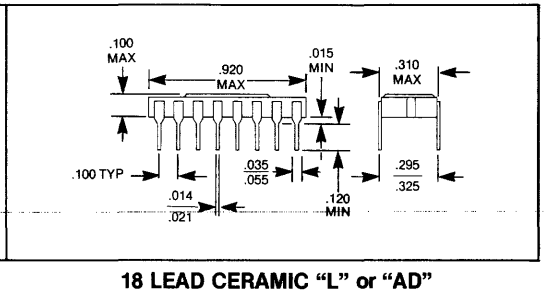
40 LEAD CERAMIC "A" or "AL"



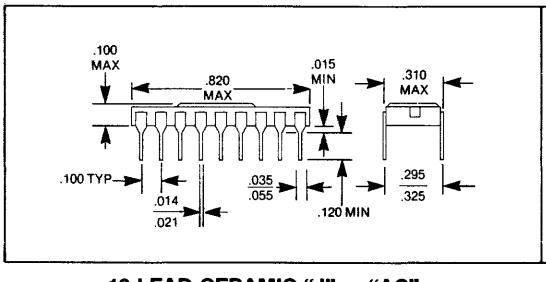
28 LEAD CERAMIC "E" or "AH"



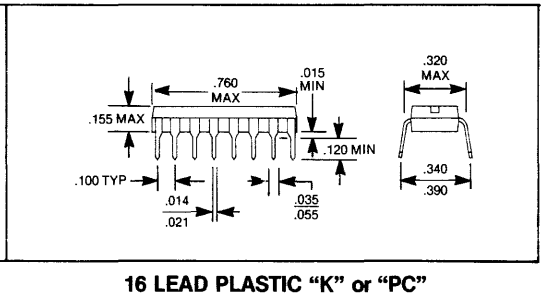
20 LEAD CERAMIC "U" or "AE"



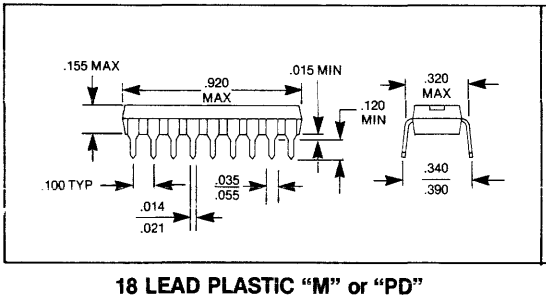
18 LEAD CERAMIC "L" or "AD"



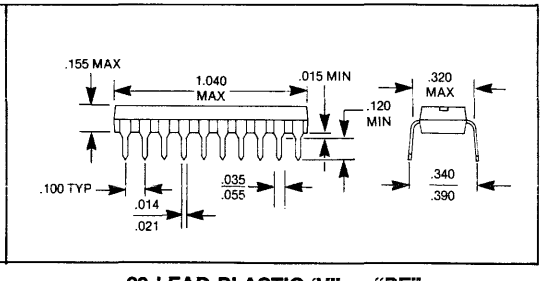
16 LEAD CERAMIC "J" or "AC"



16 LEAD PLASTIC "K" or "PC"

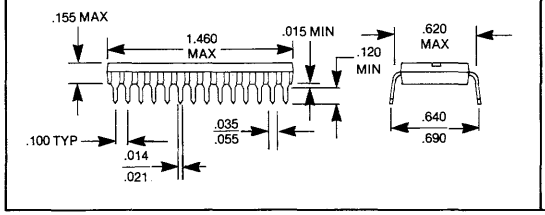


18 LEAD PLASTIC "M" or "PD"

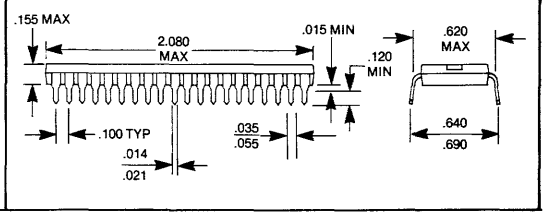


20 LEAD PLASTIC "V" or "PE"

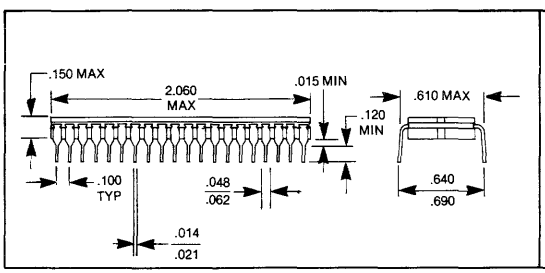
Package Diagrams



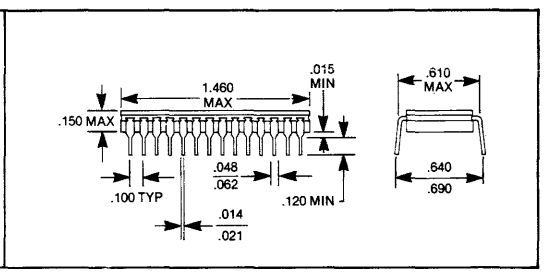
28 LEAD PLASTIC "R" or "PH"



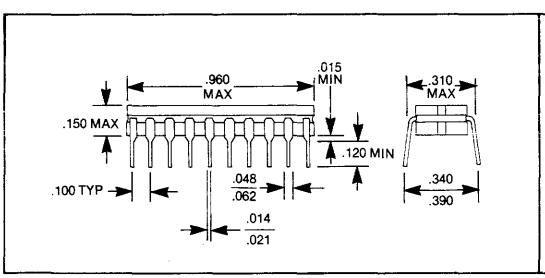
40 LEAD PLASTIC "P" or "PL"



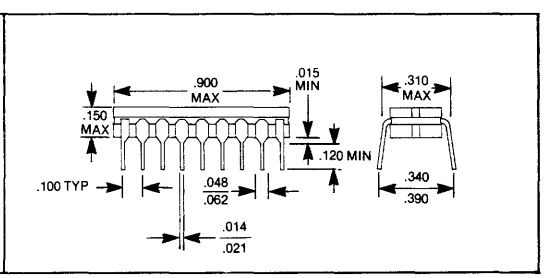
40 LEAD CERDIP "CL"



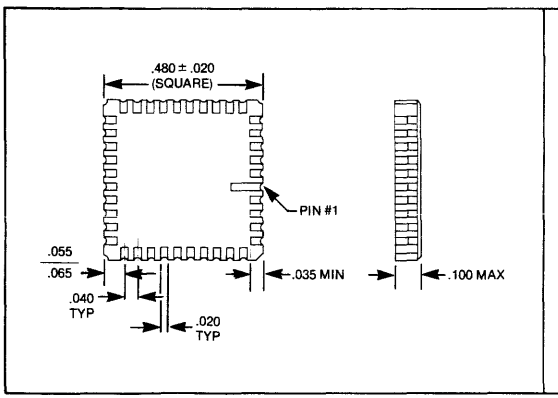
28 LEAD CERDIP "CH"



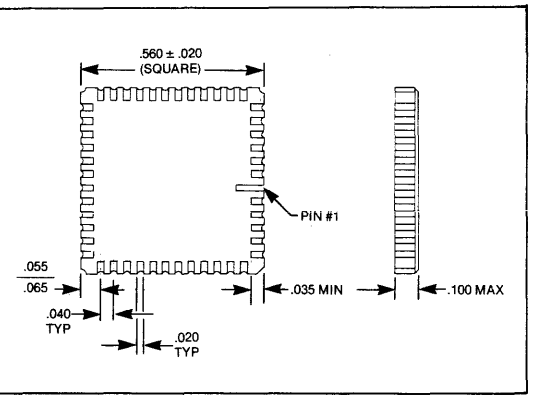
20 LEAD CERDIP "CE"



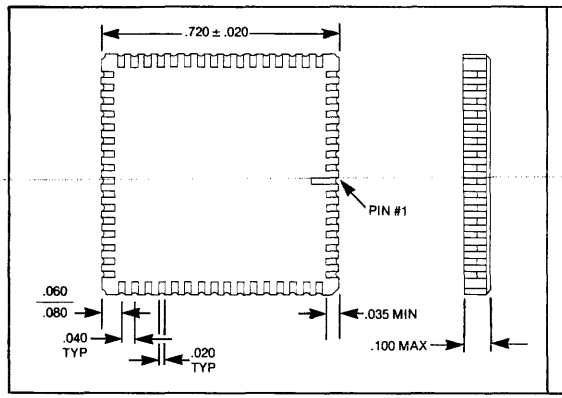
18 LEAD CERDIP "CD"



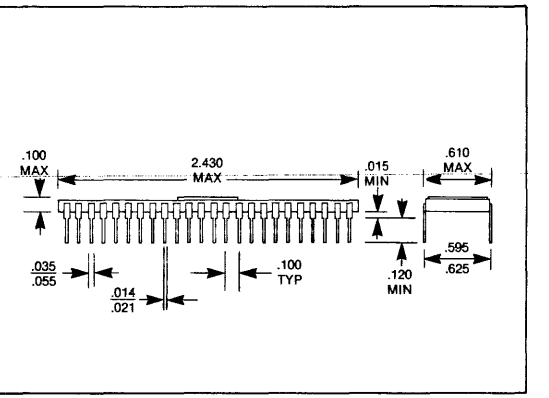
40 LEAD CERAMIC CHIP CARRIER "DL"



48 LEAD CERAMIC CHIP CARRIER "DN"



64 LEAD CERAMIC CHIP CARRIER "DS"



48 LEAD CERAMIC "T" or "AN"

Pin Compatibility Guide

	INTEL	NATIONAL	SIEMENS	TI
WD1010	82062			
FD1771-01		INS1771-1		
FD179X			SAB179X	
WD279X			SAB279X	
WD8206	8206			
WD8207	8207			
WD99650				TMS99650

Component Products
Terms and Conditions

1. **ACCEPTANCE:** Unless otherwise provided, it is agreed that sales are made on the terms, conditions and warranties contained herein and that to the extent of any conflict, the same take precedence over any terms or conditions which may appear on Buyer's order form. Seller shall not be bound by Buyer's terms and conditions unless expressly agreed to in writing. In the absence of written acceptance of these terms, acceptance of or payment for any of the articles covered hereby shall constitute an acceptance of these terms and conditions.

2. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of articles purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Unless specific instructions from Buyer specify which method of shipment is to be used, the Seller will exercise his own discretion.

3. **DELIVERY:** Shipping dates are approximate only. Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet the specified delivery schedule because of unavoidable production or other delays. Seller may deliver the articles in installments, Seller shall not be liable for any delay in delivery or for non-delivery, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, by way of illustration but not limitation, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof, judicial action, labor dispute, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw material or machinery or technical failure where Seller has exercised ordinary care in the prevention thereof. If any contingency occurs, Seller may allocate production and deliveries among Seller's customers.

4. **TERMS AND METHODS OF PAYMENT:** Where seller has extended credit to Buyer, terms of payment shall be net thirty (30) days from date of invoice. The amount of credit or terms of payment may be changed or credit withdrawn by Seller at any time. If the articles are delivered in installments, Buyer shall pay for each installment in accordance with the terms hereof. Payment shall be made for the articles without regard to whether Buyer has made or may make any inspection of the articles. If shipments are delayed by Buyer, payments are due from the date when Seller is prepared to make shipments. Articles held for Buyer are at Buyer's sole risk and expense.

5. **TAXES:** All prices are exclusive of all federal, state and local excise, sales, use, and similar taxes. Such taxes; when applicable to this sale or to the articles sold, will appear as separate additional items on the invoice unless Seller receives a properly executed exemption certificate from Buyer prior to shipment.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller, shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products of any part thereof.

7. **ASSIGNMENT:** The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY:** Seller warrants articles of its manufacture against defective materials or workmanship for a period of one year from date on which Seller delivers said articles. The liability of Seller under this warranty is limited at Seller's option, solely to repair, replacement with equivalent articles, or an appropriate credit adjustment not to exceed the original sales price of articles returned to the Seller provided that (a) Seller is promptly notified in writing by Buyer upon discovery of defects, (b) the defective article is returned to Seller, transportation charges prepaid by Buyer, and (c) Seller's examination of such article disclosed to its satisfaction that defects were not caused by negligence, misuse, improper installation, accident, or unauthorized repair or alteration by the Buyer. In the case of equipment articles, this warranty does not include mechanical parts failing from normal usage nor does it cover limited life electrical components which deteriorate with age. In the case of accessories, not manufactured by Seller, but which are furnished with the Seller's equipment, Seller's liability is limited to whatever warranty is extended by the manufacturers thereof and transferable to the Buyer. This Warranty is expressed in lieu of all other Warranties, expressed or implied, including the implied Warranty of fitness for a particlar purpose, and of all other obligations or liabilities on the Seller's part, and it neither assumes nor authorizes any other person to assume for the Seller any other liabilities. This Warranty should not be confused with or construed to imply free preventative or remedial maintenance, calibration or other service required for normal operation of the equipment articles. These Warranty provisions do not extend the original Warranty period of any article which has either been repaired or replaced by Seller. In no event will Seller be liable for any incidental or consequential damages.

9. **TERMINATION:** Buyer may terminate this contract in whole or from time to time in part upon 60 days written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of articles actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for pro-rated expenses and profits. Any termination or back off in scheduling will not be allowed on shipments scheduled for the month in which the request is made and for the month following.

10. **GOVERNMENT CONTRACTS:** If the articles to be furnished under this contract are to be used in the performance of a Government contract or subcontract and a Government contract number shall appear on Buyer's purchase order, those clauses of the applicable Government procurement regulation which are mandatorily required by Federal Statute to be included in Government subcontracts shall be incorporated herein by reference.

11. **ORIGIN OF ARTICLES:** Seller engages in off-shore production, assembly and/or processing and makes no warranty or representation, expressed or implied, that the articles delivered hereunder are United States articles or of U.S. origin for the purpose of any statute, law, rule, regulation or case thereunder. If Buyer ships the articles hereunder out of the U.S. for assembly, then at Buyer's request in writing, Seller shall provide information applicable to identification of any articles not of U.S. origin.

Corita Kent, the cover artist, is an American whose work presents an optimistic, yet philosophical view of the world we live in. A former Catholic nun and teacher, Corita now devotes her life and energies to her artwork and the "human needs she feels transcend national and religious barriers." A true "citizen of the world," Corita's philosophy positions her "on the positive side of hope." Her depiction of the Western Digital mission . . . "Making the leading edge work for you" . . . dramatizes the spectrum of solutions we provide our customers.

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